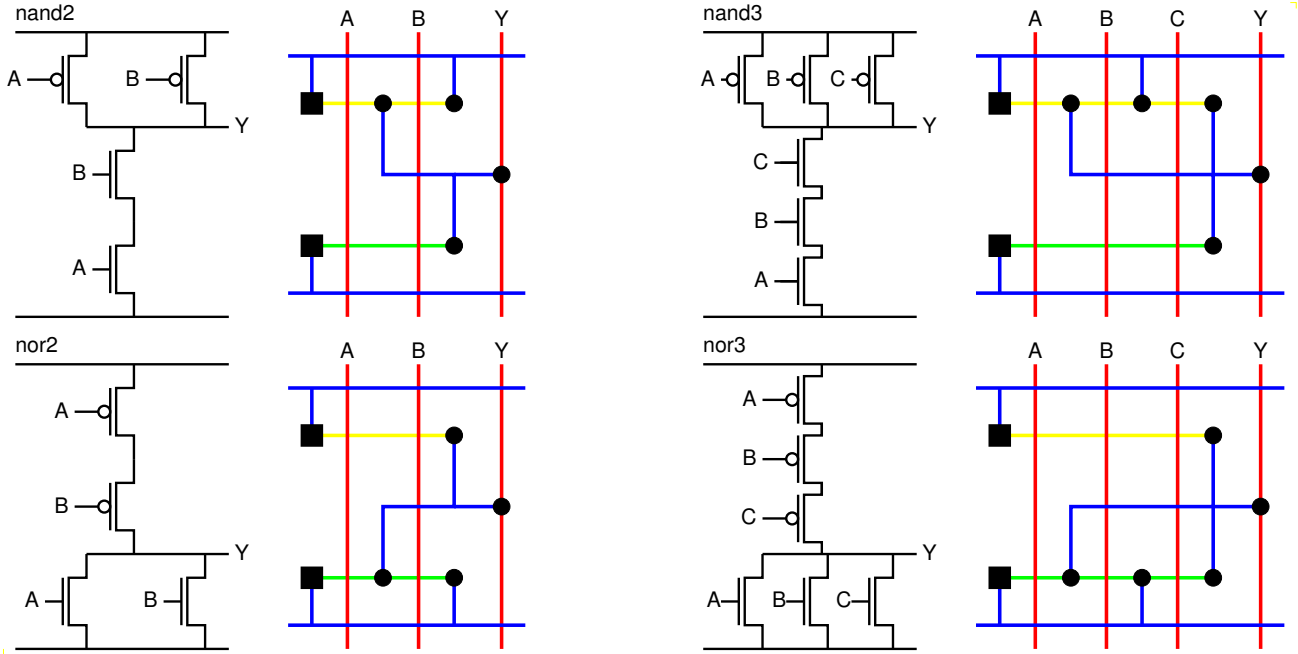
Mini Design Exercise 1

Design a 2 or 3 input NAND or NOR gate using AMS $0.35\mu m$ technology (c35b4) based on the appropriate stick diagram shown here[1].



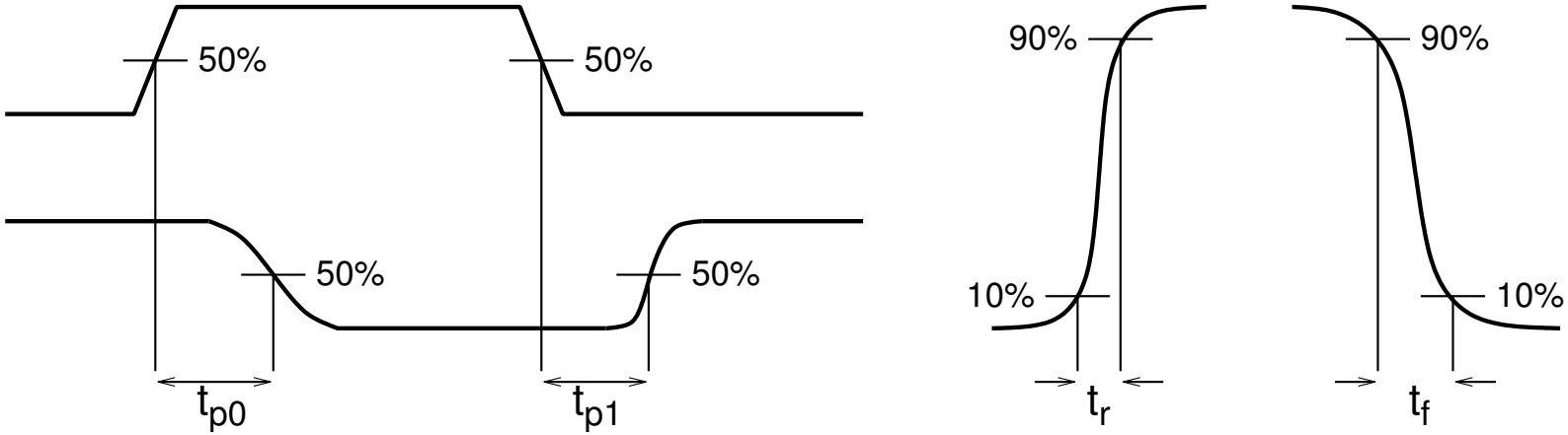
Optimize the gate for equal average rise and fall times based on restrictions you are given[2].

[1] start by editing your inverter and saving with a new name rather than starting from scratch

[2] type `get_desex1_restriction` at the unix command prompt to find your personal restrictions

Mini Design Exercise 1

Measurements

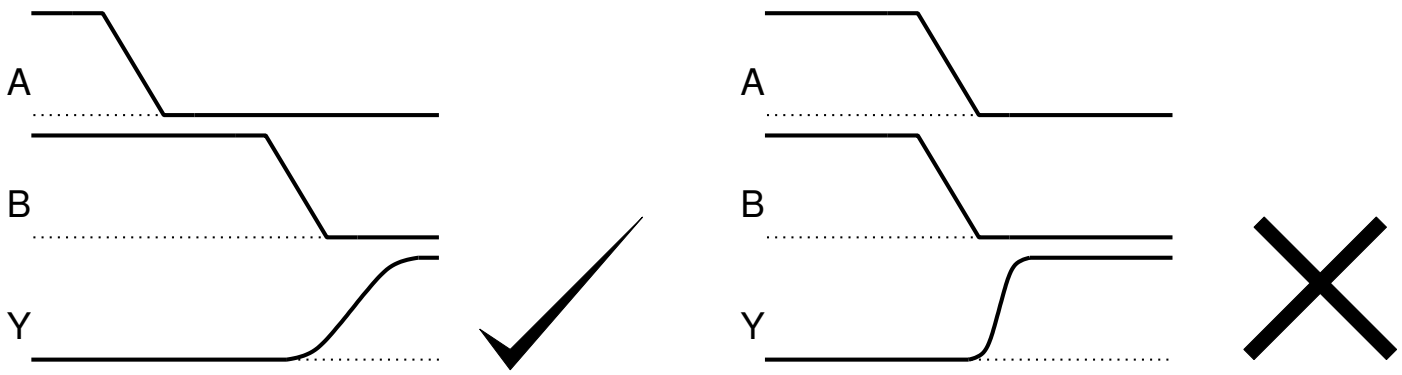


- Propagation delays are measured based on 50% of V_{DD}.
- Rise and fall times are based on 10% and 90% of V_{DD}.

Simulation Conditions

The measured performance of a gate will depend on the input drive conditions and the ouput load conditions. For useful results we must ensure realistic drive and load conditions.

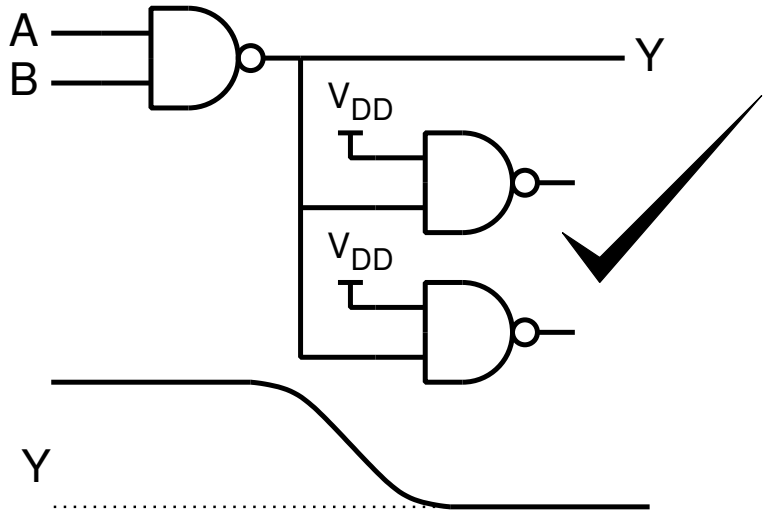
- Don't allow two inputs to change simultaneously.

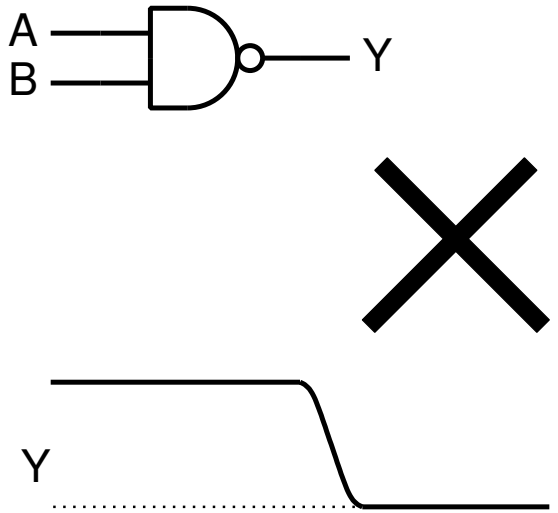


Simulation Conditions

- All simulations loaded[3]

  Load should be in proportion to the load experienced in a real circuit.



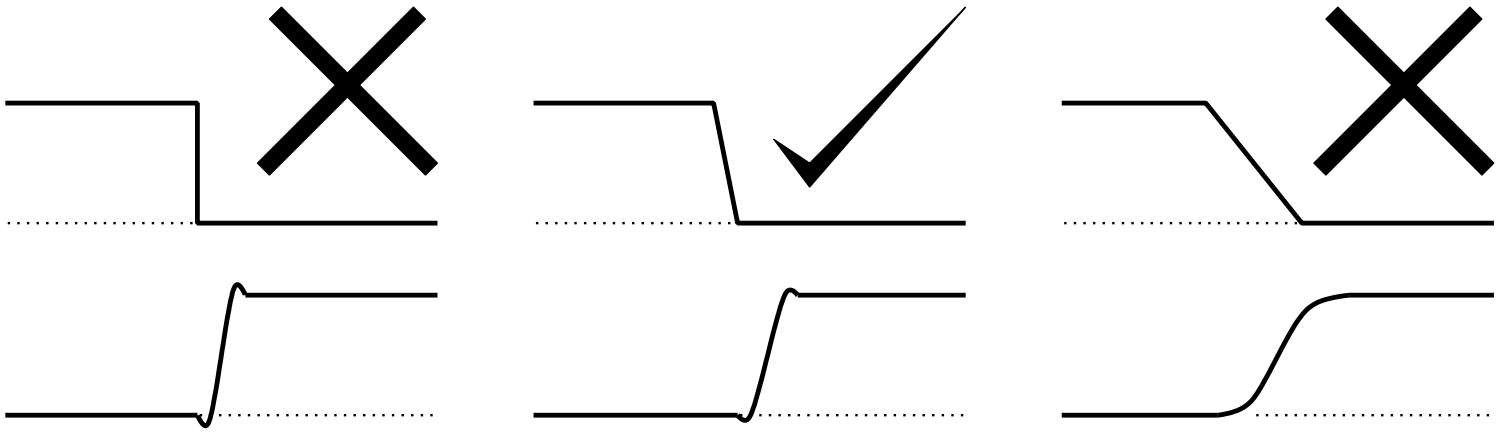


Where a NAND gate is used as the load, tie unused inputs to V_{DD}. Where a NOR gate is used as the load, tie unused inputs to GND.

[3] remember to record the results at **Y** rather than at the output of one of the load devices!

Simulation Conditions

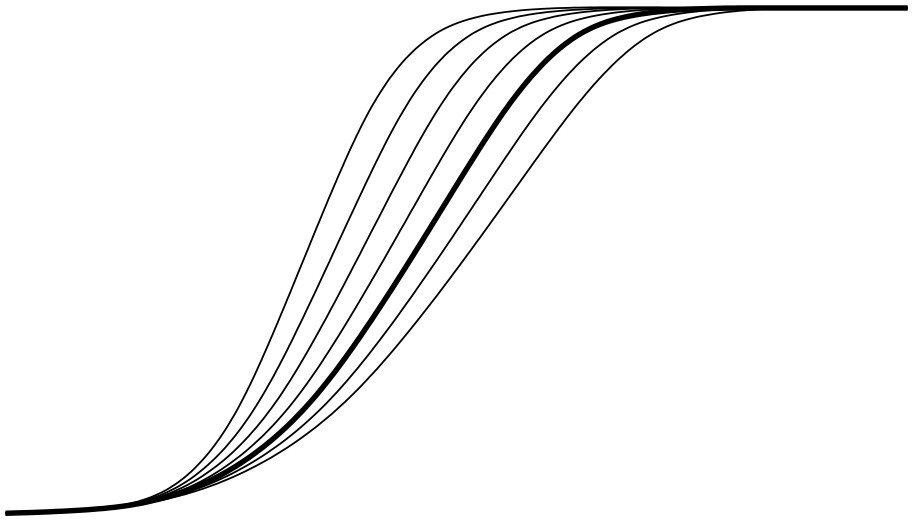
- reasonable input slopes
  - not much faster nor much slower than the resulting output slope



Advanced Simulation

HSpice's sweep facility allows you to run several different simulations in one batch and then select the simulation which gives the best results for further development. See the following web page for more information:

`https://secure.ecs.soton.ac.uk/notes/bim/notes/vlsi/assign/sweep.html`



Remember to update the Magic files and recreate the HSpice netlist before final submission.

Deliverables

- Files

  The following files must exist in your home file store before the submission process begins[4]:

  - `~/design/magic/desex1/<cellname>.mag`
  - `~/design/magic/desex1/<cellname>_ld.mag`
  - `~/design/magic/desex1/<cellname>_ld.sp`
  - `~/design/magic/desex1/<cellname>_ld.spice`

- Information

  - Transistor size information: W_N, W_P (in microns, μm)
  - Rise and Fall information: t_r, t_f (in picoseconds, ps)

- Documentation

  No documentation is required for this exercise other than an up to date log book.

[4] where <*cellname*> is `nand2`, `nand3`, `nor2` or `nor3`

Handin & Deadline

- Preparation For Handin

  Run the following script to collect together the files for handin. (This script will also prompt you for the information that you have collected.)

  ```
  prepare_vlsi desex1
  ```

  The script will create a single file

  ```
  ~/design/magic/desex1/handin.tar
  ```

  for the next stage of handin.

- Electronic Handin

  The Computer-Based Assignment Submissions System at

  ```
  https://handin.ecs.soton.ac.uk/
  ```

  will guide you through the stages required to upload the `handin.tar` file.

- The Deadline for this exercise is *16:00 on Wednesday 23rd October*.