Characterisation and Cell Library Databook

25% of the marks for the assignment will be awarded for a cell library databook which gives information about the cells.

The sort of information that we expect to see in a databook will include: *cell name, cell function, port names, propagation delays (preferably with a variety of different load capacitances), input capacitances, cell area, port positions*

The aim is use scripting[1] to generate a simple document describing the cells. Significant scripting skills are not expected and a proof of concept document (e.g. only dealing with a subset of the cells) is acceptable where scripting is employed. For teams who struggle with scripting, a hand generated document may be submitted as an alternative[2].

[1]Modern cell library databooks generate themselves. The cell designer creates a new cell and runs a script that adds another page to the databook.

[2]For all databooks, however generated, the accuracy of the presented numerical results and the consistency of the presentation is the very important (and will greatly influence the marks awarded).

Design Exercise Report

Main Body

- Title page + table of contents
- Brief introduction covering team decisions (max 2 sides)
- Design documentation for major cells (max 4 sides per designer)
- A conclusion sumarising the work done (max 1 side)

Appendices

- **A**: Team Management (max 1 side)
- **B**: Division of Labour Form (1 side)

The design exercise report provides evidence of the design, implementation and testing work that you have done and should include justifications for any important design decisions.[3]

[3]Since I will be reading your report in order to judge the quality of your work, you will need to do good work and write it up well in order to get a good mark.

Design Exercise Report

- Design documentation for major cells:

  `rdtype, smux2, smux3, fulladder, leftbuf, halfadder, xor2`[4]

  A sub-section should exist for each designer (max 4 sides), dealing with the major cells they have designed. This will cover one or two major cells and any work done on the merged cells: `scandtype` and `scanreg`.

  For each major cell, justification should be given for important design decisions. To support the text, the following information should be provided:[5]

  – transistor level circuit diagram
    with comments on derivation if appropriate
  – stick diagram
  – details of testing carried out

[4] only teams of five should provide documentation for the `halfadder` and `xor2` gates

[5] take care with diagrams, don't scan/capture my schematics, avoid screen capture of simulation and layout if possible, and avoid using inappropriate pre-defined circuit symbols (e.g. MOS transistors with visible substrate connection).

Design Exercise Report

- Presentation
  - Use full sentences and paragraphs
  - Further advice on report writing can be found on the module homepage.

- Editing
  - The page limits will require you to make decisions such as *what to take out and what to leave in?* or *how big should a figure be so that it is clear and easy to read but not so big that there is no room for the text to explain it?*

    If you leave the report to the last minute, you will not have time to consider these decisions properly.

Submission – Documentation

The following documentation files should be submitted via the ECS Handin system:

- The auto-generated cell library databook should be submitted as a simple .txt or .html file (if no script has been created, a PDF version of the databook may be submitted instead).
- The script used to generate the databook (if one was used) should also be submitted.
- A README.txt should be submitted which explains how to use the script and what it does (or, if there is no script, this file will tell us that).
- The design exercise report should be submitted as a PDF file.

Deadline for documentation is 16:00 on Wednesday 4th December.