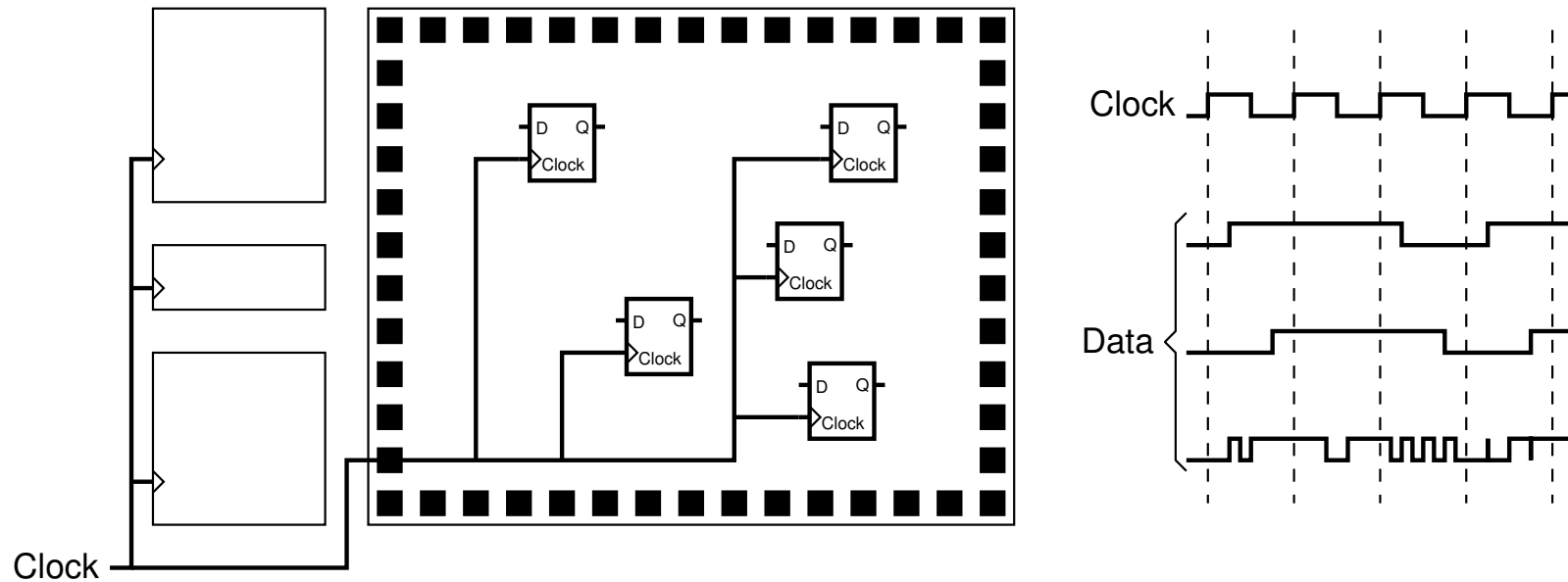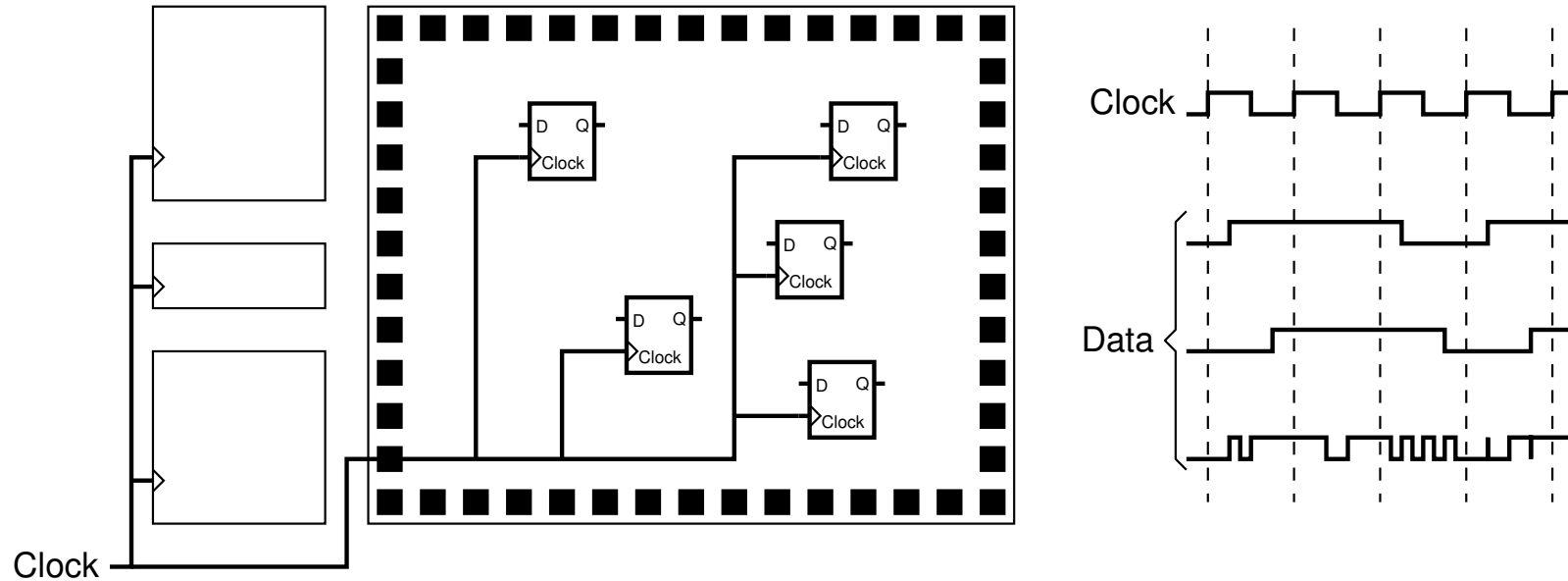# Synchronous Systems

- All parts of the system share the same clock   .

- The data may change between active clock transitions but must be stable by the time the next active transition occurs[1].

---

[1]for most systems the *active transition* is the rising edge of the clock

20001

Synchronous Systems

- All parts of the system share the same clock and the same clock edge sensitivity.

- The data may change between active clock transitions but must be stable by the time the next active transition occurs[1].

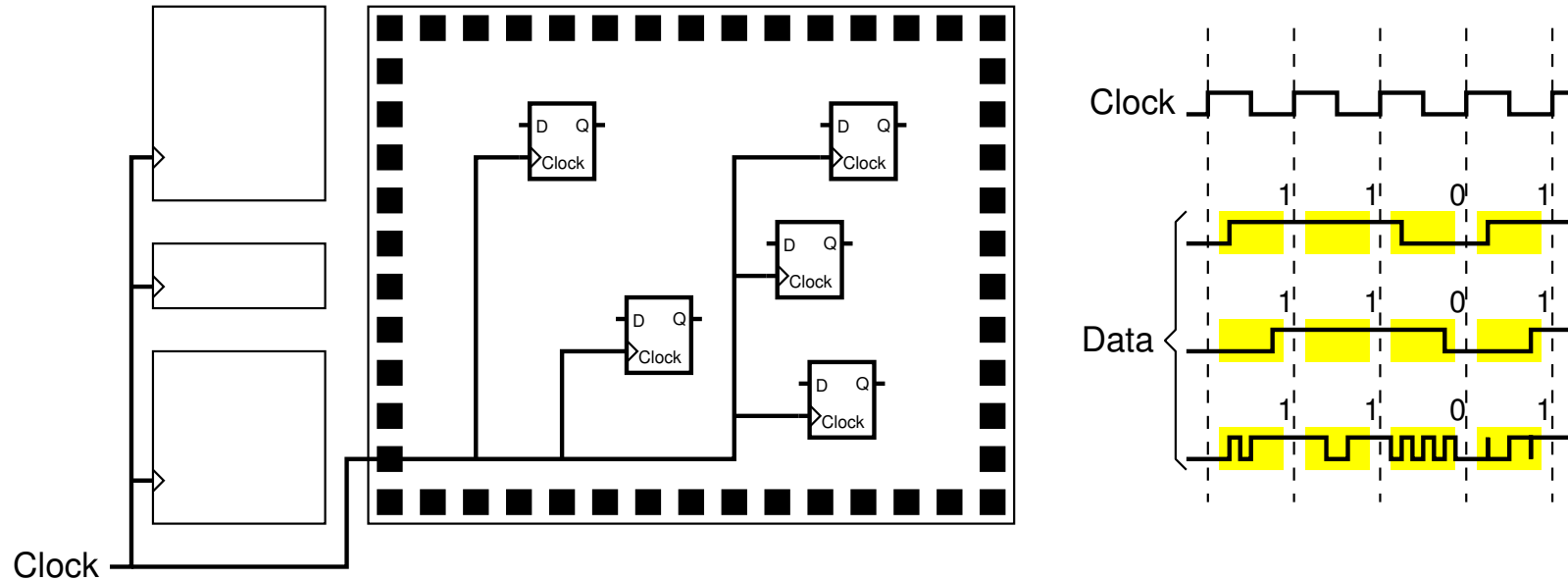[1]for most systems the *active transition* is the rising edge of the clock
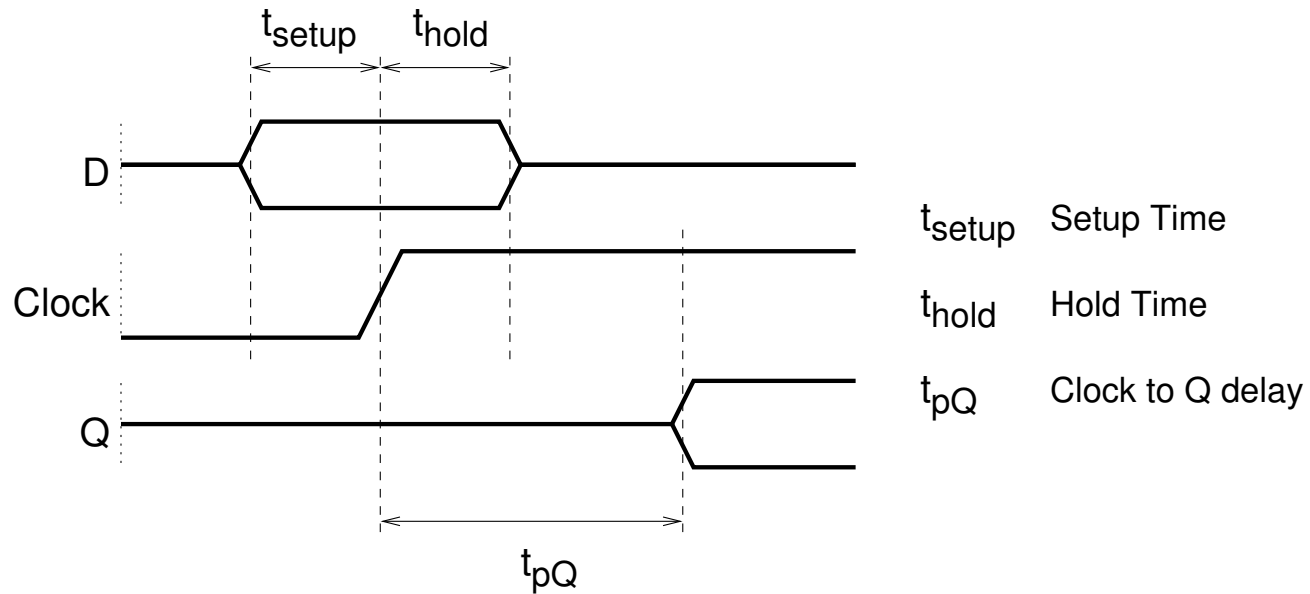
20001

Synchronous Systems

- All parts of the system share the same clock and the same clock edge sensitivity.

- The data may change between active clock transitions but must be stable by the time the next active transition occurs[1].

---

[1]for most systems the *active transition* is the rising edge of the clock

Synchronous Systems - D-type Timing

- Valid data should be present on D input for at least t_{setup} before the active clock edge and at least t_{hold} after the clock edge.

- The minimum D-type cycle time will be limited by the sum $t_{setup} + t_{pQ}$.

20002

Synchronous Systems - Static Timing Analysis (Ideal Clock)
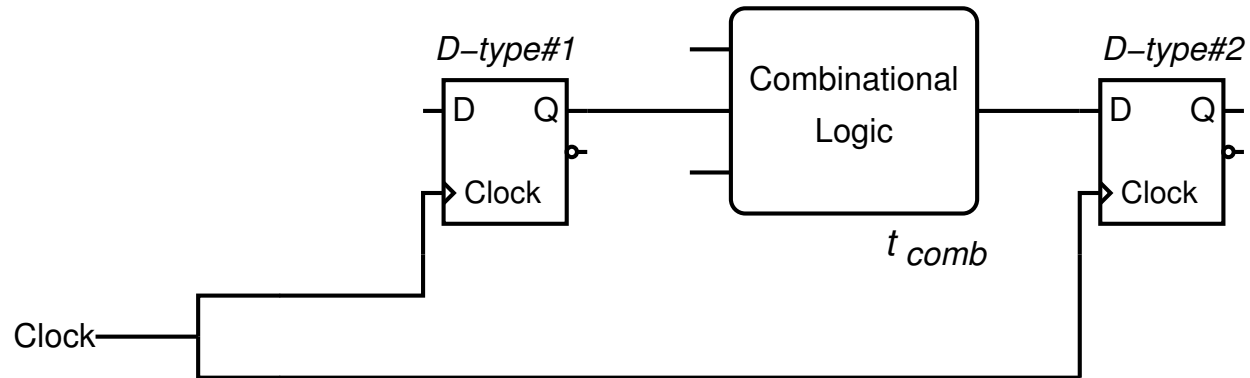
- To avoid a setup violation:

$$ClockPeriod > t_{pQ} + t_{comb} + t_{setup}$$

- To avoid a hold violation:

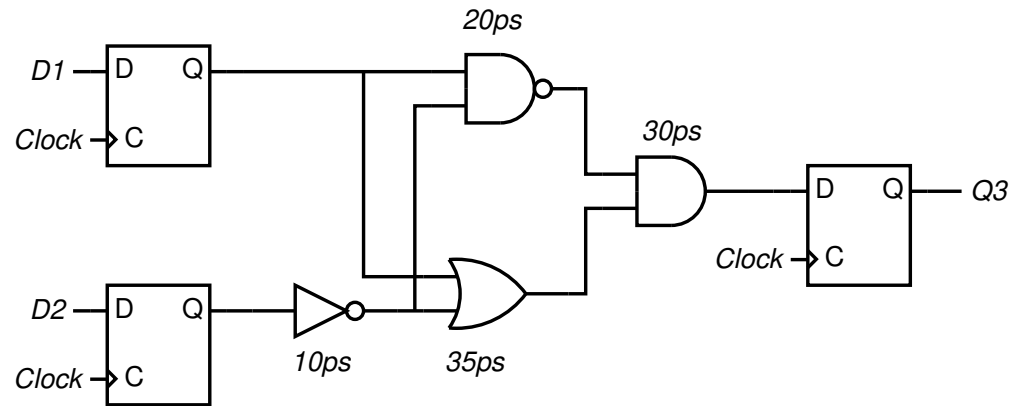$$t_{pQ} + t_{comb} > t_{hold}$$

20003

Static Timing Analysis

- Predicts the timing of a circuit without simulation[2]

- Analysis of gate network based on:

  - Propagation delays
  - Set-up and hold times for storage elements
  - Constraints such as desired operating freqency and the timing of inputs and outputs

Note that the examples given here are simplified in that they reduce the propagation delay through a gate to a single number - in reality there are predictable and unpredicatble variations in gate delays which must be accounted for by static timing analysis tools.

---

[2]timing simulations for large digital systems are slow and will usually not catch all edge and coner cases

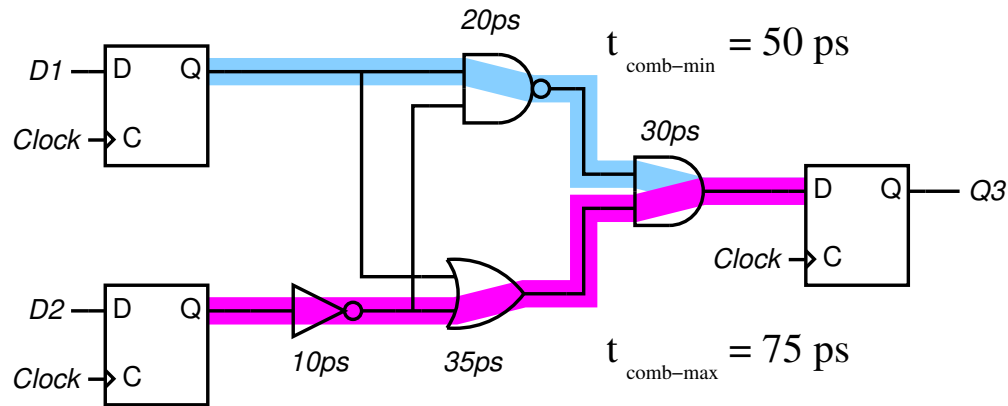# Synchronous Systems - Static Timing Analysis (Ideal Clock)

- To avoid a setup violation:

$$ClockPeriod > t_{pQ} + t_{comb-max} + t_{setup}$$

- To avoid a hold violation:

$$t_{pQ} + t_{comb-min} > t_{hold}$$

20005

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20005

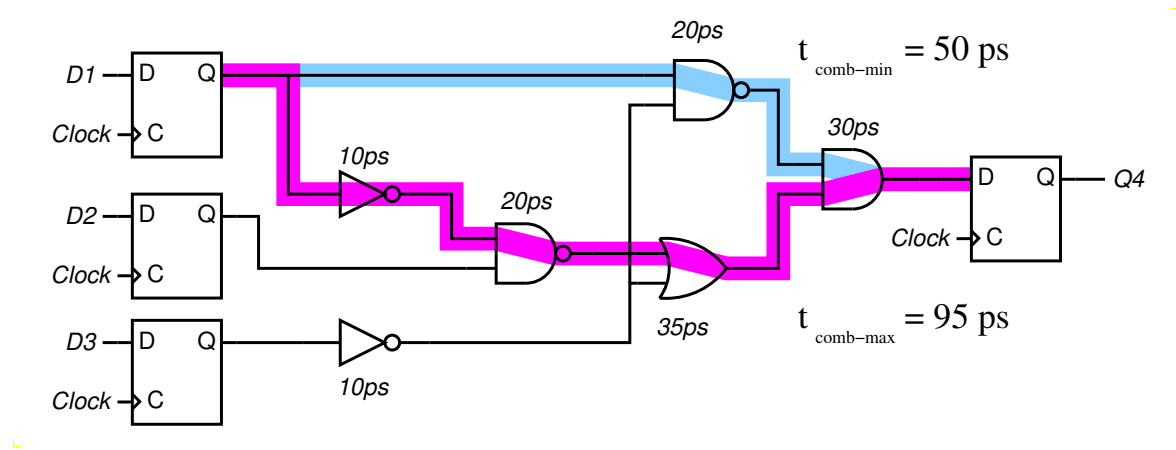# Synchronous Systems - Static Timing Analysis (Ideal Clock)
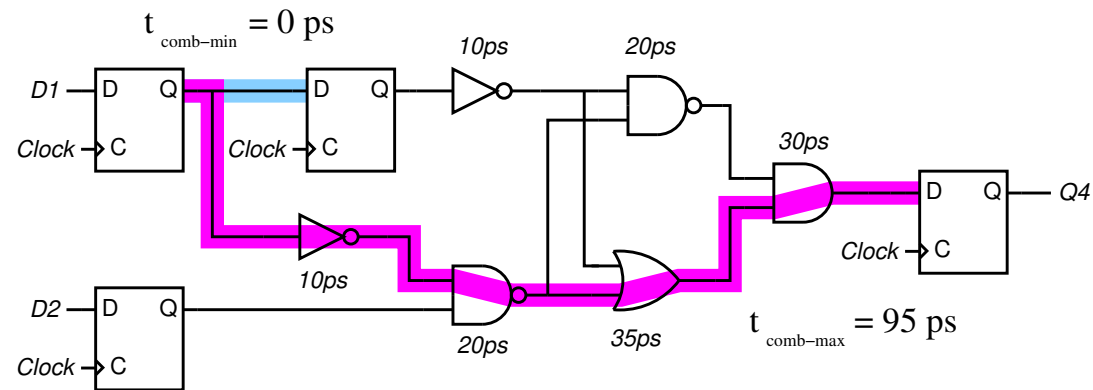

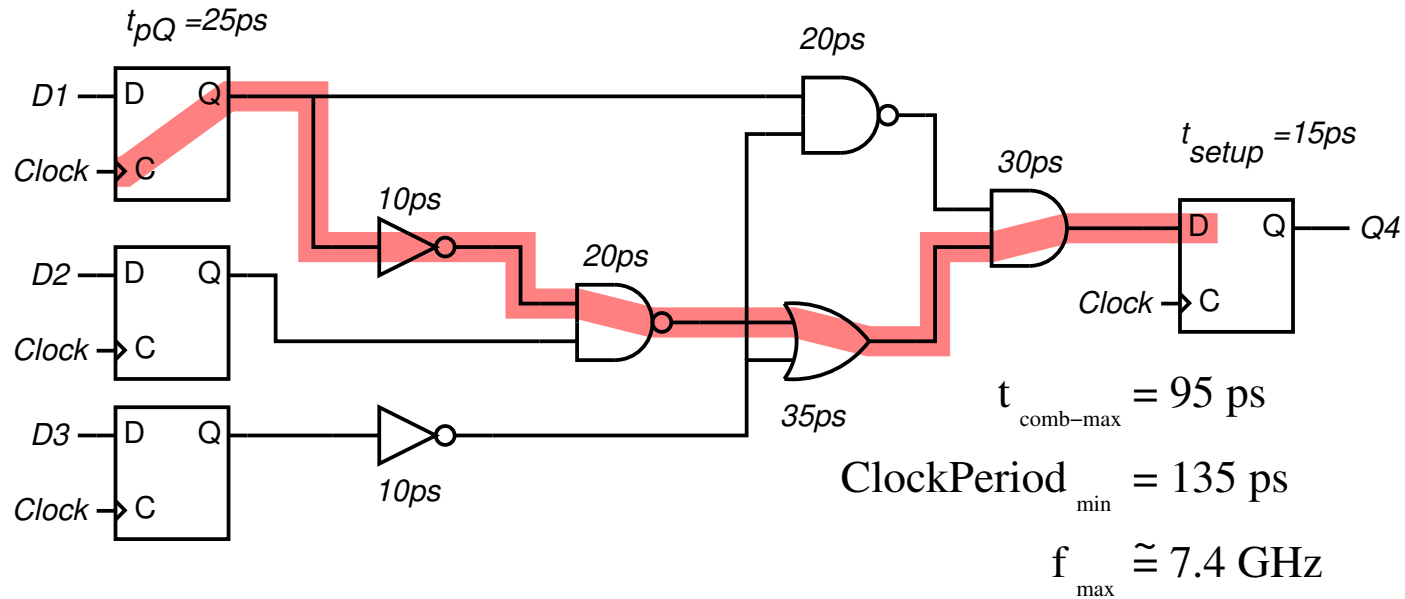- To avoid a setup violation:

$$ClockPeriod > t_{pQ} + t_{comb-max} + t_{setup}$$

- To avoid a hold violation:

$$t_{pQ} + t_{comb-min} > t_{hold}$$

20005

Synchronous Systems - Static Timing Analysis (Ideal Clock)

$t_{pQ} =25ps$

D1

20ps

Clock C

$t_{setup} =15ps$

10ps

30ps

D2

20ps

D Q — Q4

Clock C

Clock C

D3

35ps

$t_{comb-max}$ = 95 ps

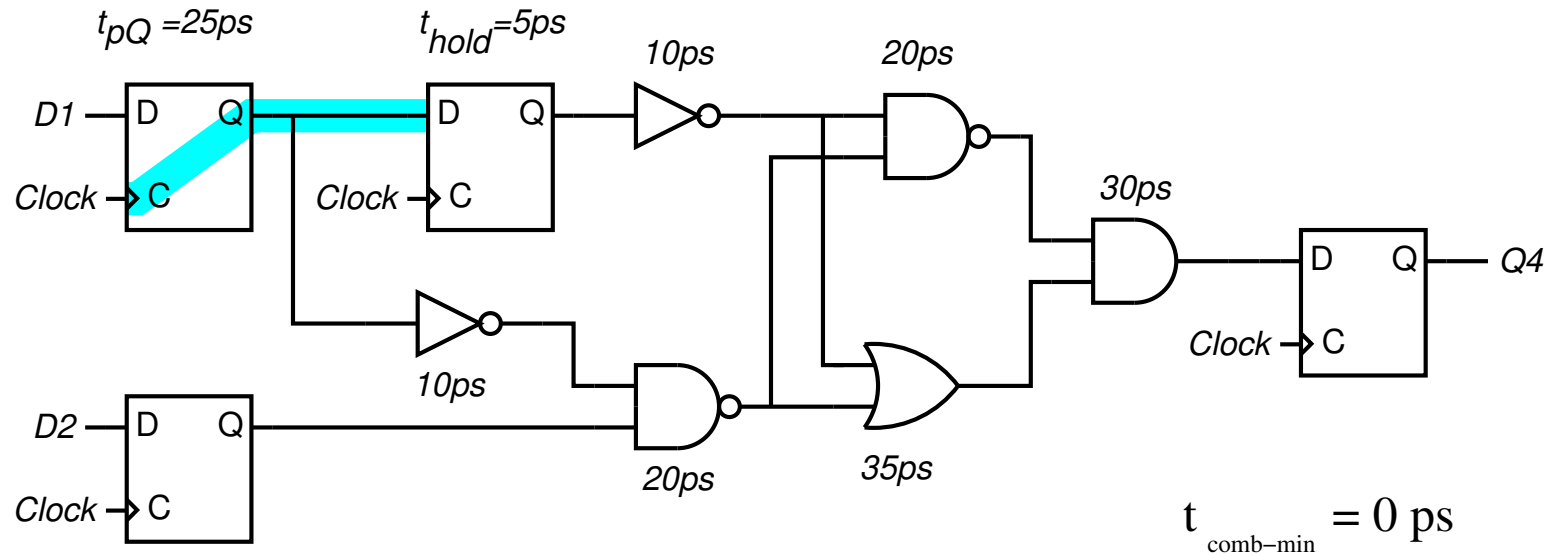10ps

$ClockPeriod_{min}$ = 135 ps

$f_{max} \cong 7.4$ GHz

- Critcal path analysis allows us to determine the maximum feasible clock frequency:

$$ClockPeriod > t_{pQ} + t_{comb-max} + t_{setup}$$

$$f_{max} = \frac{1}{t_{pQ} + t_{comb-max} + t_{setup}}$$
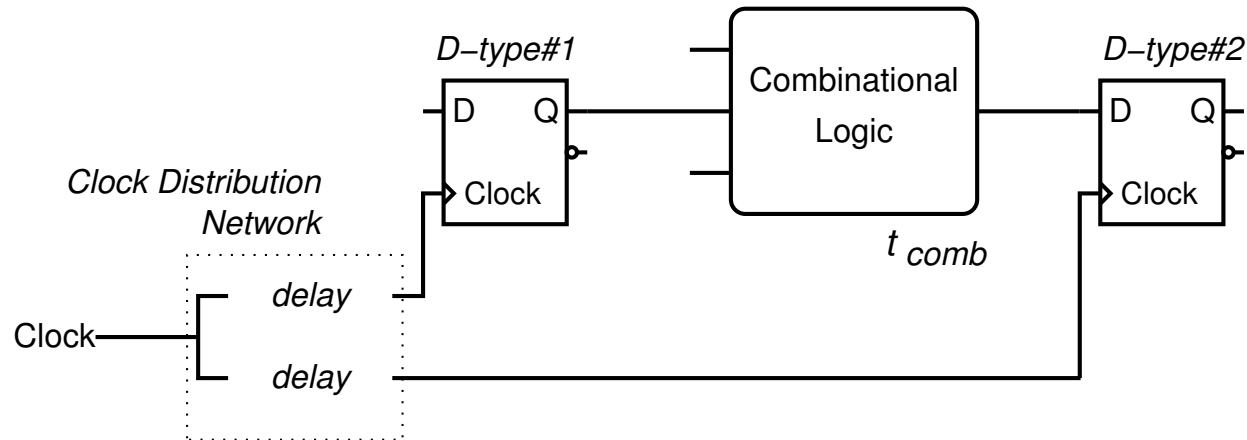
20006

Synchronous Systems - Static Timing Analysis (Ideal Clock)

$$t_{pQ} + t_{comb-min} > t_{hold}$$

If we have an ideal clock and $t_{pQ} > t_{hold}$ we won't see hold violations even with if $t_{comb-min} = 0$.

20007

Synchronous Systems - Clock Skew

- Clock Distribution

  The process of distributing clocks from a central source gives rise to delays.

  Clock skew is the difference between the arrival times of the clock at different points in the circuit.

- Clock Skew may cause unexpected timing violations

  Hold: if *D-type #1* clocks first, D input of *D-type #2* may change too early[3]

  Setup: if *D-type #1* clocks second, D input of *D-type #2* may change too late

  ---
  [3]most likely where combinational logic is minimal or absent

Synchronous Systems - Clock Skew

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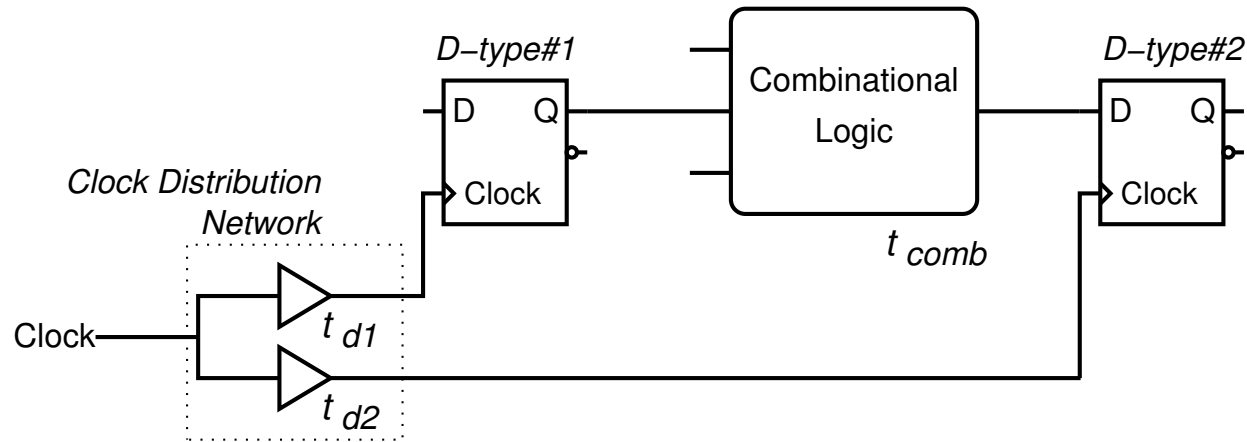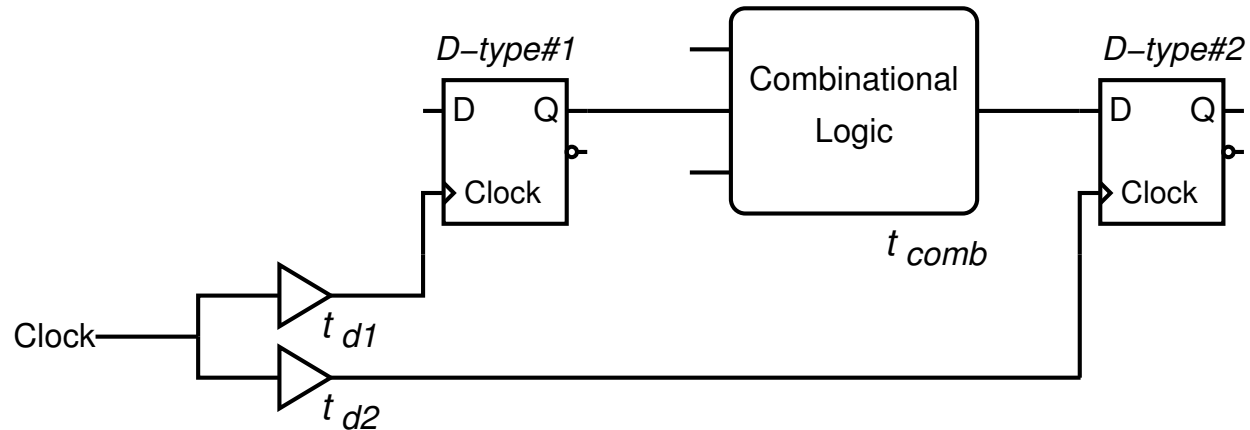
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---

[3]most likely where combinational logic is minimal or absent

Synchronous Systems - Static Timing Analysis (inc. clock skew)

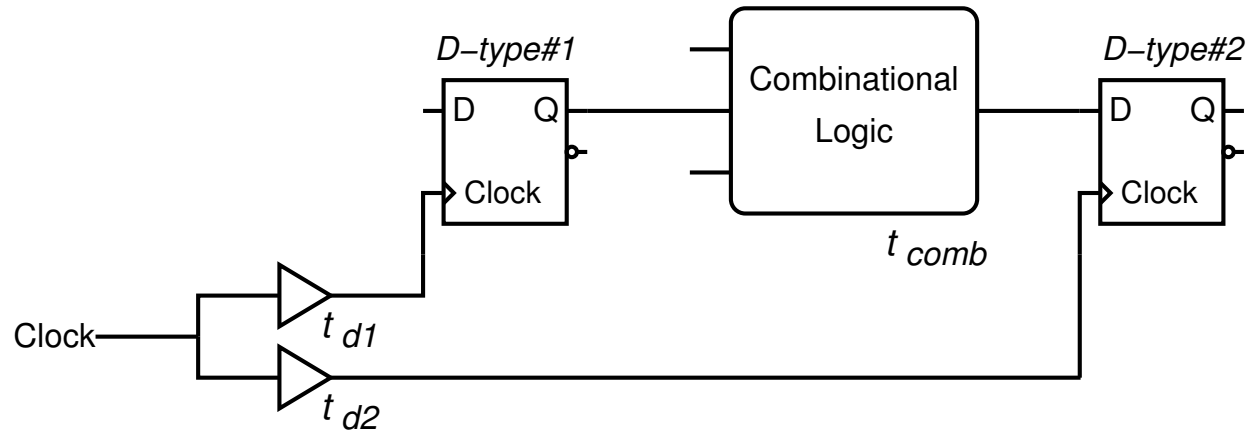

- To avoid a setup violation:

$$ClockPeriod + t_{d2} > t_{pQ} + t_{comb} + t_{setup} + t_{d1}$$

- To avoid a hold violation:

$$t_{pQ} + t_{comb} + t_{d1} > t_{hold} + t_{d2}$$

20009

Synchronous Systems - Static Timing Analysis (inc. clock skew)
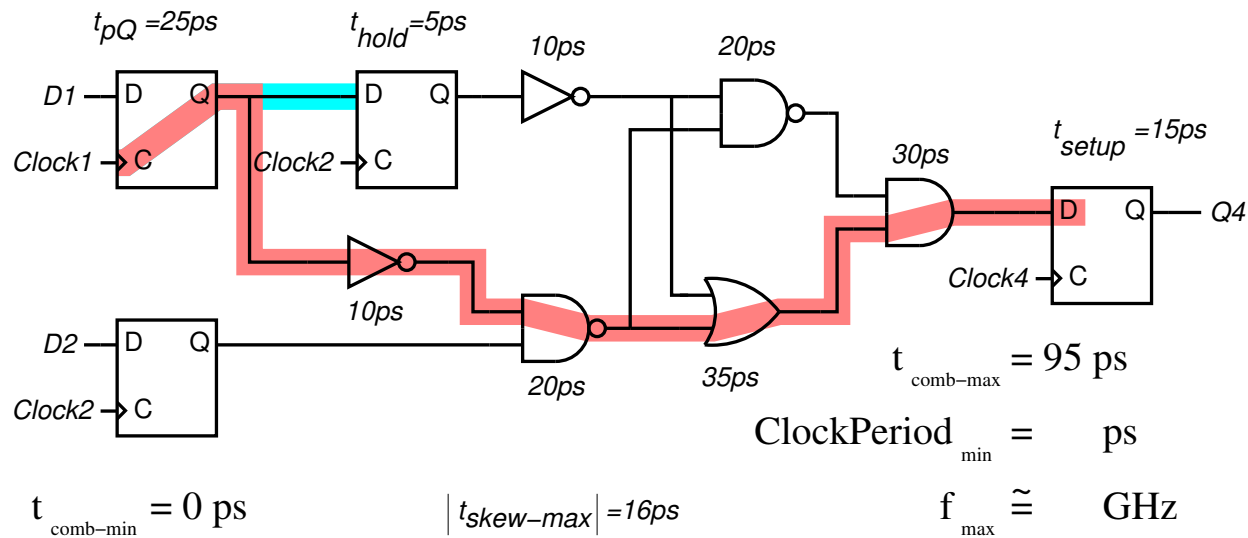

- To avoid a setup violation:

$$ClockPeriod > t_{pQ} + t_{comb} + t_{setup} + (t_{d1} - t_{d2})$$

- To avoid a hold violation:

$$t_{pQ} + t_{comb} > t_{hold} + (t_{d2} - t_{d1})$$

20009

Synchronous Systems - Static Timing Analysis (inc. clock skew)

$t_{pQ} = 25ps$ $t_{hold} = 5ps$ 10ps   20ps

D1 — D   Q

Clock1 → C   Clock2 → C

$t_{setup} = 15ps$

30ps

D   Q — Q4

Clock4 → C

10ps

D2 — D   Q

Clock2 → C

20ps   35ps $t_{comb-max} = 95$ ps

$\text{ClockPeriod}_{min} = \quad ps$

$t_{comb-min} = 0$ ps $|t_{skew-max}| = 16ps$ $f_{max} \cong \quad GHz$

- What is the maximum operating frequency of the circuit if the clock skew is no more than 16ps?
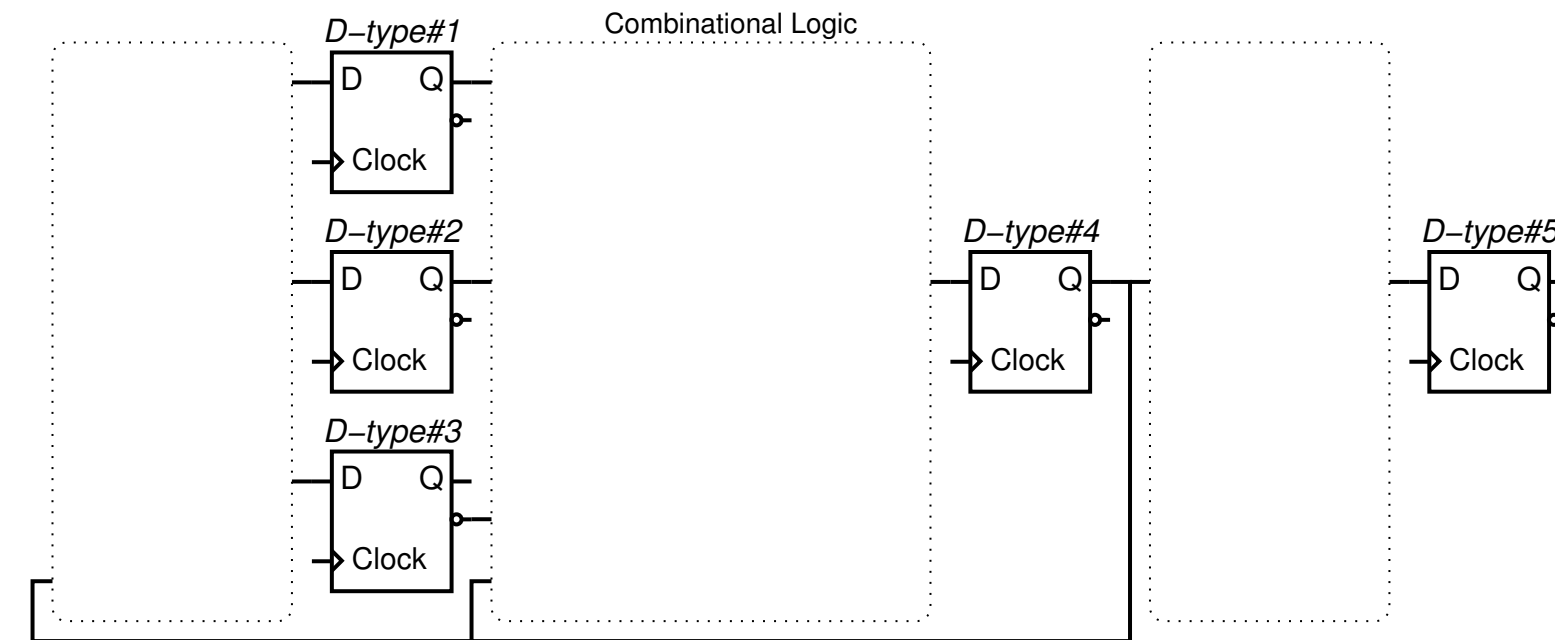
$$ClockPeriod > t_{pQ} + t_{comb} + t_{setup} + t_{skew}$$

- What is the maximum clock skew that can be tolerated before we have a hold violation?

$$t_{pQ} + t_{comb} > t_{hold} + t_{skew}$$

20010

Synchronous Systems - Static Timing Analysis (inc. clock skew)

Critical Path

D–type#1

D   Q

Clock

Combinational Logic

D–type#2

D   Q

Clock

D–type#4

D   Q

Clock

D–type#5

D   Q

Clock
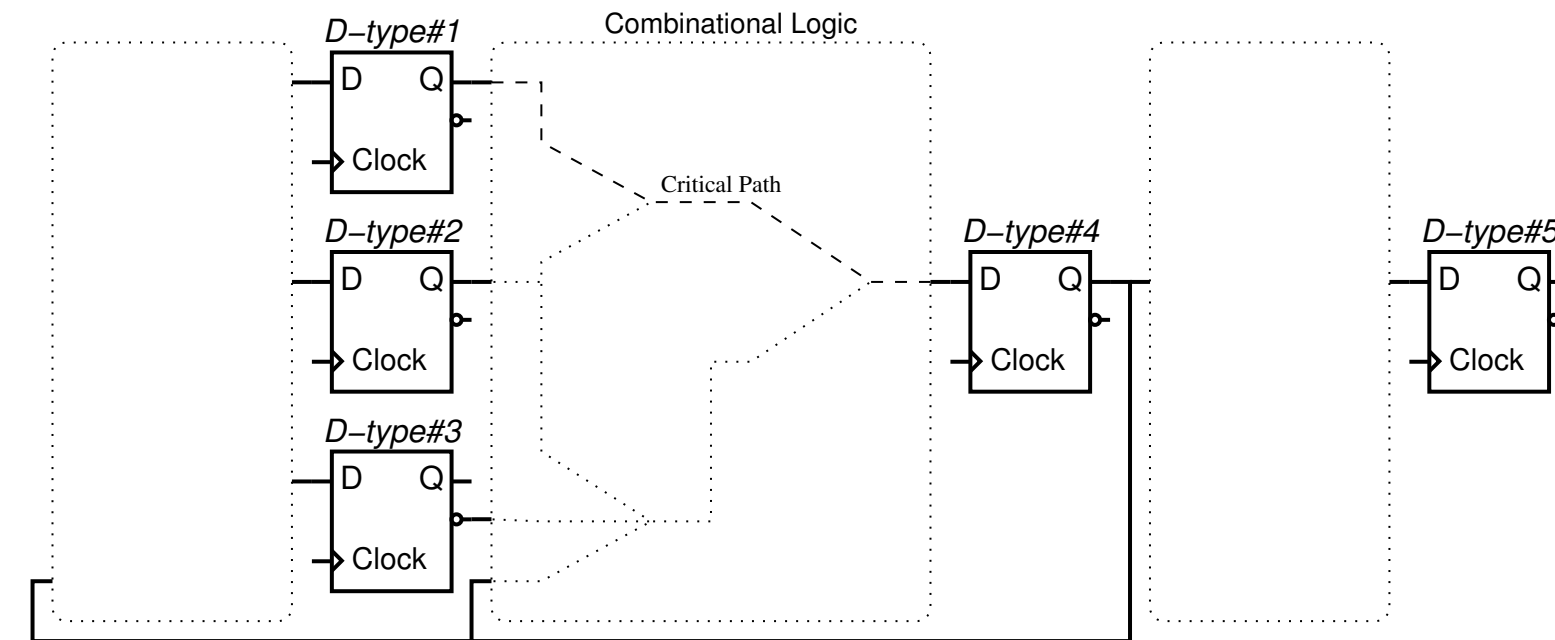
D–type#3

D   Q

Clock

- To avoid a setup violation:

$$ClockPeriod > t_{pQ} + t_{critical\_path} + t_{setup} + t_{skew}$$

20011

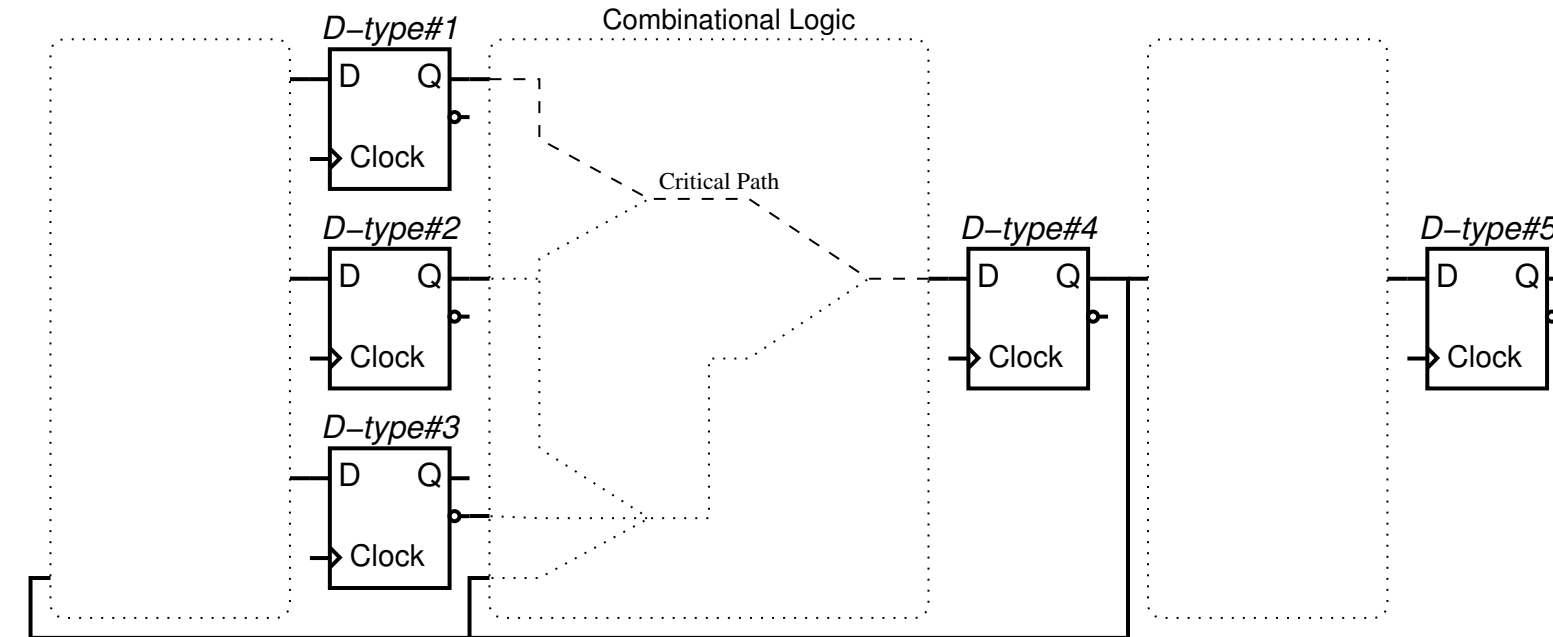# Synchronous Systems - Static Timing Analysis (inc. clock skew)

Critical Path

- To avoid a setup violation:

$$ClockPeriod > t_{pQ} + t_{critical\_path} + t_{setup} + (t_{d1} - t_{d4})$$
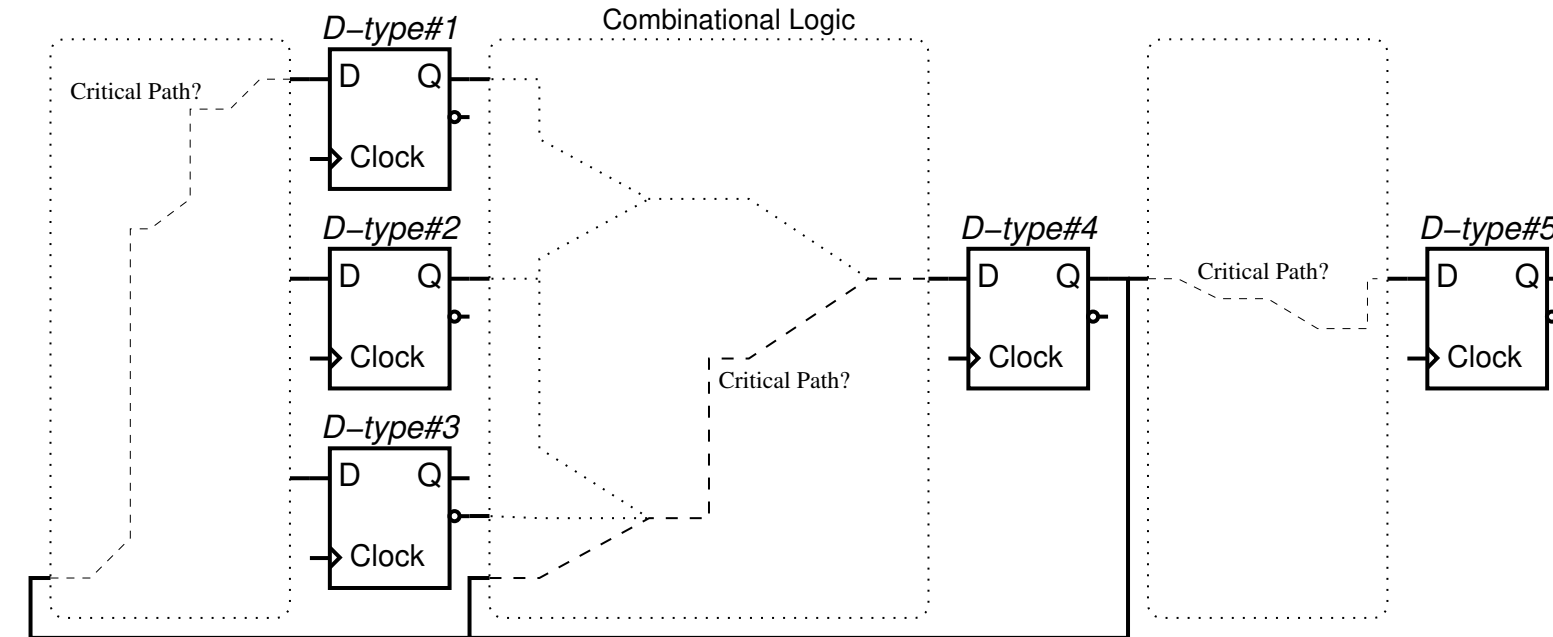
20012

Critical Path

$$ClockPeriod > t_{pQ} + t_{critical\_path} + t_{setup} + (t_{d1} - t_{d4})$$

- If we can control the skew (e.g. by increasing t_{d4}), we can ease the timing constraint.[4]

---

[4]this may result in the critical path moving to another part of the circuit
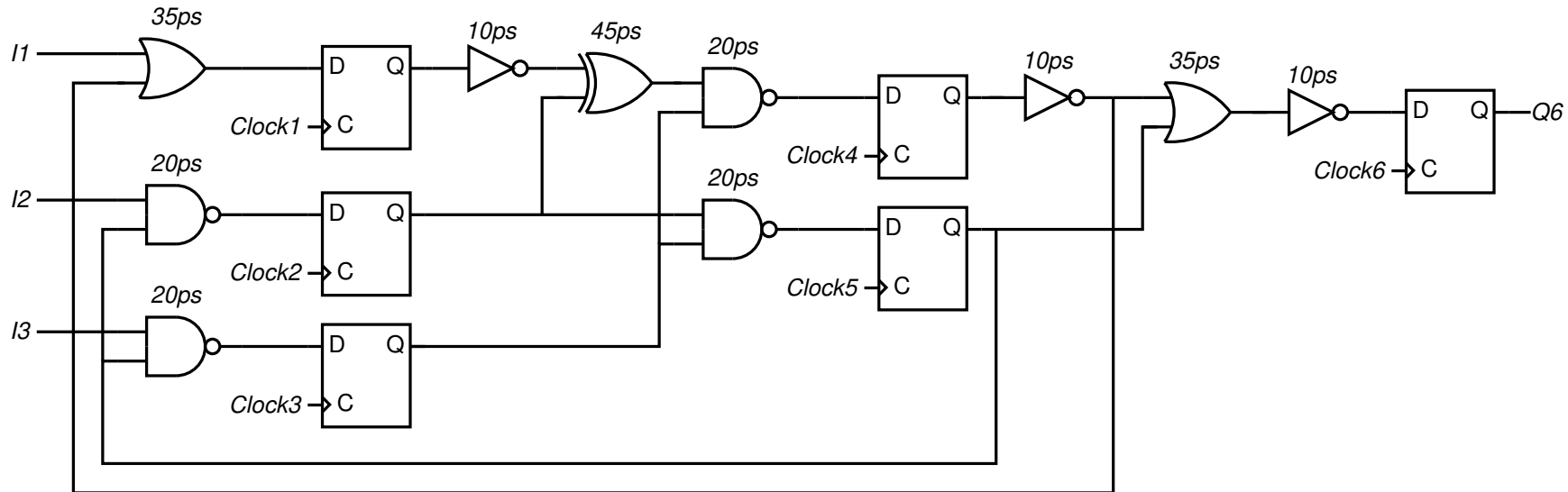
20013

Critical Path

$$ClockPeriod > t_{pQ} + t_{critical\_path} + t_{setup} + (t_{d_{launch}} - t_{d_{capture}})$$

- If we can control the skew (e.g. by increasing t_{d4}), we can ease the timing constraint.[4]

---

[4]this may result in the critical path moving to another part of the circuit

Synchronous Systems - Static Timing Analysis (inc. clock skew)
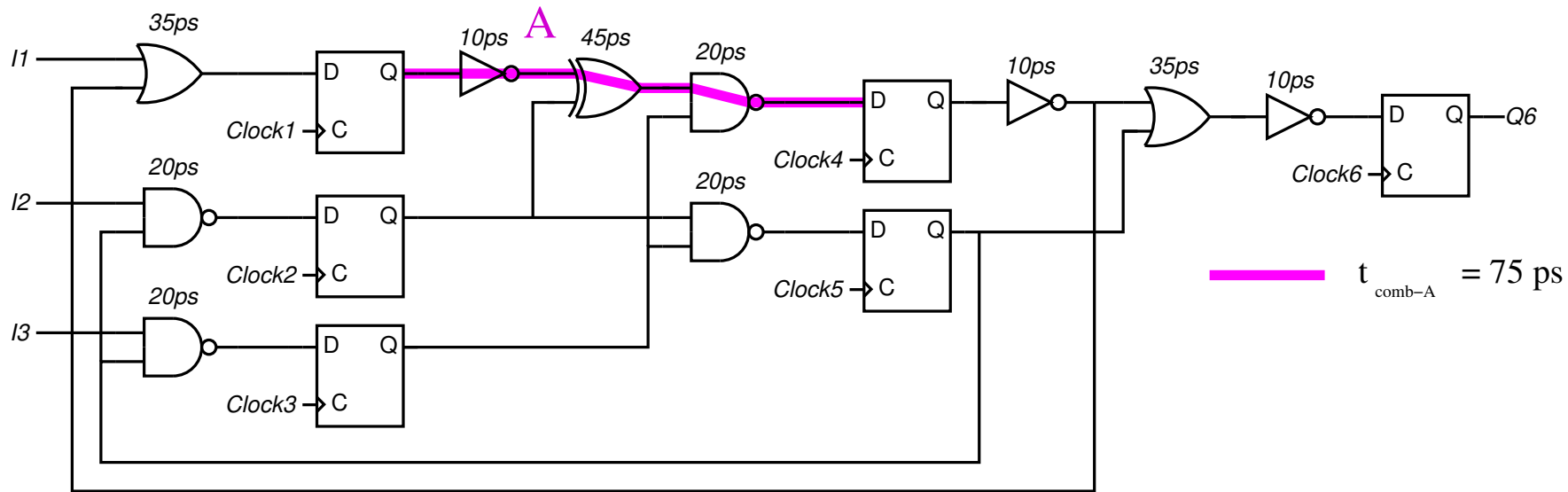

• Calculate f_{max} in the presence of intentional clock skew.

20014

Synchronous Systems - Static Timing Analysis (inc. clock skew)

- Calculate f_{max} in the presence of intentional clock skew.

- Suggest suitable values for t_{d1}, t_{d2}, t_{d3}, t_{d4}, t_{d5}, t_{d6}

20015

Synchronous Systems - Static Timing Analysis (inc. clock skew)

- Calculate f_{max} in the presence of intentional clock skew.

- Suggest suitable values for t_{d1}, t_{d2}, t_{d3}, t_{d4}, t_{d5}, t_{d6}

$\Rightarrow$ Identify longest combinational paths

20016

Synchronous Systems - Static Timing Analysis (inc. clock skew)

- Calculate f_{max} in the presence of intentional clock skew.
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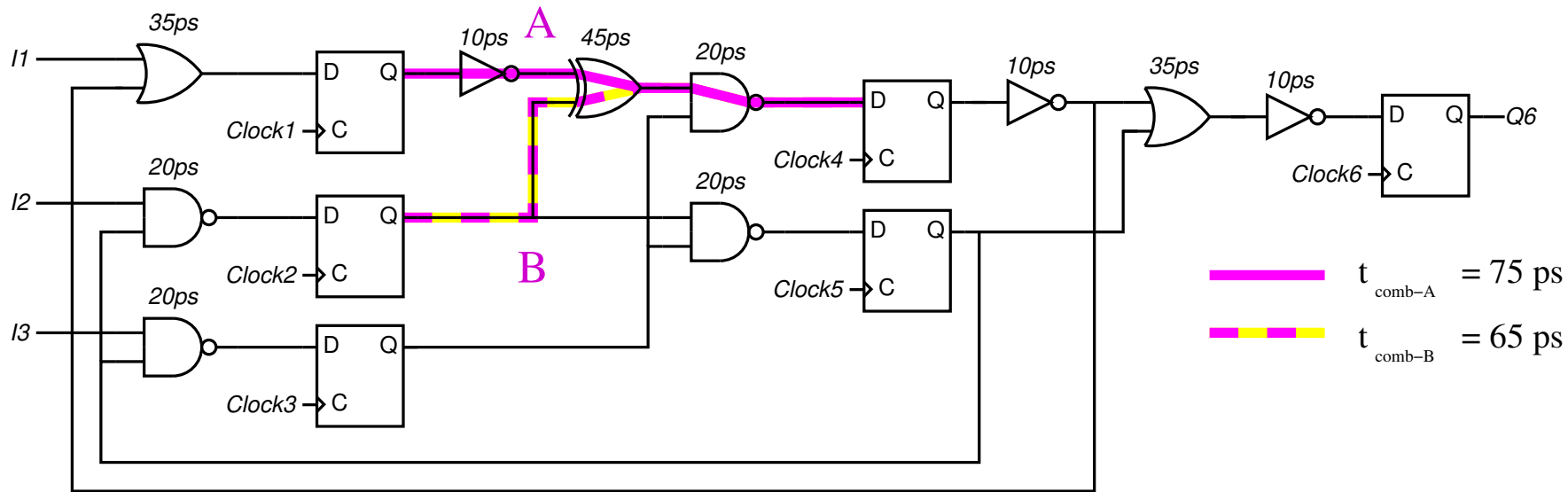$\Rightarrow$ Identify longest combinational paths
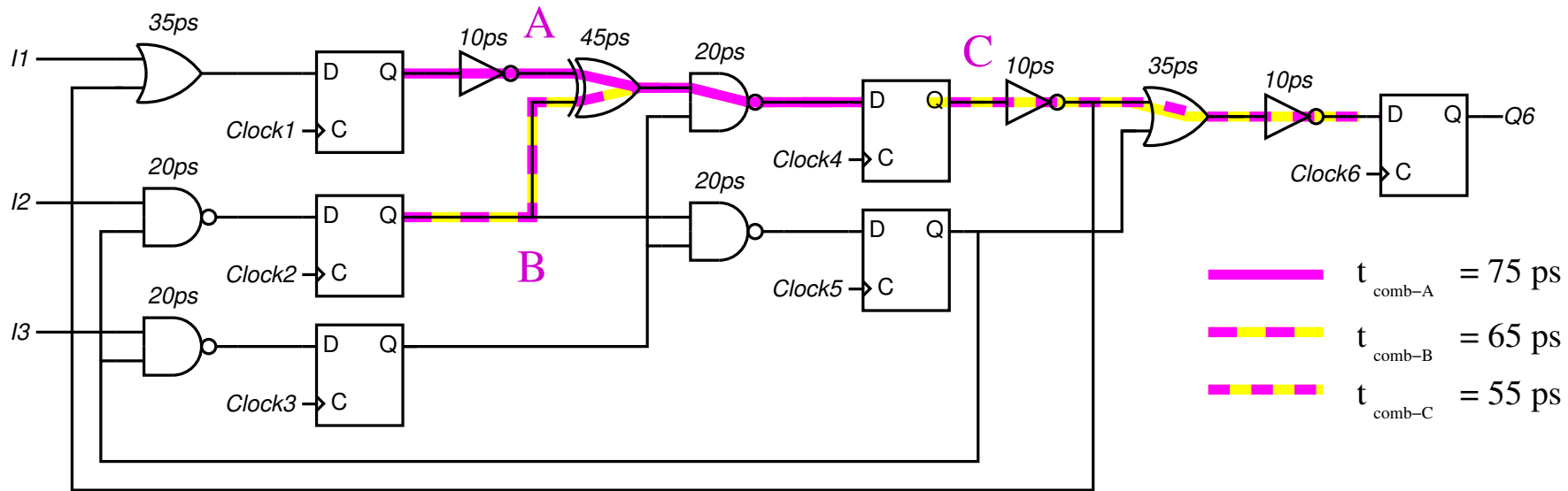
20016

Synchronous Systems - Static Timing Analysis (inc. clock skew)

- Calculate f_{max} in the presence of intentional clock skew.

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20016

Synchronous Systems - Static Timing Analysis (inc. clock skew)

35ps

I1

10ps   A   45ps   20ps   C   10ps   35ps   10ps

D   Q

Clock1 → C

20ps

I2

D   Q

Clock2 → C   B

20ps

I3

D   Q

Clock3 → C

20ps

Clock4 → C   D

D   Q

Clock5 → C

D   Q

Clock6 → C

D   Q — Q6

t_{comb-A} = 75 ps

t_{comb-B} = 65 ps

t_{comb-C} = 55 ps

t_{comb-D} = 45 ps

- Calculate f_{max} in the presence of intentional clock skew.

- Suggest suitable values for t_{d1}, t_{d2}, t_{d3}, t_{d4}, t_{d5}, t_{d6}

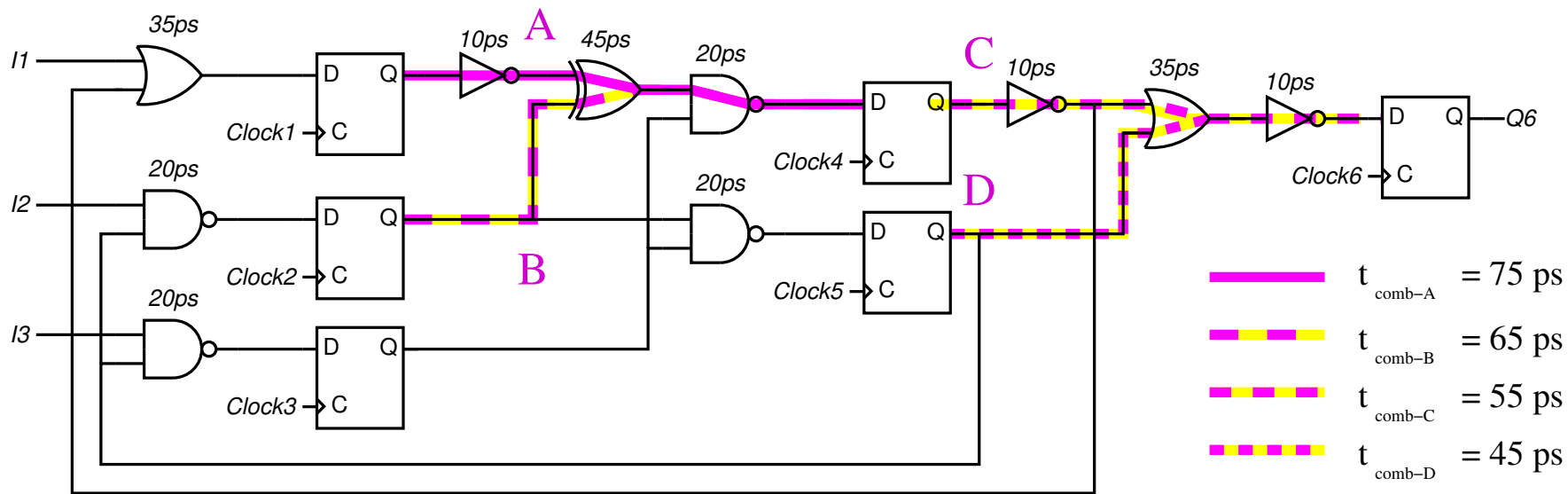$\Rightarrow$ Identify longest combinational paths

20016

Synchronous Systems - Static Timing Analysis (inc. clock skew)

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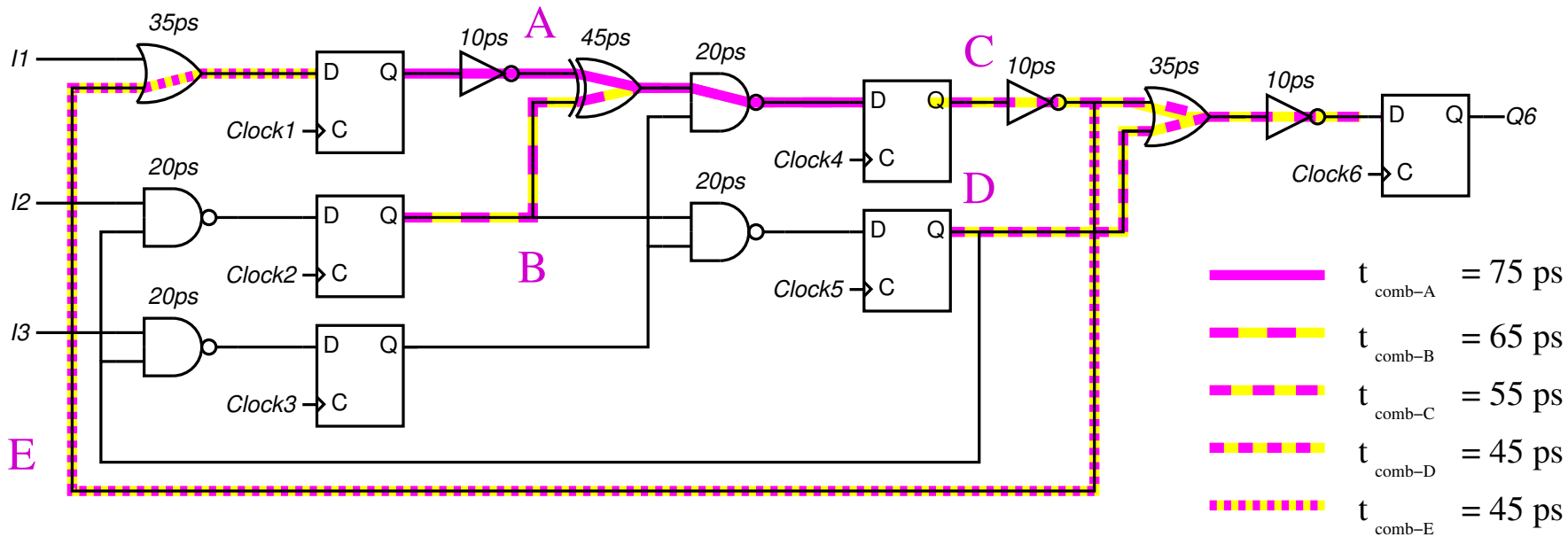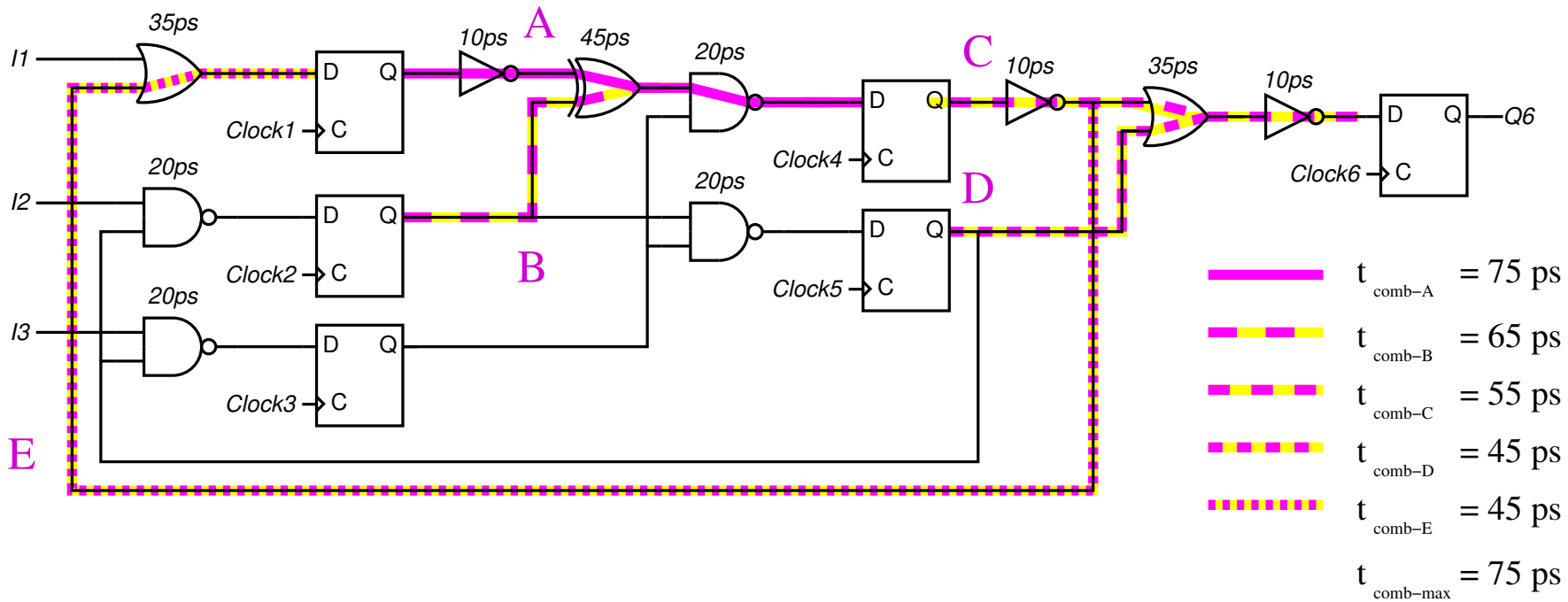$\Rightarrow$ Identify longest combinational paths
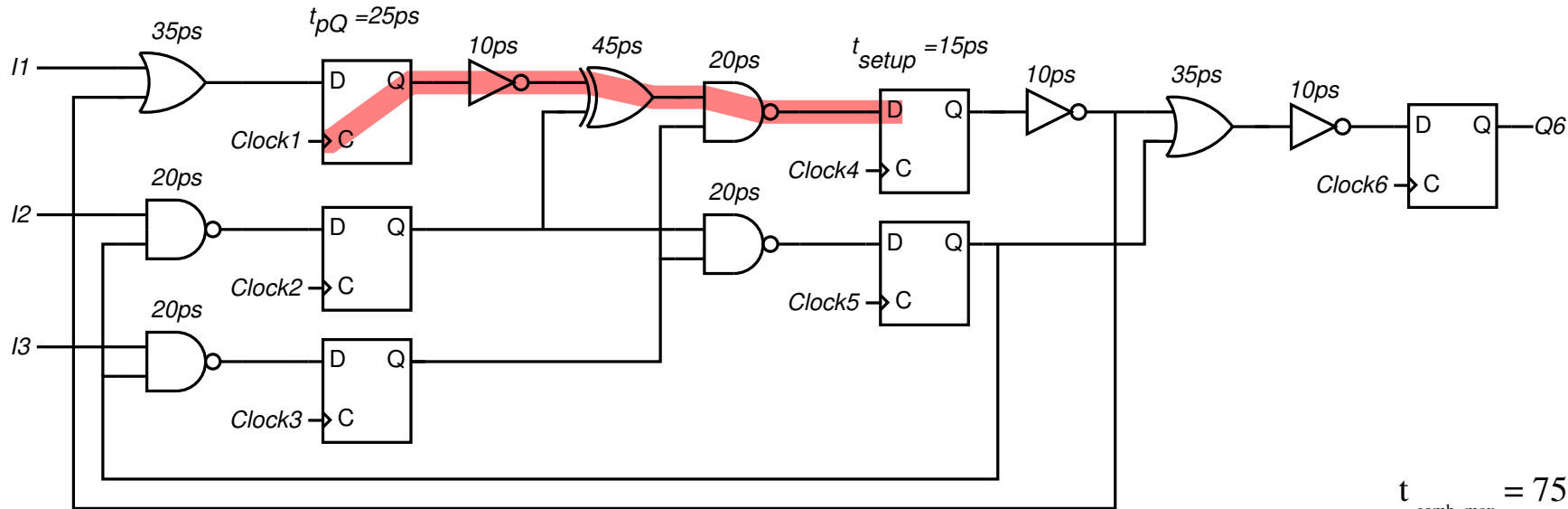
20016

Synchronous Systems - Static Timing Analysis (inc. clock skew)

- Calculate f_{max} in the presence of intentional clock skew.
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20016

Synchronous Systems - Static Timing Analysis (inc. clock skew)

$t_{comb-max}$ = 75 ps

$ClockPeriod_{min}$ = 115 ps

$f_{max} \cong 8.7$ GHz

$$ClockPeriod > t_{pQ} + t_{comb-max} + t_{setup} + (t_{d1} - t_{d4})$$

$$f_{max} = \frac{1}{t_{pQ} + t_{comb-max} + t_{setup} + (t_{d1} - t_{d4})}$$

20017

Synchronous Systems - Static Timing Analysis (inc. clock skew)

$t_{pQ} = 25ps$

$t_{setup} = 15ps$

35ps 10ps 45ps 20ps 10ps 35ps 10ps

20ps 20ps

20ps

t_{d1} t_{d2} t_{d3} t_{d4} t_{d5} t_{d6}

Clock

$t_{d1} = 50 \text{ ps}$ $t_{d2} = 50 \text{ ps}$

$t_{d3} = 50 \text{ ps}$ $t_{d4} = 50 \text{ ps}$

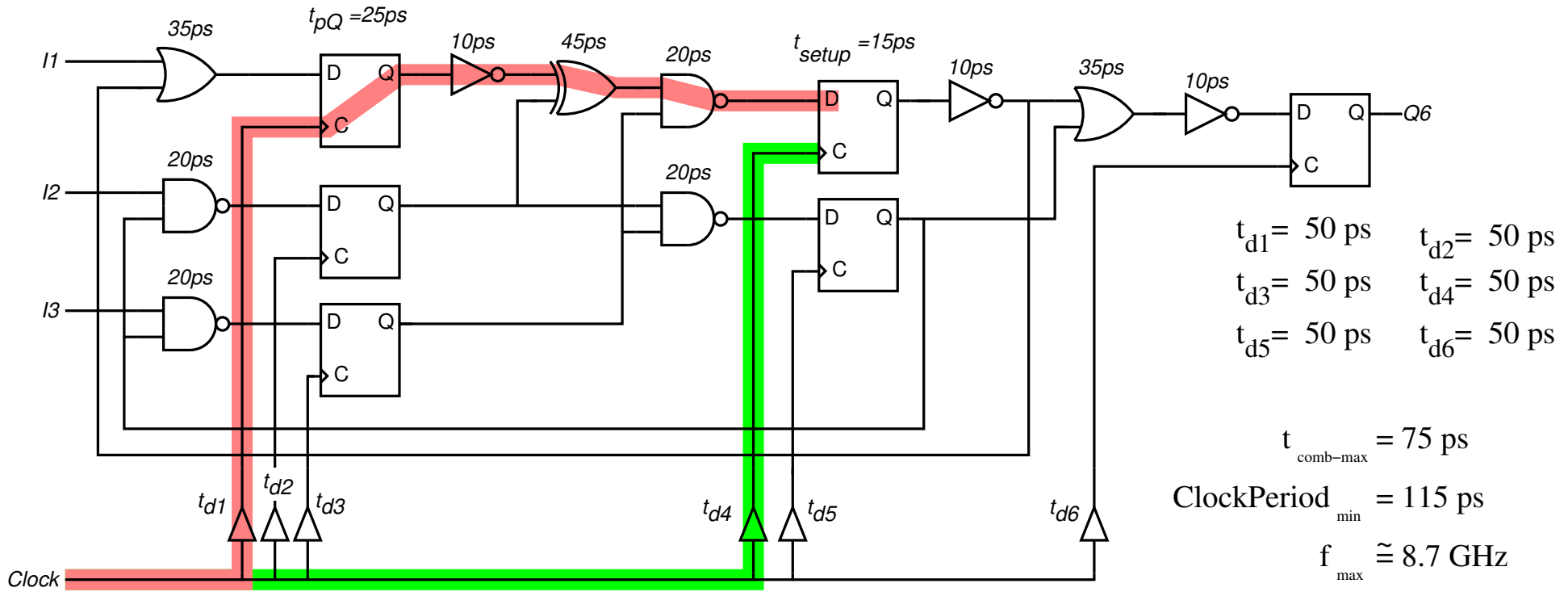$t_{d5} = 50 \text{ ps}$ $t_{d6} = 50 \text{ ps}$

$t_{comb-max} = 75 \text{ ps}$

$\text{ClockPeriod}_{min} = 115 \text{ ps}$

$f_{max} \cong 8.7 \text{ GHz}$

$$ClockPeriod > t_{pQ} + t_{comb-max} + t_{setup} + (t_{d1} - t_{d4})$$

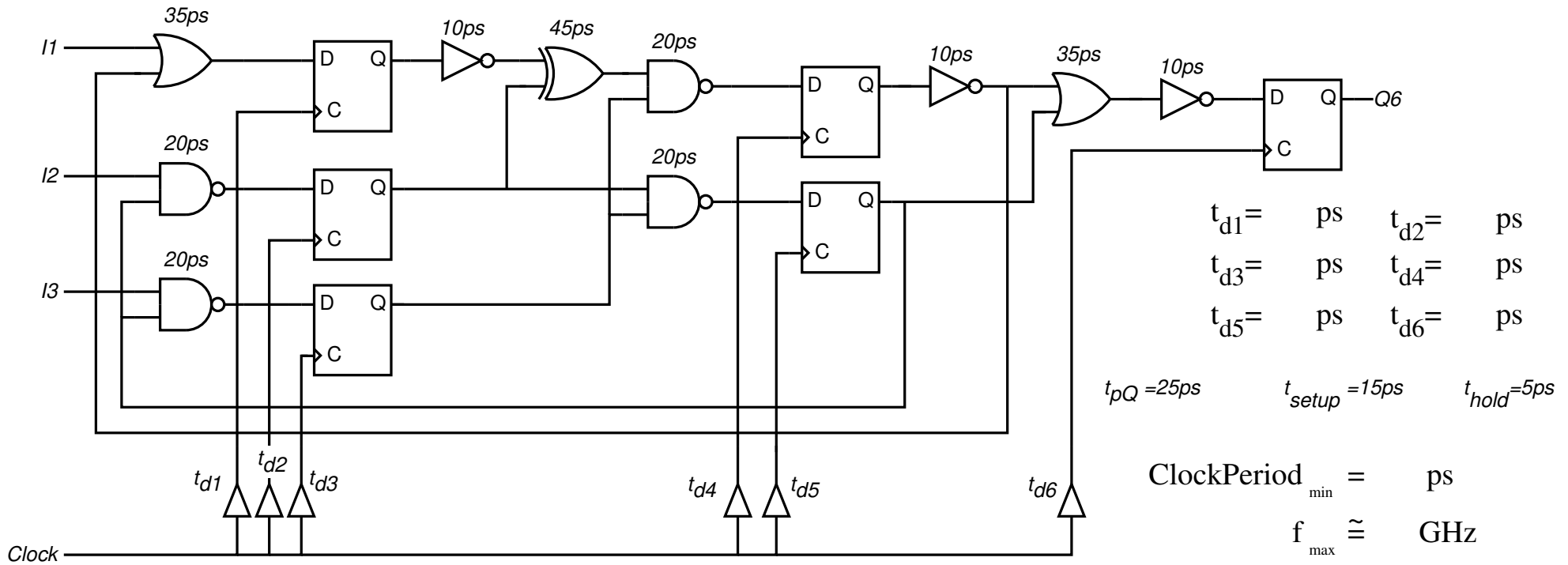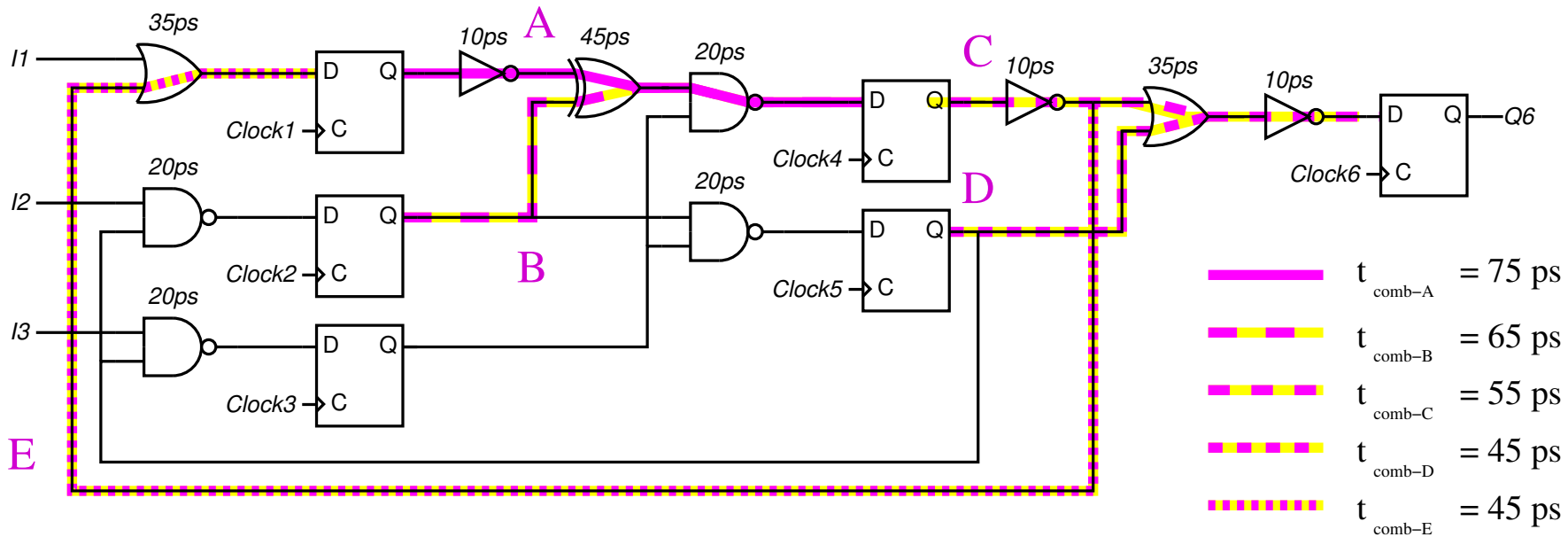$$f_{max} = \frac{1}{t_{pQ} + t_{comb-max} + t_{setup} + (t_{d1} - t_{d4})}$$

20018

Synchronous Systems - Static Timing Analysis (inc. clock skew)

$t_{d1}=$ ps $t_{d2}=$ ps

$t_{d3}=$ ps $t_{d4}=$ ps

$t_{d5}=$ ps $t_{d6}=$ ps

$t_{pQ}=25ps$ $t_{setup}=15ps$ $t_{hold}=5ps$

$ClockPeriod_{min} = $ ps

$f_{max} \cong $ GHz

$$ClockPeriod > t_{pQ} + t_{comb-crit} + t_{setup} + \left(t_{d_{launch}} - t_{d_{capture}}\right)$$
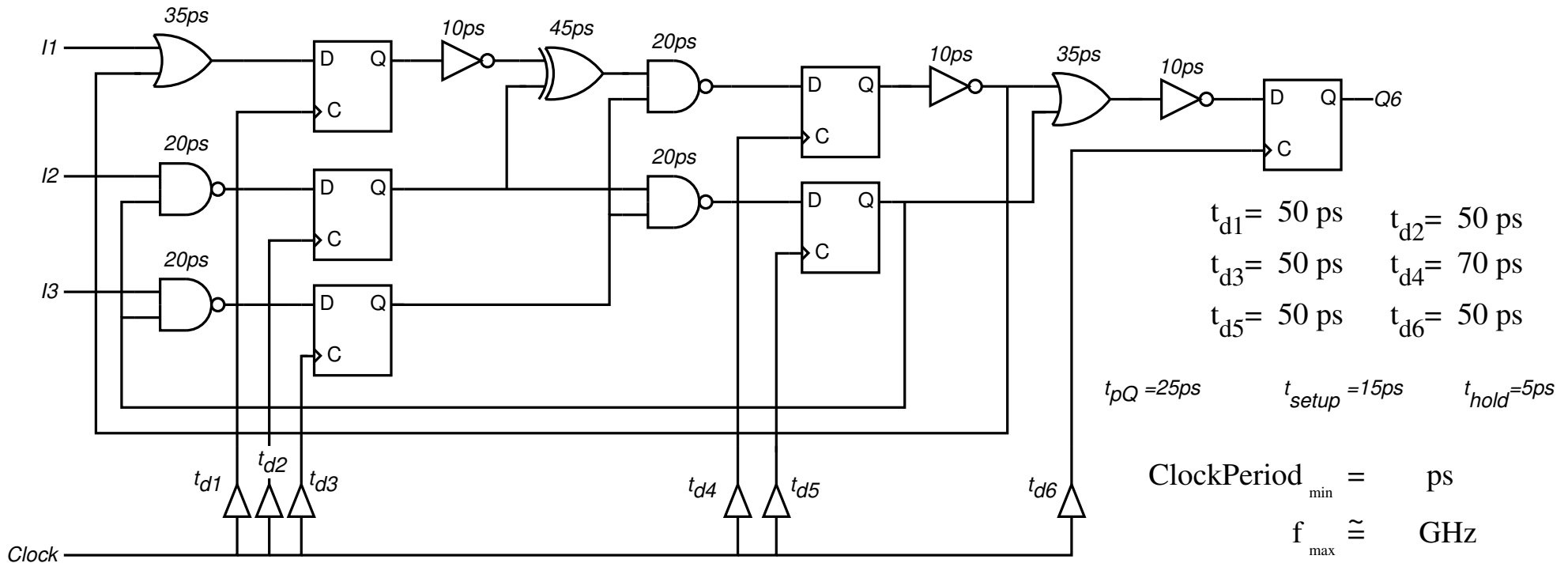
$$f_{max} = \frac{1}{t_{pQ} + t_{comb-crit} + t_{setup} + \left(t_{d_{launch}} - t_{d_{capture}}\right)}$$

20019

Synchronous Systems - Static Timing Analysis (inc. clock skew)

$\Rightarrow$ Initially try increasing t_{d4} by 20ps

20020

Synchronous Systems - Static Timing Analysis (inc. clock skew)

t_{d1} = 50 ps t_{d2} = 50 ps

t_{d3} = 50 ps t_{d4} = 70 ps

t_{d5} = 50 ps t_{d6} = 50 ps

t_{pQ} = 25ps t_{setup} = 15ps t_{hold} = 5ps

ClockPeriod$_{min}$ =   ps

f$_{max}$ $\cong$ GHz

$$ClockPeriod > t_{pQ} + t_{comb-crit} + t_{setup} + (t_{d_{launch}} - t_{d_{capture}})$$

$$f_{max} = \frac{1}{t_{pQ} + t_{comb-crit} + t_{setup} + (t_{d_{launch}} - t_{d_{capture}})}$$

20021

Synchronous Systems - Static Timing Analysis (inc. clock skew)

$t_{d1}=$ ps $t_{d2}=$ ps

$t_{d3}=$ ps $t_{d4}=$ ps

$t_{d5}=$ ps $t_{d6}=$ ps

$t_{pQ} =25ps$ $t_{setup} =15ps$ $t_{hold}=5ps$

$ClockPeriod_{min} =$ ps

$f_{max} \cong$ GHz

$$ClockPeriod > t_{pQ} + t_{comb-crit} + t_{setup} + \left(t_{d_{launch}} - t_{d_{capture}}\right)$$

$$f_{max} = \frac{1}{t_{pQ} + t_{comb-crit} + t_{setup} + \left(t_{d_{launch}} - t_{d_{capture}}\right)}$$
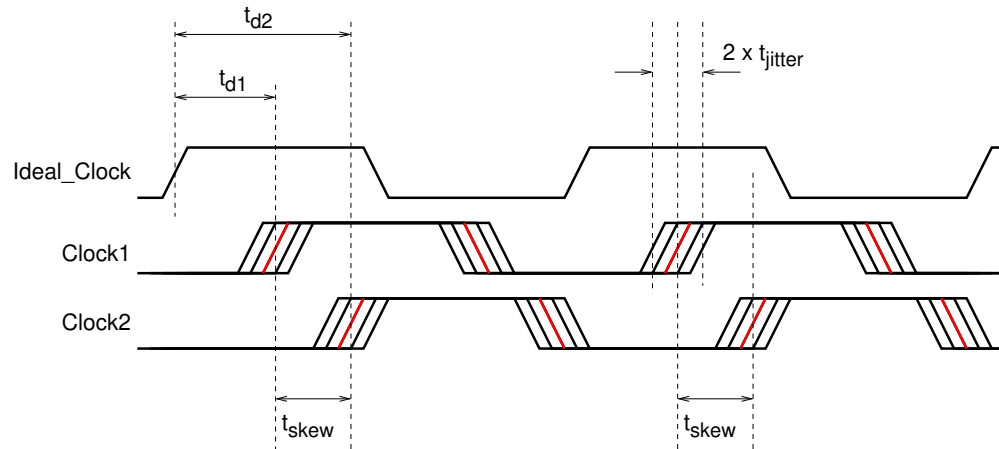
20022
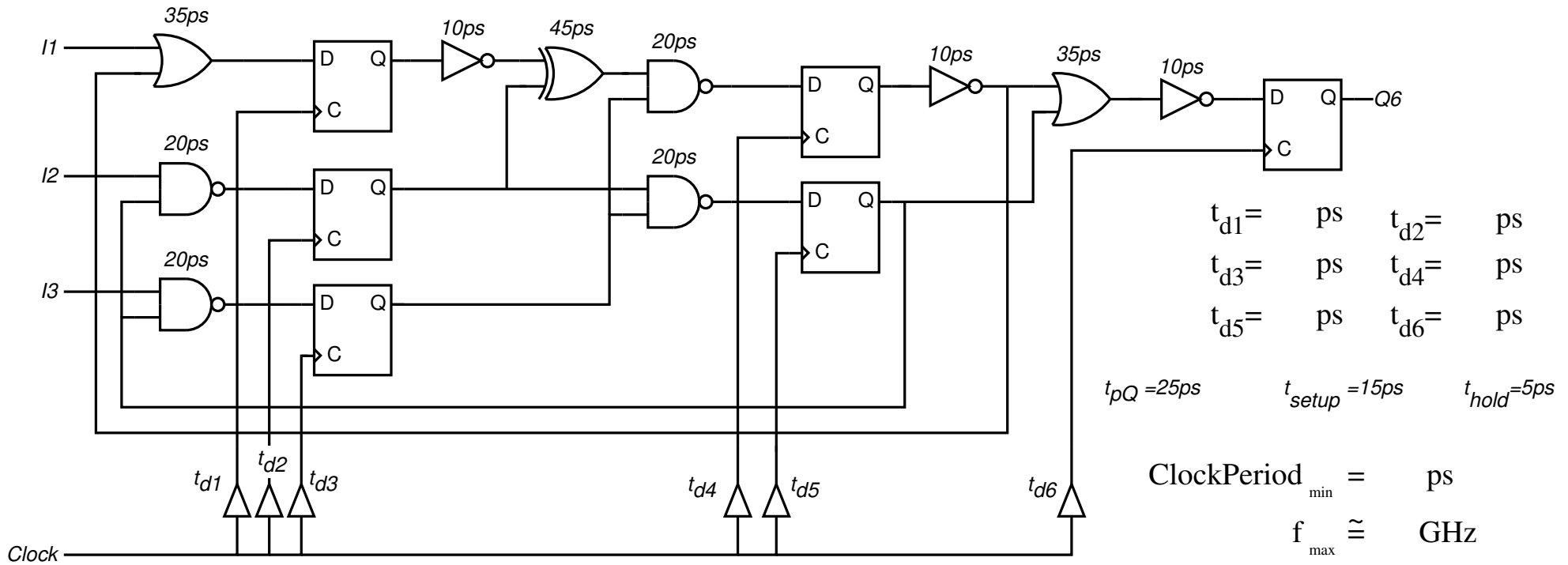
Synchronous Systems - Static Timing Analysis (inc. clock skew)

- Calculate f_{max} in the presence of intentional clock skew.

- Suggest suitable values for $t_{d1}, t_{d2}, t_{d3}, t_{d4}$ given that the minimum delay through the clock tree is 50ps

remember to check for hold violations

20023

Synchronous Systems - Jitter

- Jitter

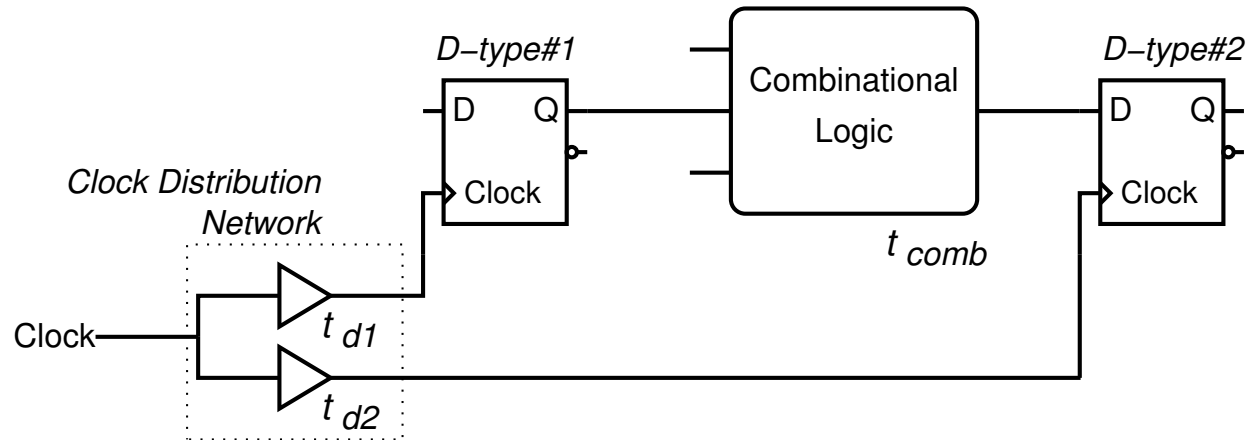 Jitter is the cycle-by-cycle variation in the arrival time of the clock.

- Caused by

  - Variation in frequency/phase of clock source[5]
  - Power supply noise affecting clock distribution
  - Cross-talk affecting clock distribution

- Jitter may cause unexpected timing violations

[5]primary clock source or Phase-Locked Loop (PLL)
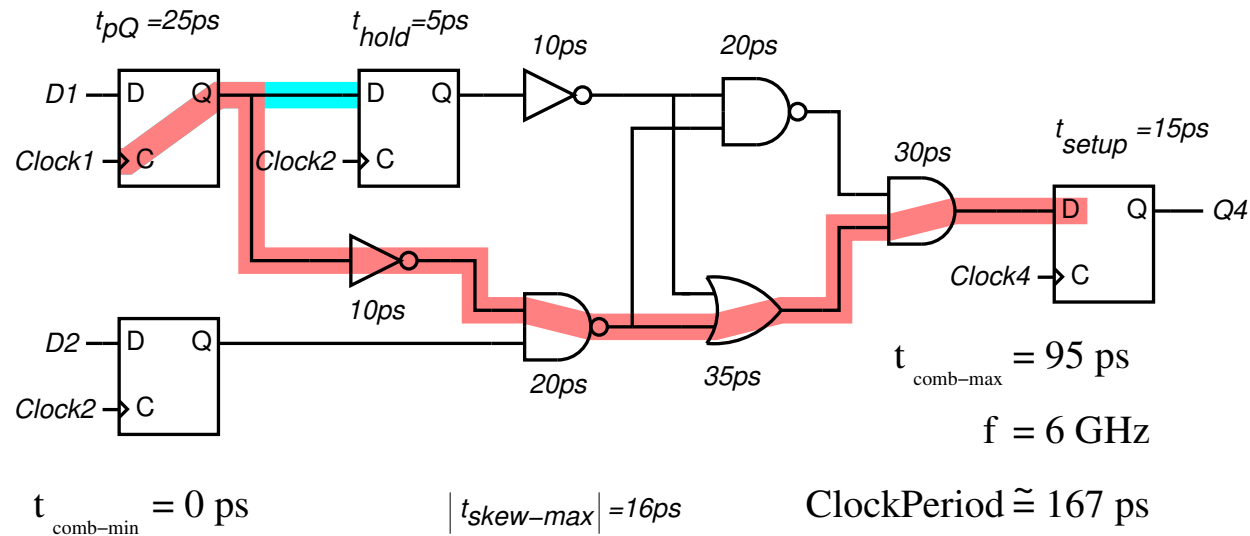
Synchronous Systems - Jitter

- To avoid a setup violation:

$$ClockPeriod > t_{pQ} + t_{comb} + t_{setup} + (t_{d1} - t_{d2}) + 2 \times t_{jitter}$$

- To avoid a hold violation:

$$t_{pQ} + t_{comb} > t_{hold} + (t_{d2} - t_{d1}) + 2 \times t_{jitter}$$

20025

Synchronous Systems - Static Timing Analysis (skew + jitter)

- What is the maximum jitter that can be tolerated given an operating frequency of 6GHz and clock skew of no more than 16ps?[6]

$$ClockPeriod > t_{pQ} + t_{comb-max} + t_{setup} + t_{skew} + 2 \times t_{jitter}$$

$$t_{pQ} + t_{comb-min} > t_{hold} + t_{skew} + 2 \times t_{jitter}$$

---

[6]remember to consider both setup and hold violations