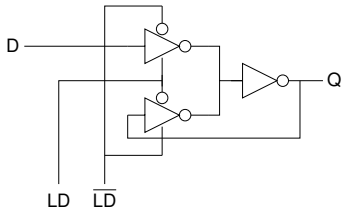
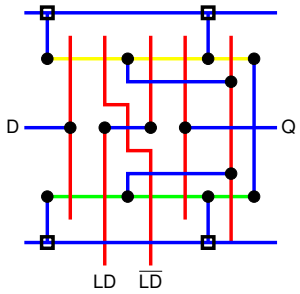
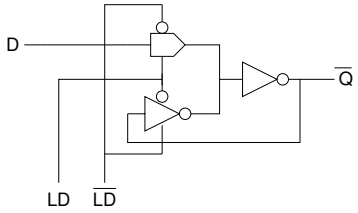
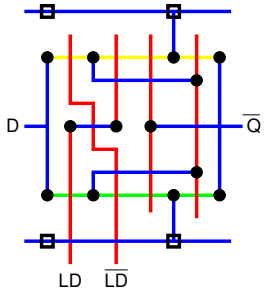
Latch

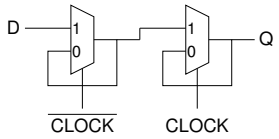


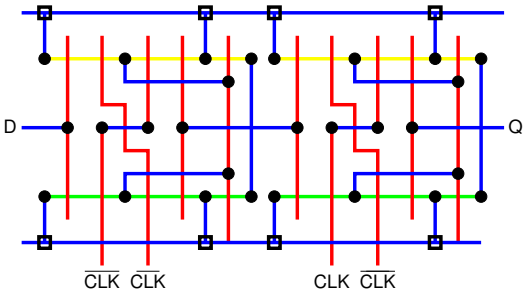


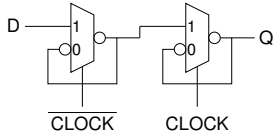


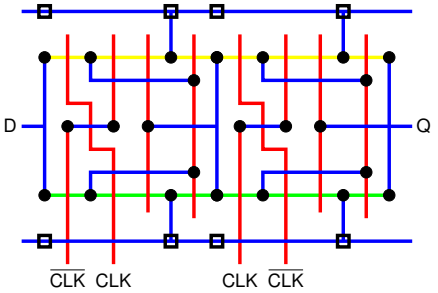


Master Slave D–Type Flip–Flop



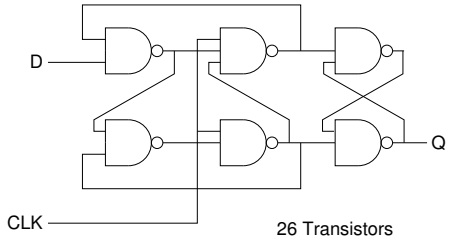


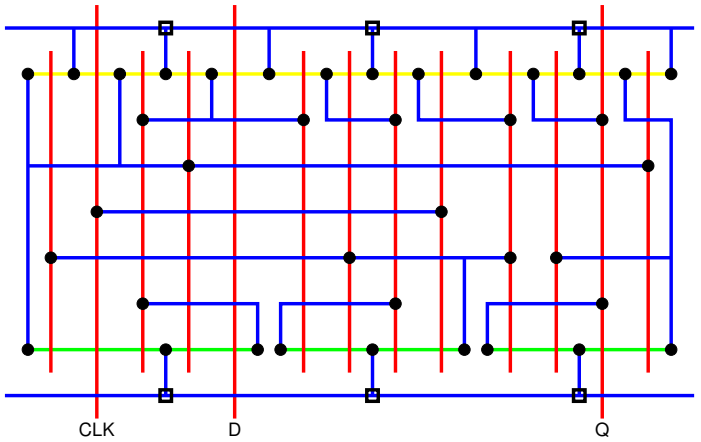




*muliplexor based latches and flip–flops include distictive polysilicon crossover

Edge Triggered D–Type Flip–Flop





Euler path analysis is applied creatively to these multi–gate cells – gates are often linked via the common gnd/pwr node
Final layouts will be more complex where clock buffers, reset circuitry and metal 2 i/o are included