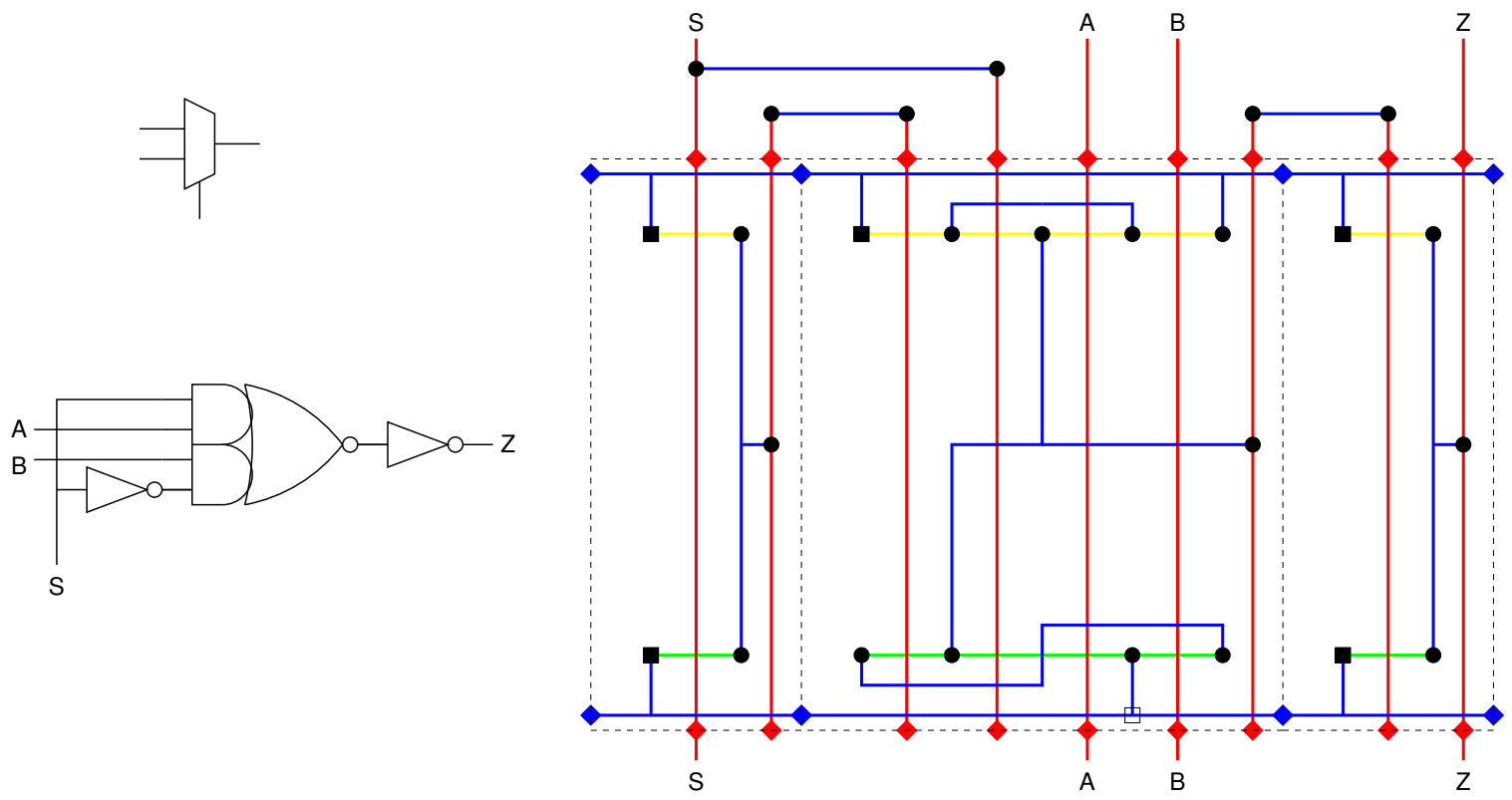


Digital CMOS Design

Multiple gates



Multiple gates

- Gates should all be of same height.
 - Power and ground rails will then line up when butted.
- All gate inputs and outputs are available at top and bottom.
 - All routing is external to cells.
 - Preserves the benefits of hierarchy.
- Interconnect is via *two conductor routing*.
 - In this case Polysilicon vertically and Metal horizontally.

Standard Cell Design

Many ICs are designed using the standard cell method.

- Cell Library Creation

A cell library, containing commonly used logic gates, is created for a process. This is often carried out by or on behalf of the foundry.

- ASIC¹ Design

The ASIC designer must design a circuit using the logic gates available in the library.

The ASIC designer usually has no access to the full layout of the standard cells and doesn't create any new cells for the library.

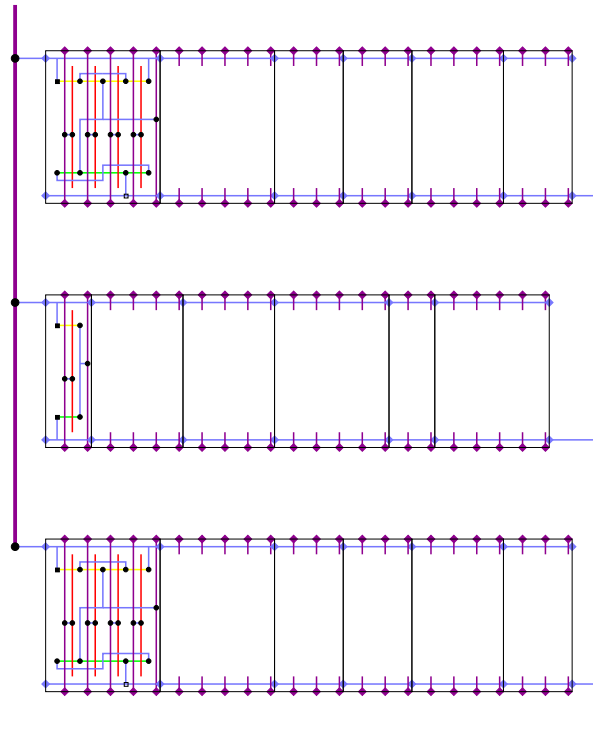
Layout work performed by the ASIC designer is divided into two stages:

- Placement
- Routing

¹Application Specific Integrated Circuit

Placement & Routing

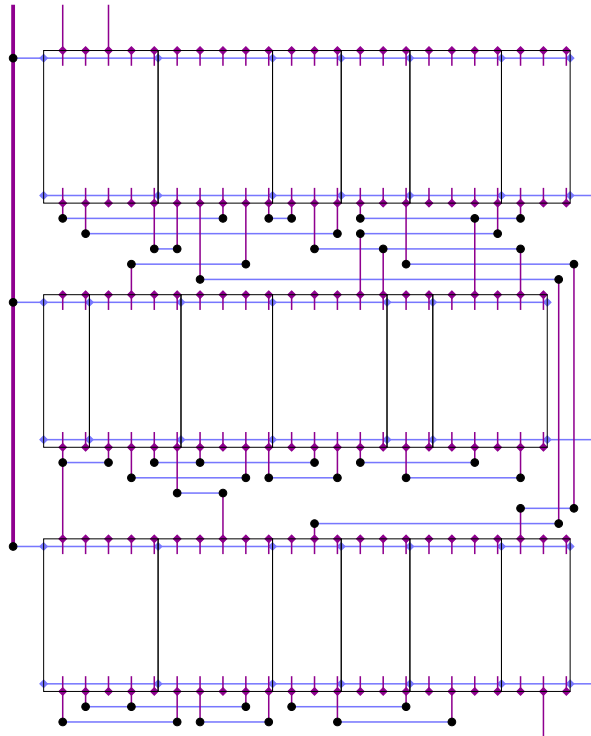
Placement



Cells are placed in one or several equal length lines with inter-digitated power and ground rails.

Placement & Routing

Routing



In the routing channels between the cells we route metal1 horizontally and metal2 vertically.

Placement & Routing

Two conductor routing

- Conductor A for horizontal inter-cell routing ²
Conductor B for vertical
- This logical approach means that we should never have to worry about signals crossing.
This makes life considerably easier for a computer (or even a human) to complete the routing.
- We must only ensure that two signals will not meet in the same horizontal or vertical channel.
- Computer algorithms can be used to ensure placement of cells such that wires are short.³
- Further computer algorithms can be used to optimize the routing itself.

²In the two-metal example Conductor A is Metal1 and Conductor B is Metal2

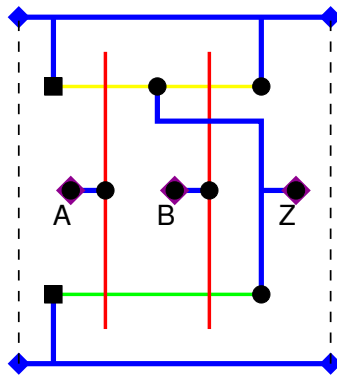
³In VLSI circuits we often find that inter-cell wiring occupies more area than the cells themselves.

Standard Cell Design

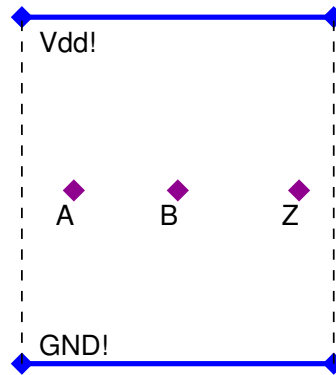
More Metal Layers

With three or more metal layers it is possible to take a different approach. The simplest example uses three metal layers.

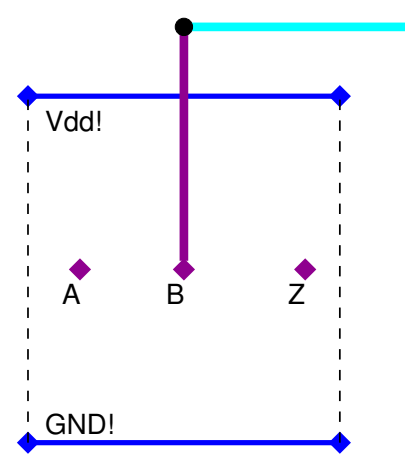
- Standard Cells
Use only metal1 except for I/O which is in metal2
- Two Conductor Routing
Uses metal2 and metal3



LAYOUT



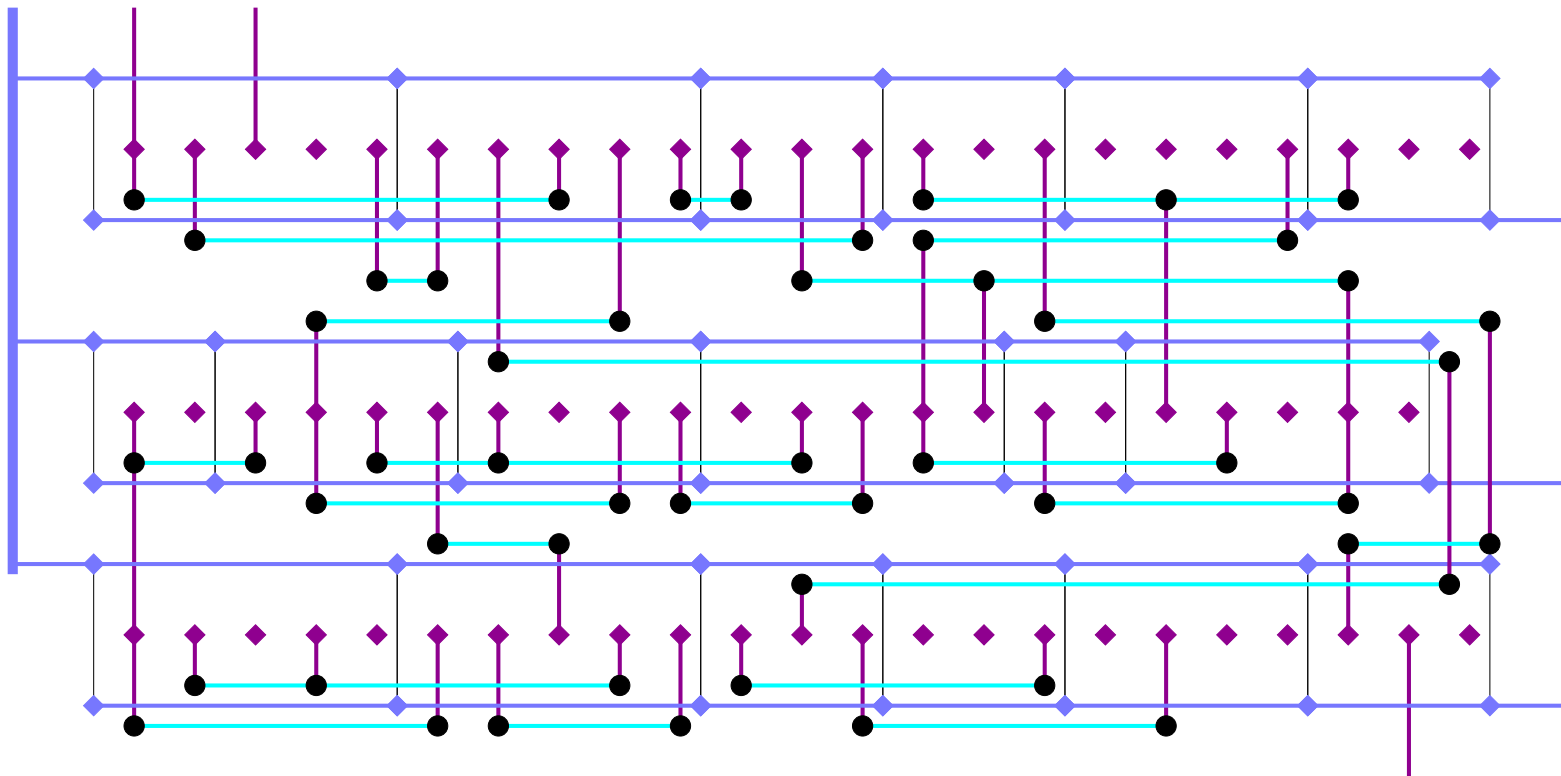
ABSTRACT



ROUTING

Standard Cell Design

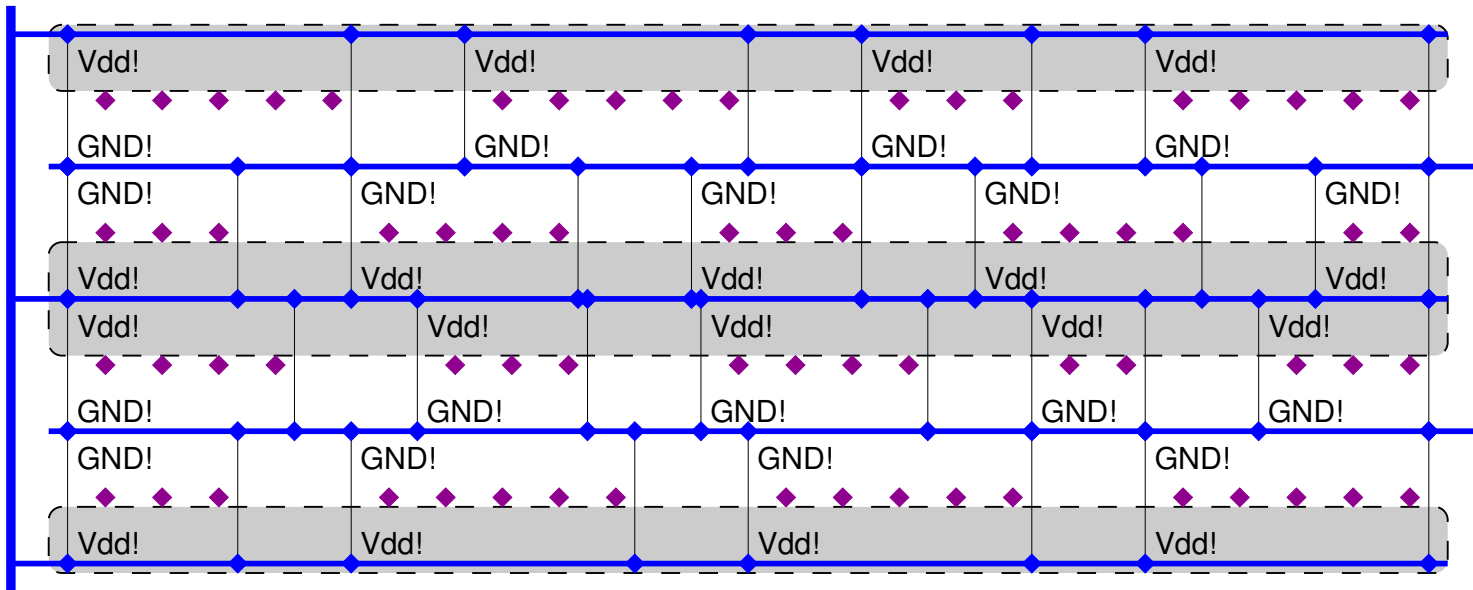
More Metal Layers



With this approach we can route safely over the cell to the specified pins leading to much smaller gaps between cell rows.

Standard Cell Design

Alternative Placement Style



By flipping every second row it may be possible to eliminate gaps between rows. N-wells are merged and power or ground rails are shared. This approach is normally associated with sparse rows and non channel based routing algorithms.