# Digital IC & Sytems Design

Iain McNally

 $\approx 10$  lectures

Koushik Maharatna

 $\approx$  12 lectures

Basel Halak

 $\approx$  12 lectures

# Digital IC & Sytems Design SoC Design Techniques

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# Digital IC & Sytems Design

### Assessment

10% Coursework L-Edit Gate Design (BIM)

90% Examination

### • Books

### **Integrated Circuit Design**

a.k.a. Principles of CMOS VLSI Design - A Circuits and Systems Perspective

Neil Weste & David Harris

Pearson, 2011

### Digital System Design with SystemVerilog

Mark Zwolinski

Pearson Prentice-Hall, 2010

# Digital IC & Sytems Design

# Iain McNally

# Integrated Circuit Design

- Content
  - Introduction
  - Overview of Technologies
  - Layout
  - CMOS Processing
  - Design Rules and Abstraction
  - Cell Design and Euler Paths
  - System Design using Standard Cells
  - Wider View

### Notes & Resources

http://users.ecs.soton.ac.uk/bim/notes/icd

#### 1947 First Transistor

John Bardeen, Walter Brattain, and William Shockley (Bell Labs)

# 1952 Integrated Circuits Proposed

Geoffrey Dummer (Royal Radar Establishment) - prototype failed...

### 1958 First Integrated Circuit

Jack Kilby (Texas Instruments) - Co-inventor

# 1959 First Planar Integrated Circuit

Robert Noyce (Fairchild) - Co-inventor

#### 1961 First Commercial ICs

Simple logic functions from TI and Fairchild

#### 1965 Moore's Law

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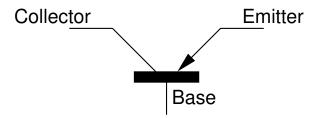
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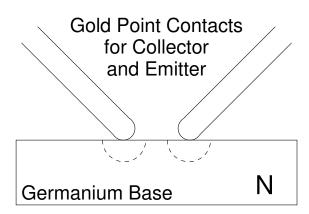
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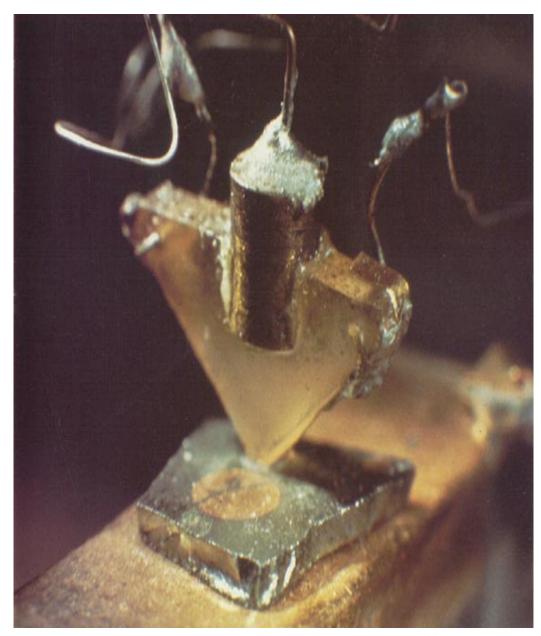
#### 1965 Moore's Law

### **1947 Point Contact Transistor**





Each contact creates a metal/semiconductor (Schottky) diode Depletion regions are shown for zero bias voltage.



Source: Bell Labs

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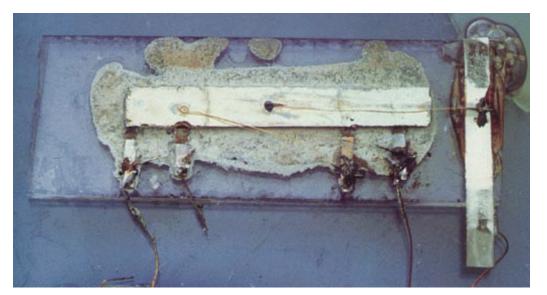
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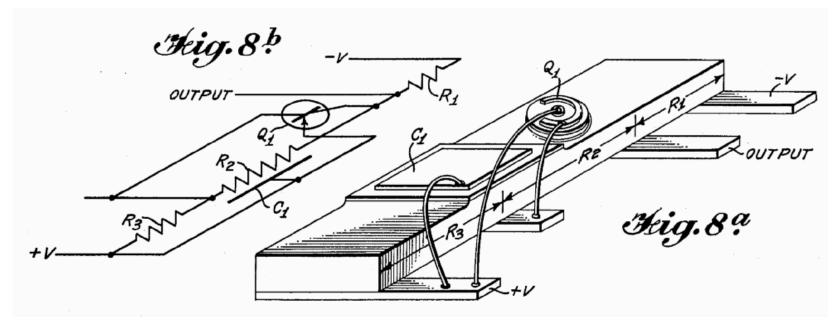
### 1958 First Integrated Circuit

- 1 Transistor
- 1 Capacitor
- 3 Resistors

Hand soldered interconnect



Source: Texas Instruments



Source: Jack Kilby (Patent Application)

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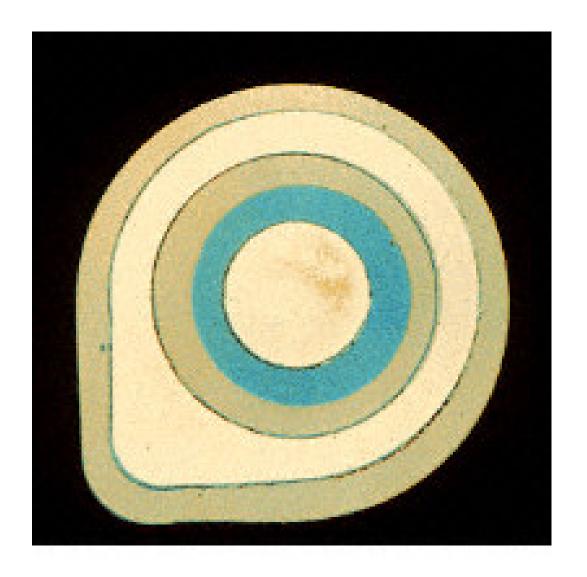
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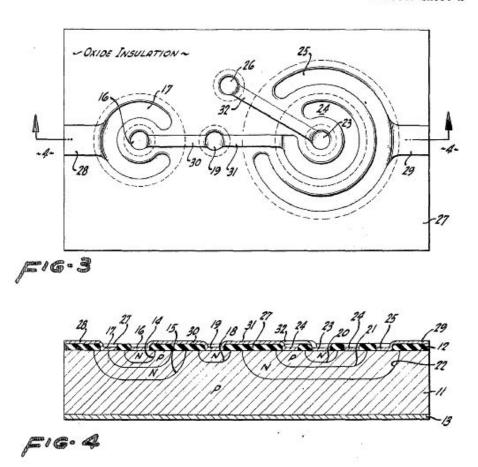


Source: Fairchild

SEMICONDUCTOR DEVICE-AND-LEAD STRUCTURE

Filed July 30, 1959

3 Sheets-Sheet 2



Source: Robert Noyce (Patent Application)

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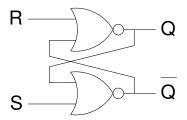
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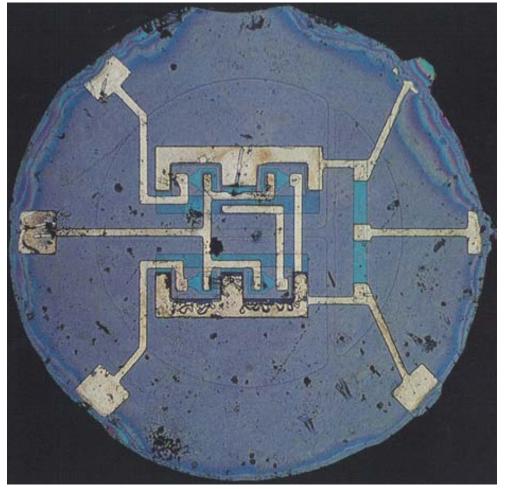
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#### 1965 Moore's Law

### **1961 First Commercial ICs**

Fairchild Bipolar RTL RS Flip-Flop

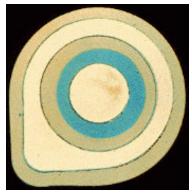




Source: Fairchild

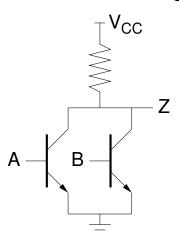
#### Using

• Planar Bipolar Transistors



Source: Fairchild

- Back to back PN junctions to provide isolation
- Integrated interconnect
- Resistor Transistor Logic



RTL NOR gate

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### Moore's Law

Predicts exponential growth in the number of components per chip.

# 1965 - 1975 Doubling Every Year

In 1965 Gordon Moore observed that the number of components per chip had doubled every year since 1959 and predicted that the trend would continue through to 1975.

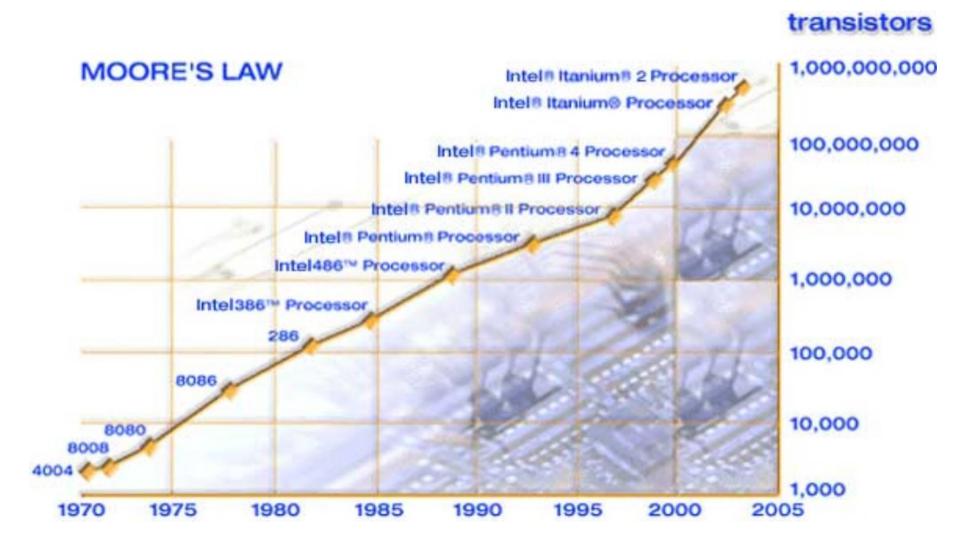
Moore describes his initial growth predictions as "ridiculously precise".

# 1975 - 201? Doubling Every Two Years

In 1975 Moore revised growth predictions to doubling every two years.

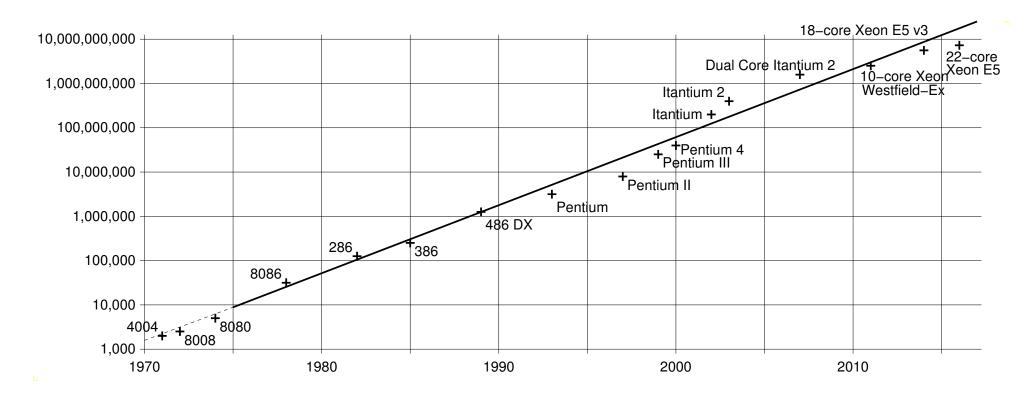
Growth would now depend only on process improvements rather than on more efficient packing of components.

In 2000 he predicted that the growth would continue at the same rate for another 10-15 years before slowing due to physical limits.



Source: Intel

# Moore's Law at Intel<sup>1</sup>



<sup>&</sup>lt;sup>1</sup>Intel was founded by Gordon Moore and Robert Noyce from Fairchild

# Moore's Law; a Self-fulfilling Prophesy

The whole industry uses the Moore's Law curve to plan new fabrication facilities.

**Slower** - wasted investment

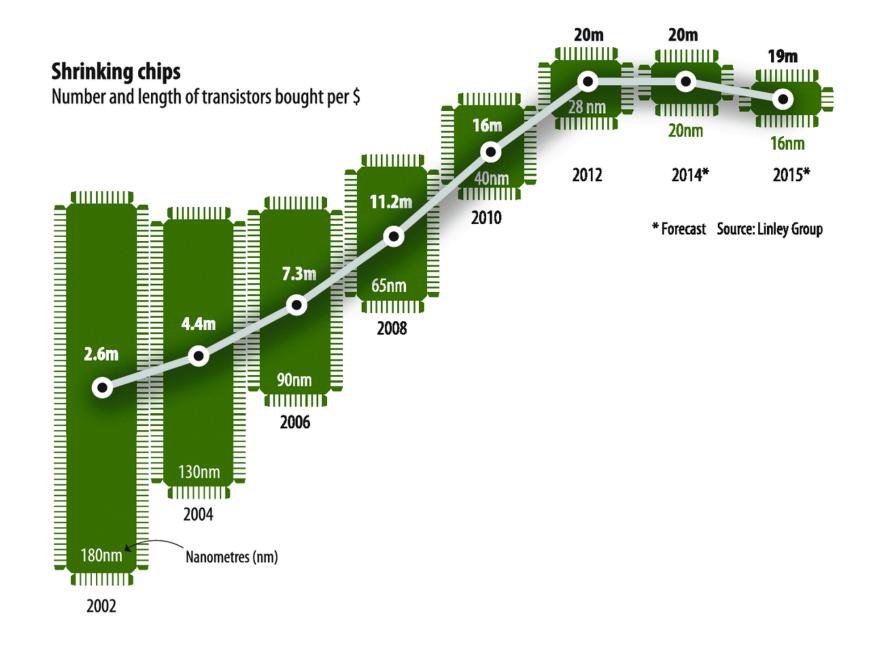
Must keep up with the Joneses<sup>2</sup>.

**Faster** - too costly

Cost of capital equipment to build ICs doubles approximately every 4 years.

Moore's law is not dead (at least not quite), although there are worries that below 20nm, clever processing required for smaller transistors means that cost per transistor goes up rather than down.

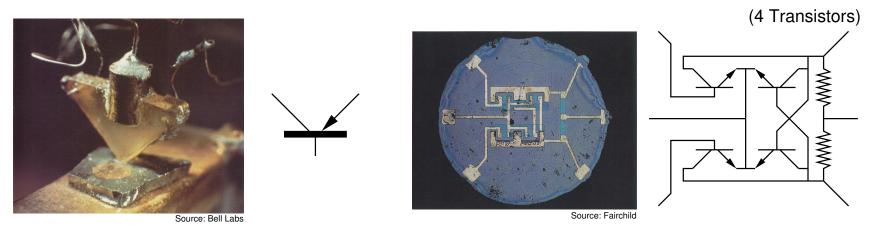
<sup>&</sup>lt;sup>2</sup>or the Intels



#### Is Moore's Law Ending? Chip introduction ■ Transistors per chip, '000 Clock speed (max), MHz Thermal design power\*, w dates, selected Transistors bought per \$, m Core 2 Duo Pentium 4 Xeon Log scale Pentium III 15 107 Pentium II 10 5 Pentium 105 2002 04 06 08 10 12 15 486 8086 386 $10^{3}$ 4004 10 - 10<sup>-1</sup> 75 80 85 90 95 05 10 15 1970 2000

Sources: Intel; press reports; Bob Colwell; Linley Group; IB Consulting; *The Economist* \*Maximum safe power consumption Economist, March 12-18, 2016

1947 Point Contact transistor 1961 Fairchild Bipolar RTL RS Flip-Flop



Moore's Law (1965) Number of transistor has doubled every year and will continue to do so until 1975

Moore's Law (1975) Number of transistors will double every two years

