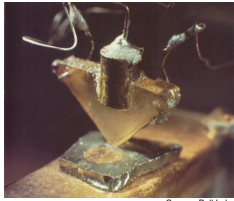
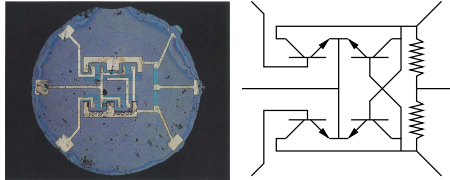


1947 Point Contact transistor



Source: Bell Labs

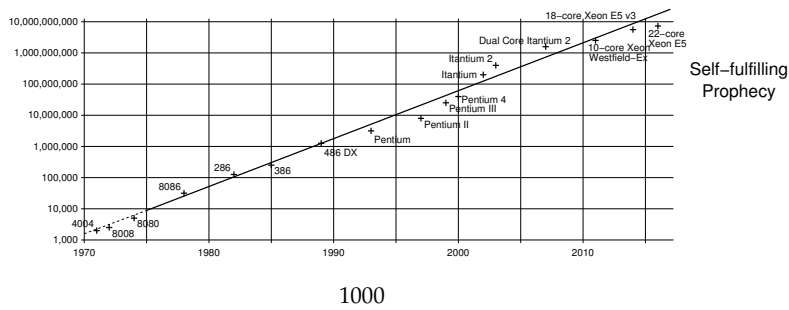
1961 Fairchild Bipolar RTL RS Flip-Flop (4 Transistors)



Source: Fairchild

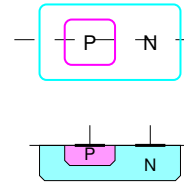
Moore's Law (1965) Number of transistor has doubled every year and will continue to do so until 1975

Moore's Law (1975) Number of transistors will double every two years

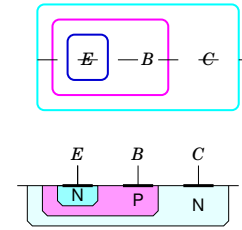


1000

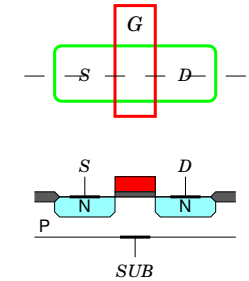
Diode



NPN Transistor



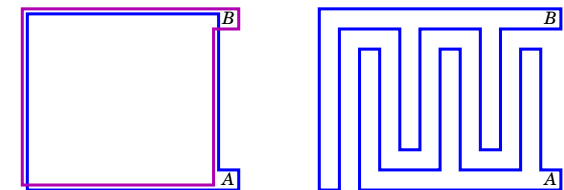
NMOS Enhancement transistor
NMOS Process



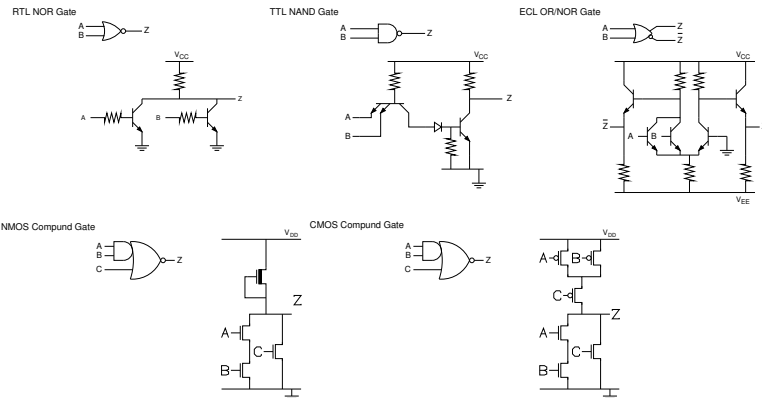
Resistor

1	2	3	4	5	6	7	8	9	1
3	18	17	16	15	14	13	12	11	2
19									
4	20	21	22	23	24	25	26	27	5
7	36	35	34	33	32	31	30	29	6
37									
8	38	39	40	41	42	43	44	45	46

Capacitors



3000

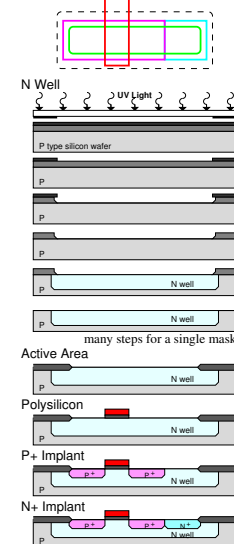


- Bipolar Transistors with Resistors - MSI/LSI
RTL - NOR TTL - NAND ECL - OR/NOR
- MOS Transistors (no resistors) - VLSI
NMOS CMOS - No static power!

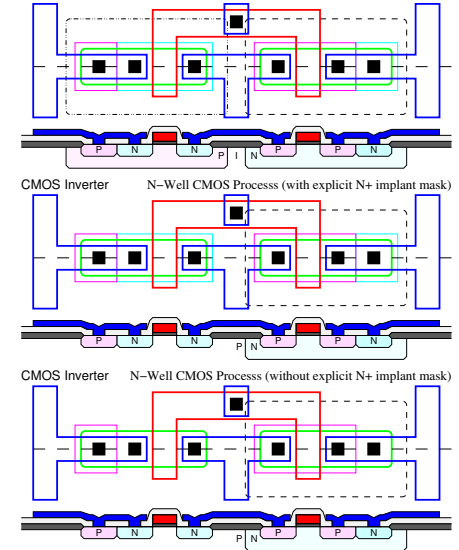
Both allow construction of NOR, NAND & Compound gate (always inverting)

2000

PMOS Enhancement transistor
CMOS Process



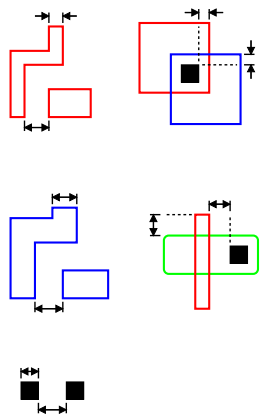
CMOS Inverter Twin Tub CMOS Process



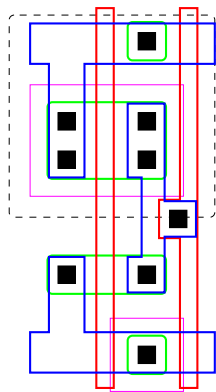
Features may be determined by a number of masks
e.g. NMOS source drain: ActiveArea AND NOT(NWell OR Poly OR PImplant)

4000

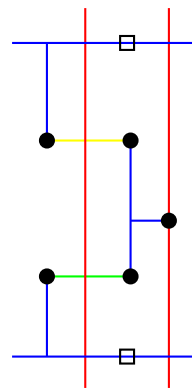
Design Rules – width, separation, overlap



Optimised Mask Layout



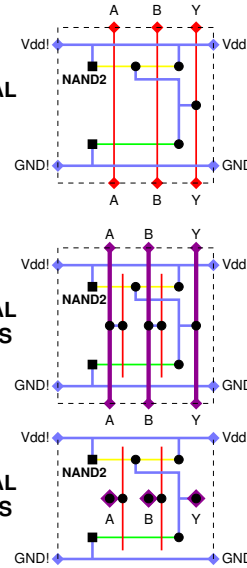
Equivalent Stick Diagram



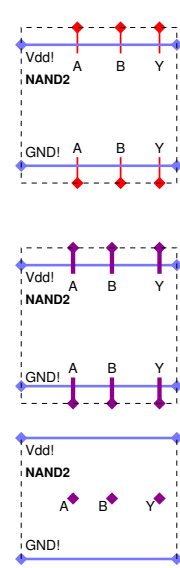
- Metal
- Polysilicon
- N+
- P+
- Contact
- Tap
- Combined contact & tap

5000

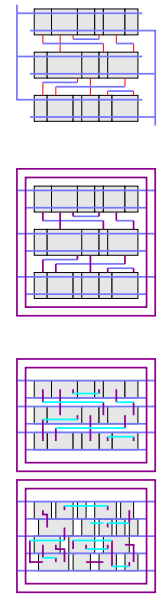
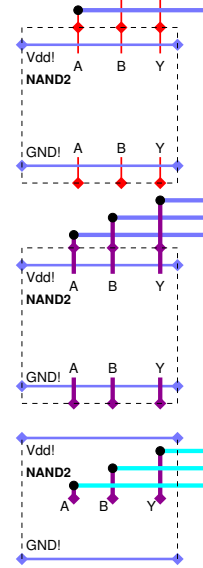
LAYOUT



ABSTRACT



ROUTING



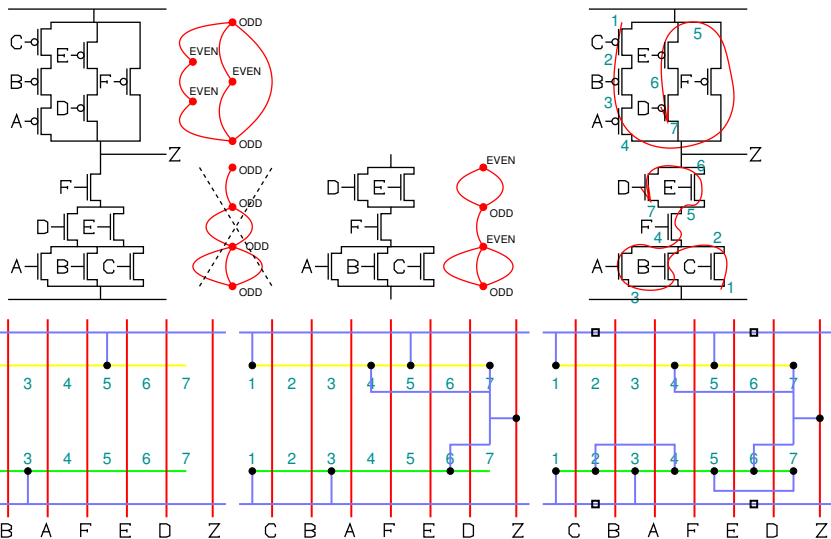
1 METAL LAYER

2 METAL LAYERS

3 METAL LAYERS

7000

Investigation of Euler paths leads to more efficient layout*



*not all gates will support a common Euler path for both PMOS and NMOS

6000

Programmable Logic Semi-Custom Full Custom

Skill Required	Little Lots	[Line from Little to Lots]	
Time to Market	Quick Slow	[Line from Quick to Slow]	
One-off Manufacturing Cost	Cheap Expensive	[Line from Cheap to Expensive]	
Unit Cost In Production	Cheap Expensive	[Line from Cheap to Expensive]	
Speed	Fast Slow	[Line from Fast to Slow]	
Area	Small Big	[Line from Small to Big]	
Power	Low High	[Line from Low to High]	

All design styles need full custom designers
A large ASIC (especially SoC) may mix Semi-Custom and Full Custom

8000