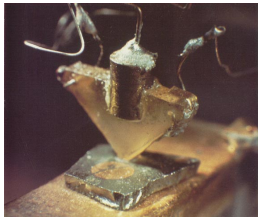
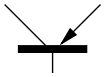
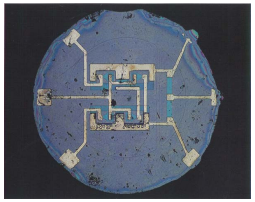
1947 Point Contact transistor

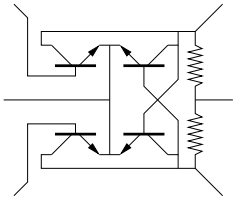




1961 Fairchild Bipolar RTL RS Flip–Flop

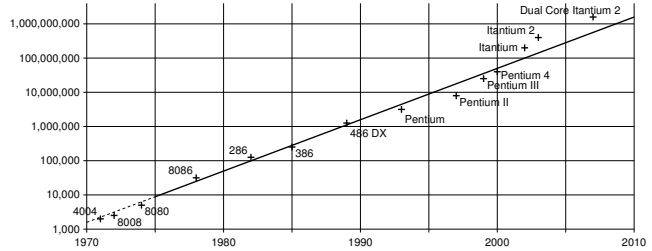
(4 Transistors)





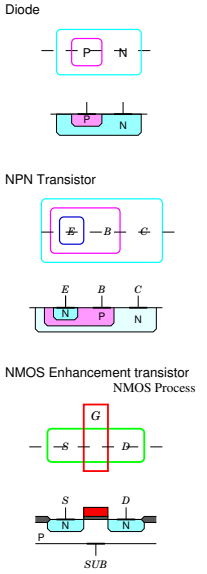
1965 Moore's Law (Mk I) Number of transistor has doubled every year and will continue to do so until 1975

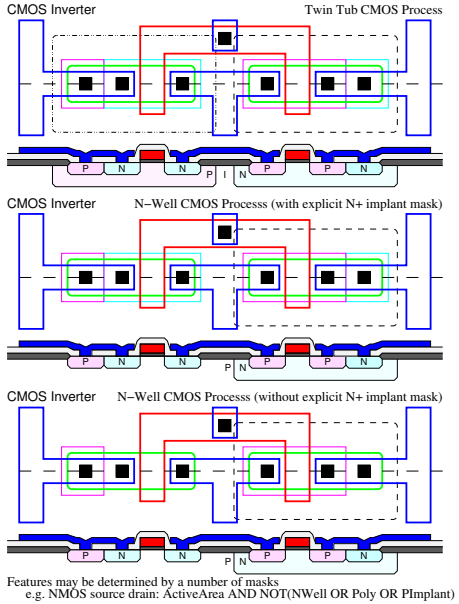
1975 Moore's Law (Mk II) Number of transistors will double every two years



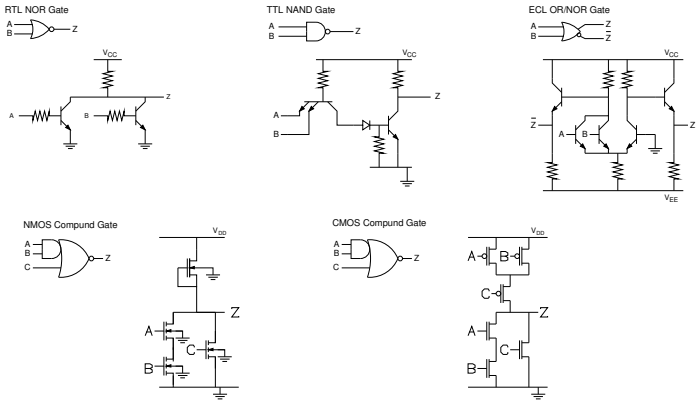
Self–fulfilling Prophecy

1000





3000



- Bipolar Transitors with Resistors - MSI/LSI

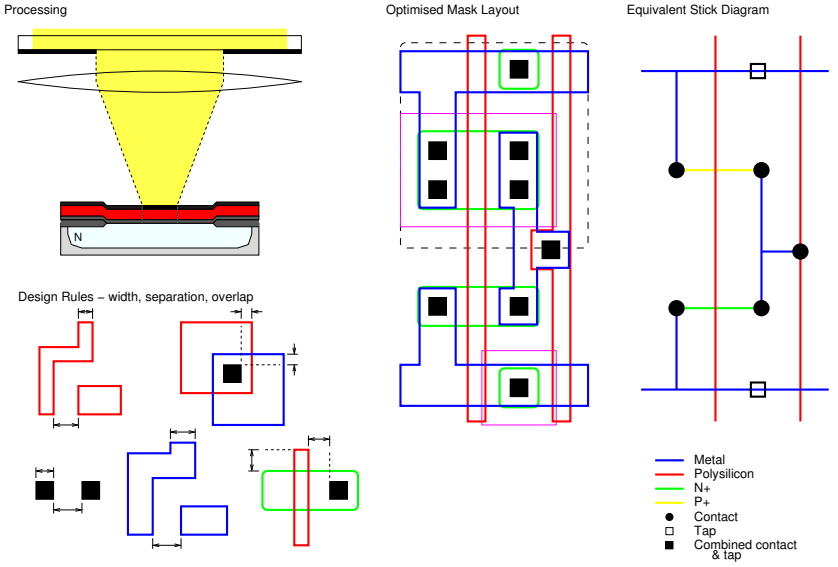
  RTL - NOR TTL - NAND ECS - OR/NOR

- MOS Transistors (no resistors) - VLSI

  NMOS CMOS - No static power!

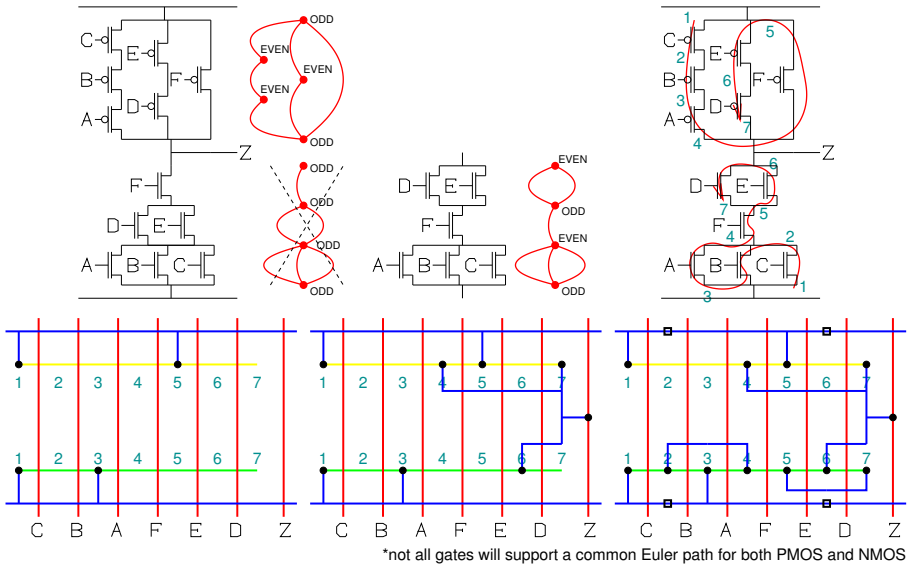
Both allow construction of NOR, NAND & Compound gate (always inverting)

2000



4000

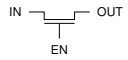
Investigation of Euler paths leads to more efficient layout*



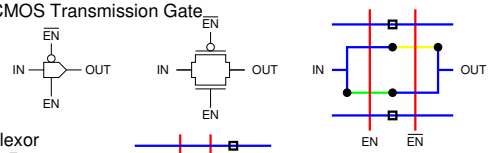
*not all gates will support a common Euler path for both PMOS and NMOS

5000

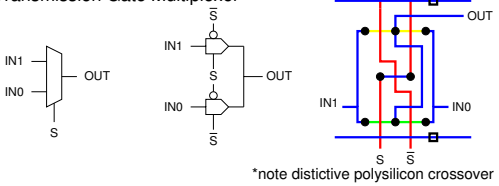
Pass Transistor



CMOS Transmission Gate



Transmission Gate Multiplexor

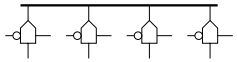


*note distictive polysilicon crossover

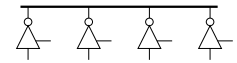
Tri–state gates are used for Multiplexing

Distributed Multiplexing

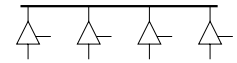
using transmission gates



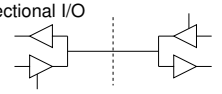
using tri–state inverters



using tri–state buffers

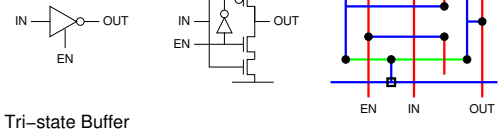


Bi–directional I/O

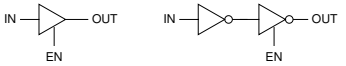


*this is another form of multiplexing

Tri–state Inverter

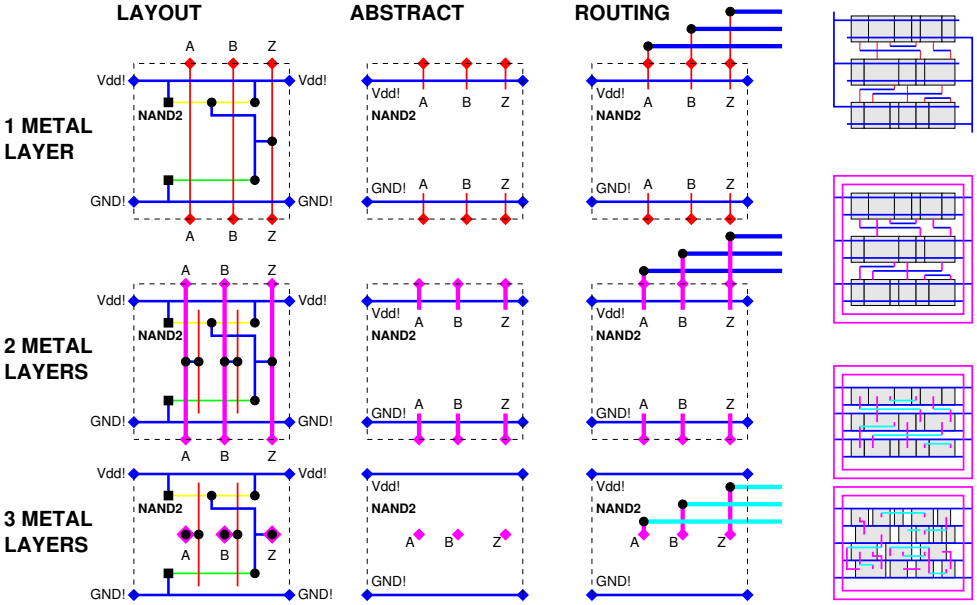


Tri–state Buffer



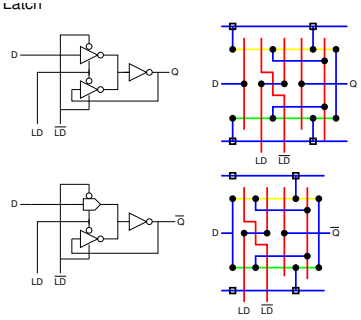
7000

LAYOUT ABSTRACT ROUTING

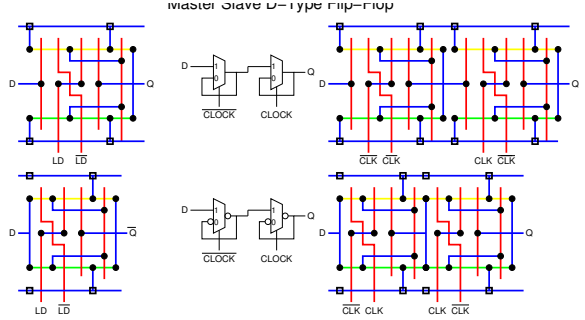


6000

Latch

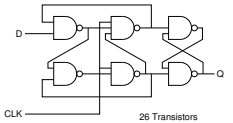


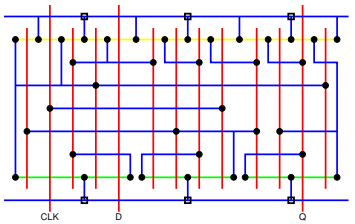
Master Slave D–Type Flip–Flop



*muliplexor based latches and flip–flops include distictive polysilicon crossover

Edge Triggered D–Type Flip–Flop

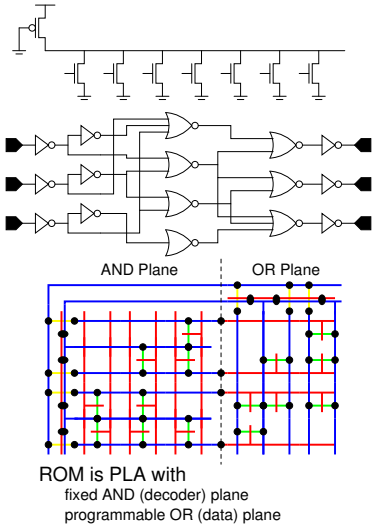




Euler path analysis is applied creatively to these multi–gate cells – gates are often linked via the common gnd/pwr node
Final layouts will be more complex where clock buffers, reset circuitry and metal 2 i/o are included

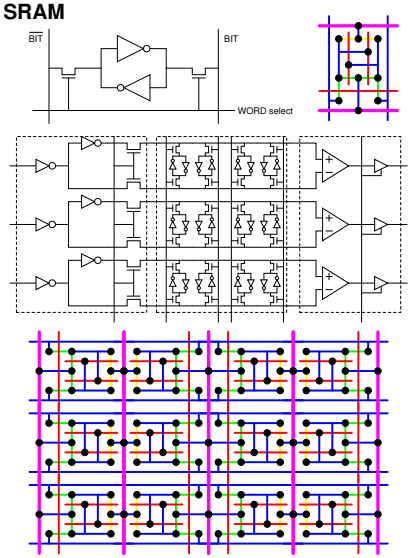
8000

PLA and ROM



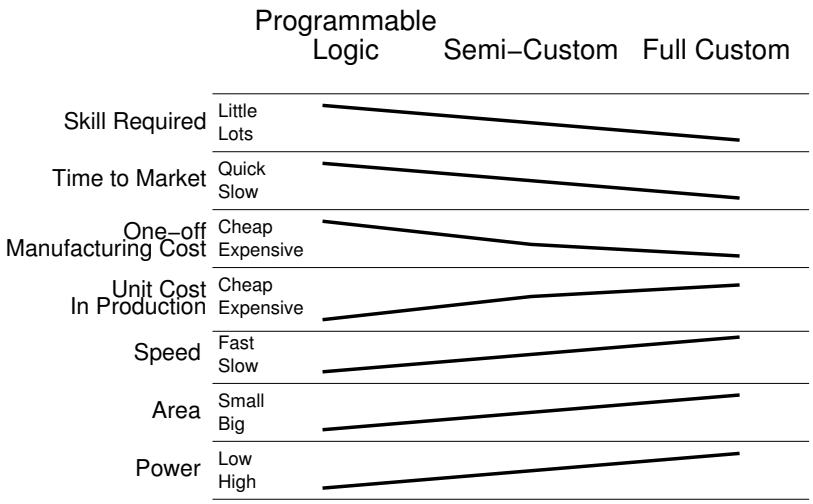
ROM is PLA with
fixed AND (decoder) plane
programmable OR (data) plane

SRAM



Cells are designed to butt together in two dimensions leading to efficient layout

PLA layout efficiency will depend on the actual function implemented (e.g. number of common product terms)



All design styles need full custom designers

A large ASIC (especially SoC) may mix Semi−Custom and Full Custom