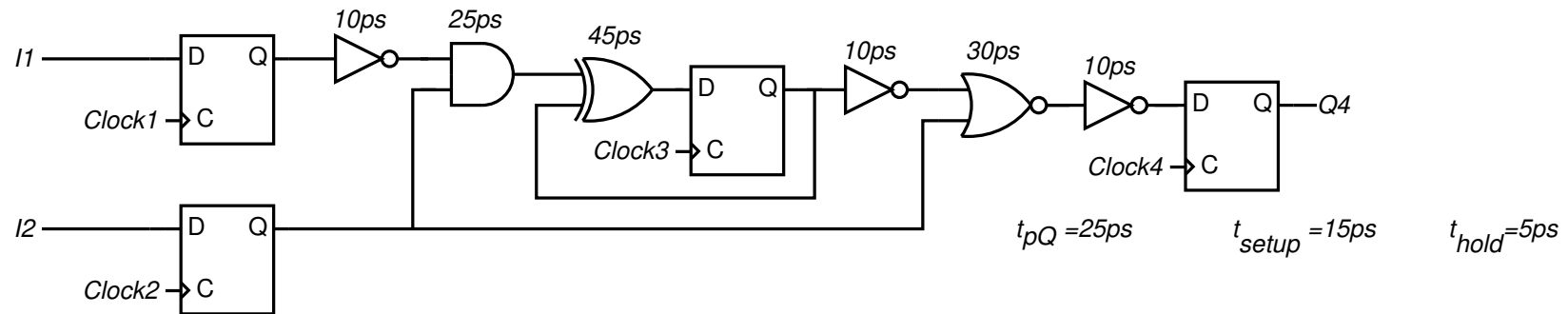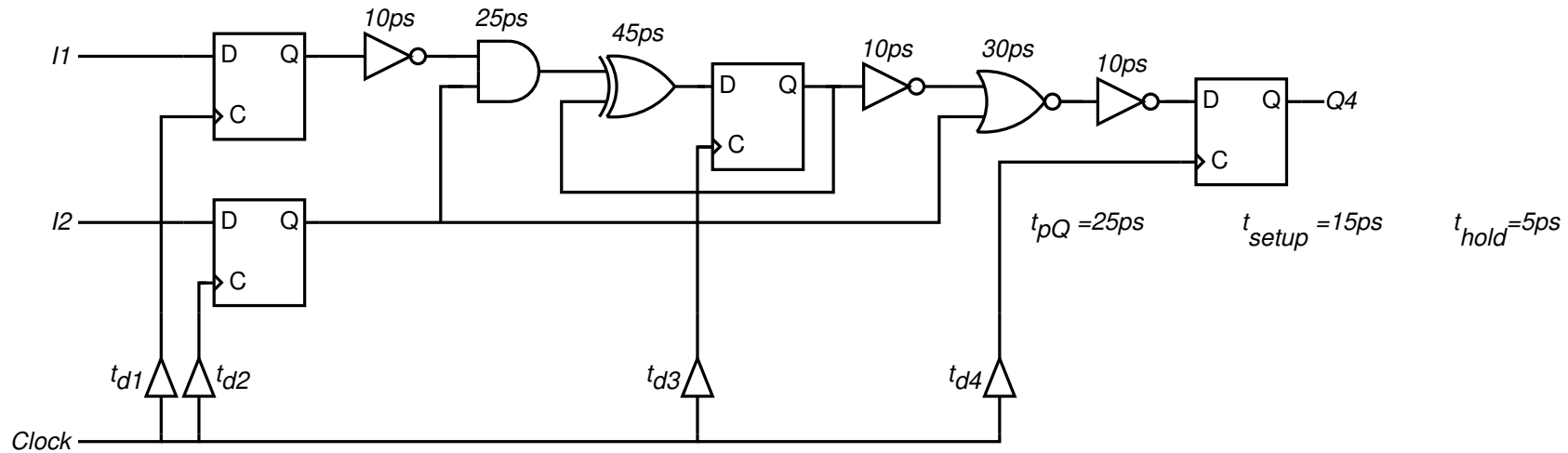# Synchronous Systems - Static Timing Analysis (inc. clock skew)

• Calculate f_{max} in the presence of intentional clock skew.

20101

Synchronous Systems - Static Timing Analysis (inc. clock skew)

- Calculate f_{max} in the presence of intentional clock skew.

- Suggest suitable values for t_{d1}, t_{d2}, t_{d3}, t_{d4}

20102

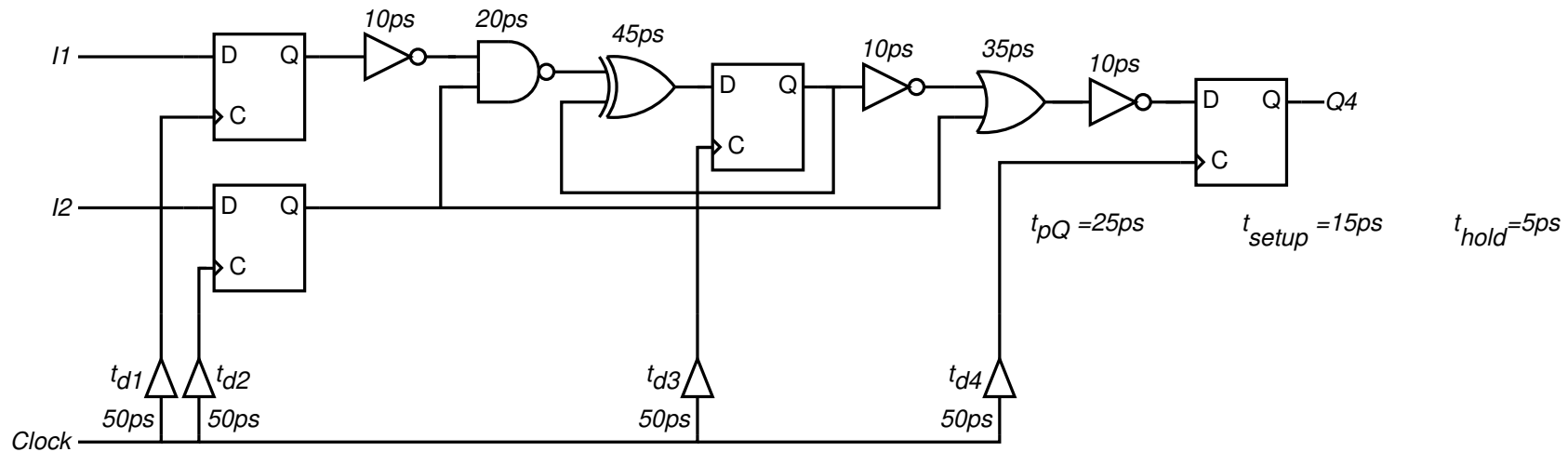# Synchronous Systems - Static Timing Analysis (inc. clock skew)

- Calculate f_{max} in the presence of intentional clock skew.

- Suggest suitable values for t_{d1}, t_{d2}, t_{d3}, t_{d4}
  Initially set all to a minimum value (in this case 50ps)
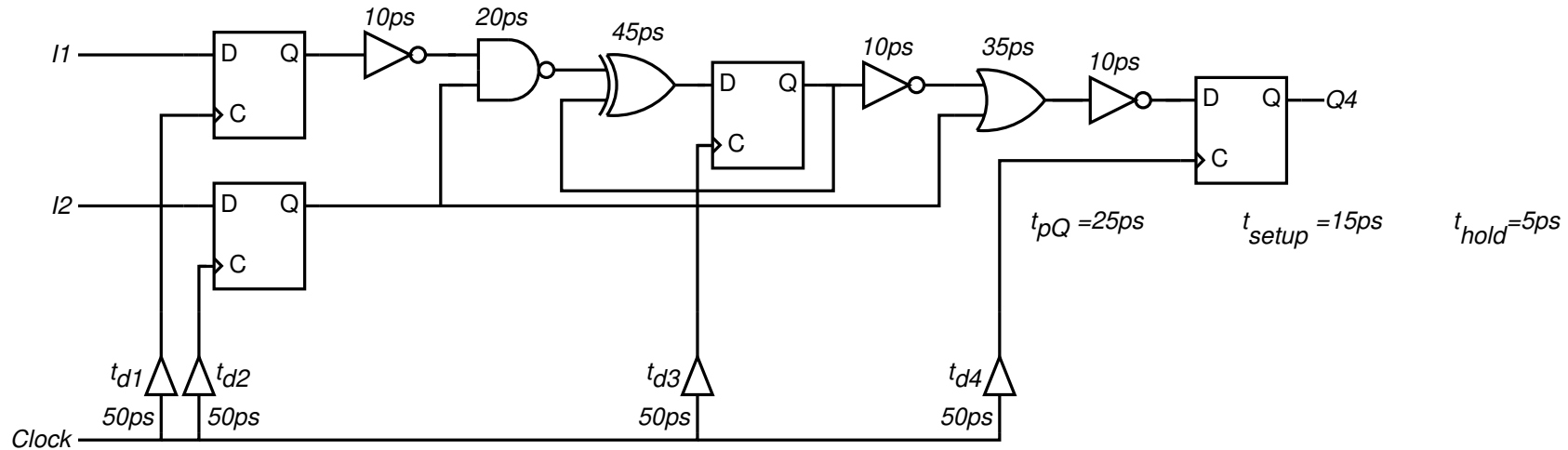
20103

Synchronous Systems - Static Timing Analysis (inc. clock skew)

- Calculate f_{max} in the presence of intentional clock skew.

- Suggest suitable values for t_{d1}, t_{d2}, t_{d3}, t_{d4}

$\Rightarrow$ Identify longest timing paths
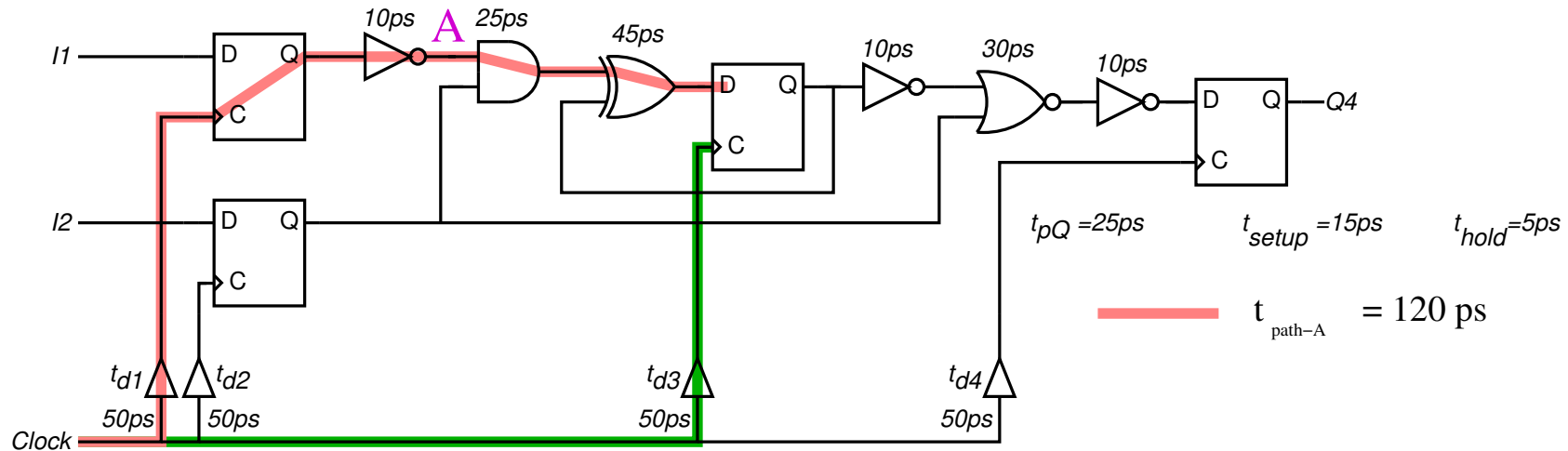
20104

Synchronous Systems - Static Timing Analysis (inc. clock skew)

- Calculate f_{max} in the presence of intentional clock skew.
- Suggest suitable values for t_{d1}, t_{d2}, t_{d3}, t_{d4}
$\Rightarrow$ Identify longest timing paths

$$t_{path-A} = t_{pQ} + t_{comb-A} + t_{setup} + (t_{d1} - t_{d3})$$
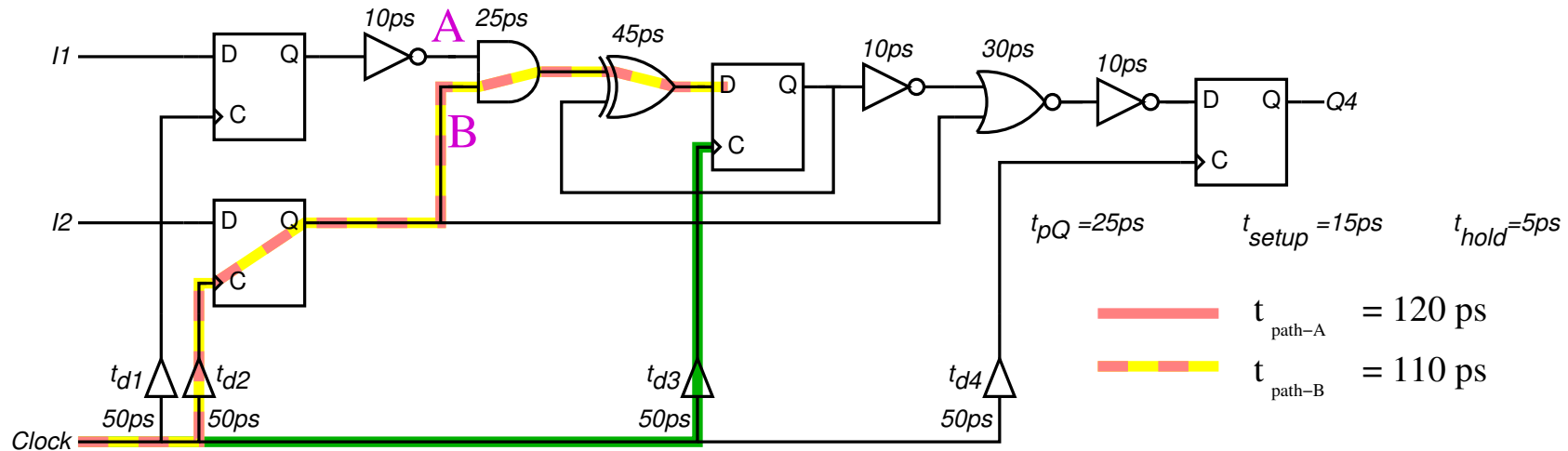
20105

Synchronous Systems - Static Timing Analysis (inc. clock skew)

- Calculate f_{max} in the presence of intentional clock skew.
- Suggest suitable values for t_{d1}, t_{d2}, t_{d3}, t_{d4}

$\Rightarrow$ Identify longest timing paths

$$t_{path-B} = t_{pQ} + t_{comb-B} + t_{setup} + (t_{d2} - t_{d3})$$

20105

Synchronous Systems - Static Timing Analysis (inc. clock skew)

$t_{pQ} = 25ps$ $t_{setup} = 15ps$ $t_{hold} = 5ps$

t_{path-A}	= 120 ps
t_{path-B}	= 110 ps
t_{path-C}	= 85 ps

- Calculate f_{max} in the presence of intentional clock skew.
- Suggest suitable values for t_{d1}, t_{d2}, t_{d3}, t_{d4}
- ⇒ Identify longest timing paths

$$t_{path-C} = t_{pQ} + t_{comb-C} + t_{setup} + (t_{d3} - t_{d3})$$
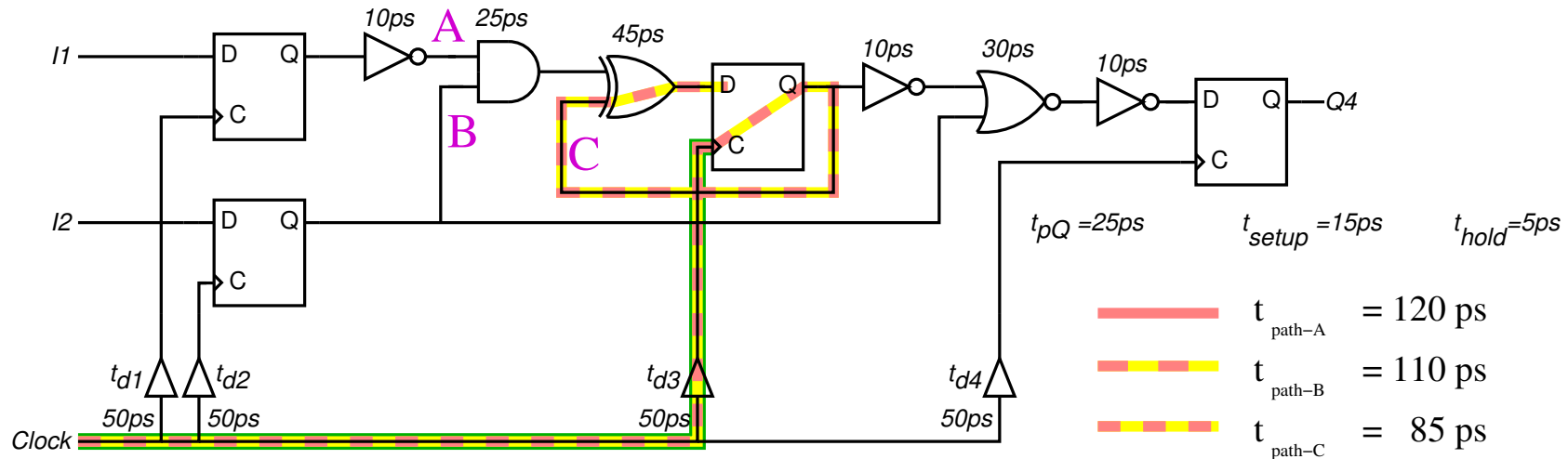
20105

Synchronous Systems - Static Timing Analysis (inc. clock skew)

- Calculate f_{max} in the presence of intentional clock skew.

- Suggest suitable values for t_{d1}, t_{d2}, t_{d3}, t_{d4}

$\Rightarrow$ Identify longest timing paths

$$t_{path-D} = t_{pQ} + t_{comb-D} + t_{setup} + (t_{d3} - t_{d4})$$
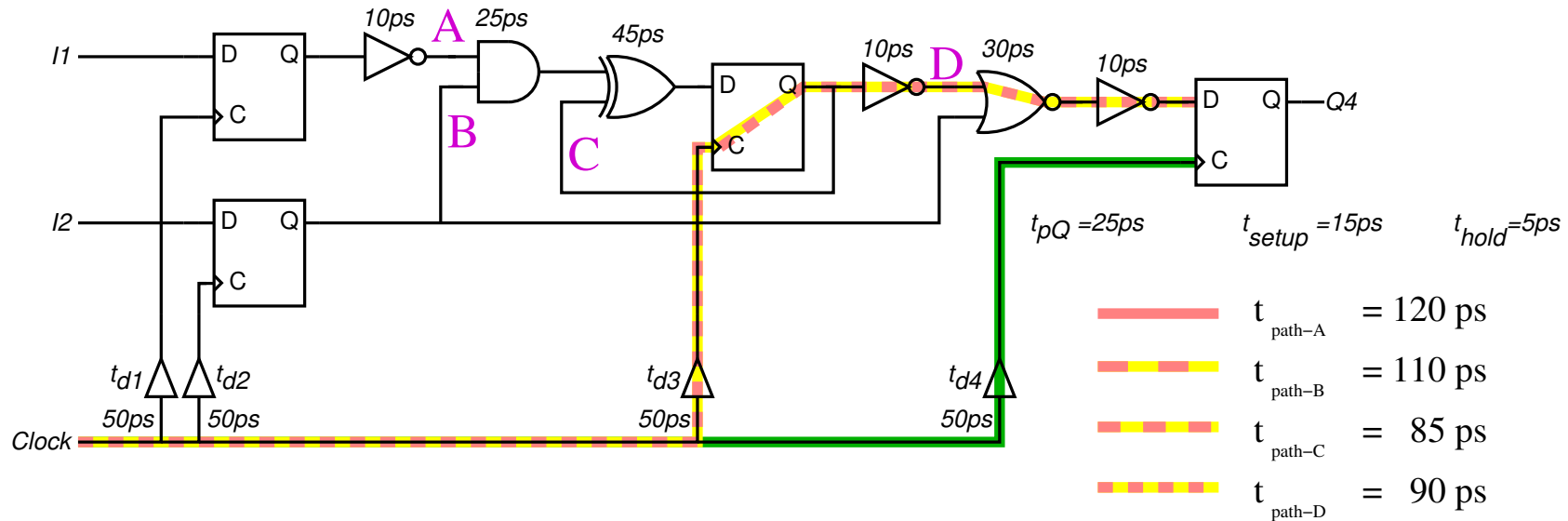
20105

Synchronous Systems - Static Timing Analysis (inc. clock skew)

- Calculate f_{max} in the presence of intentional clock skew.
- Suggest suitable values for $t_{d1}, t_{d2}, t_{d3}, t_{d4}$
$\Rightarrow$ Identify longest timing paths

$$t_{path-D} = t_{pQ} + t_{comb-E} + t_{setup} + (t_{d2} - t_{d4})$$
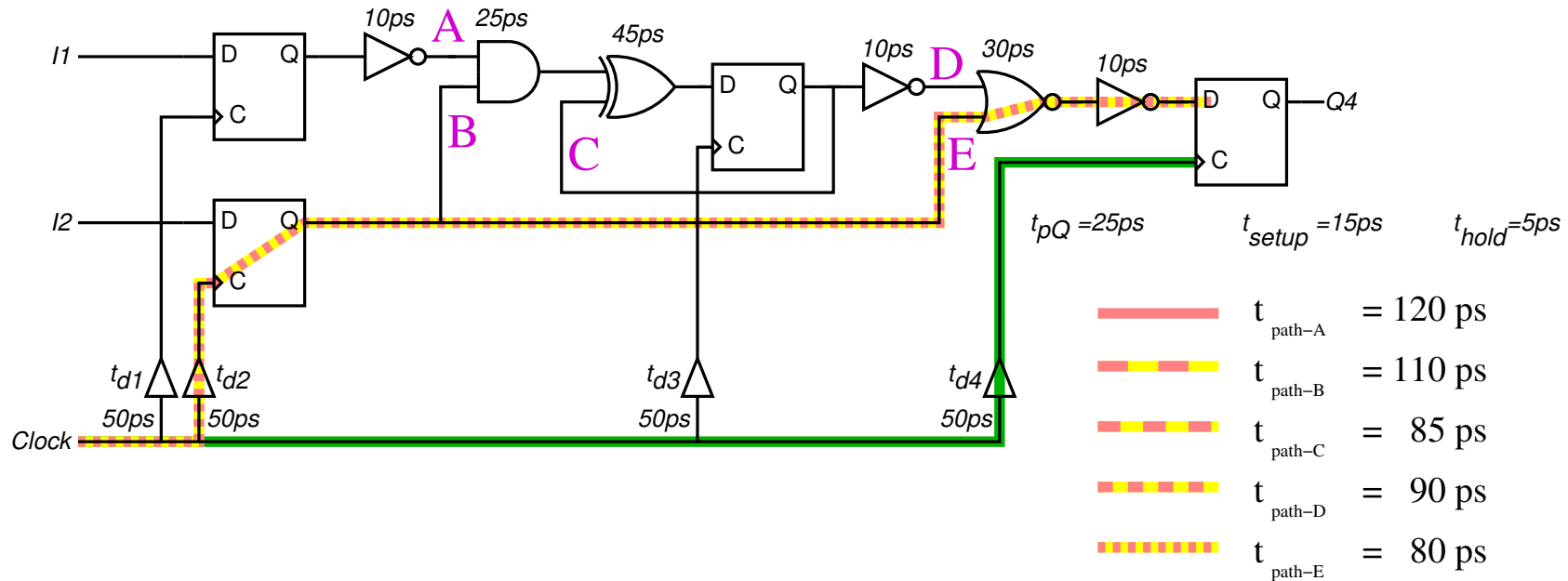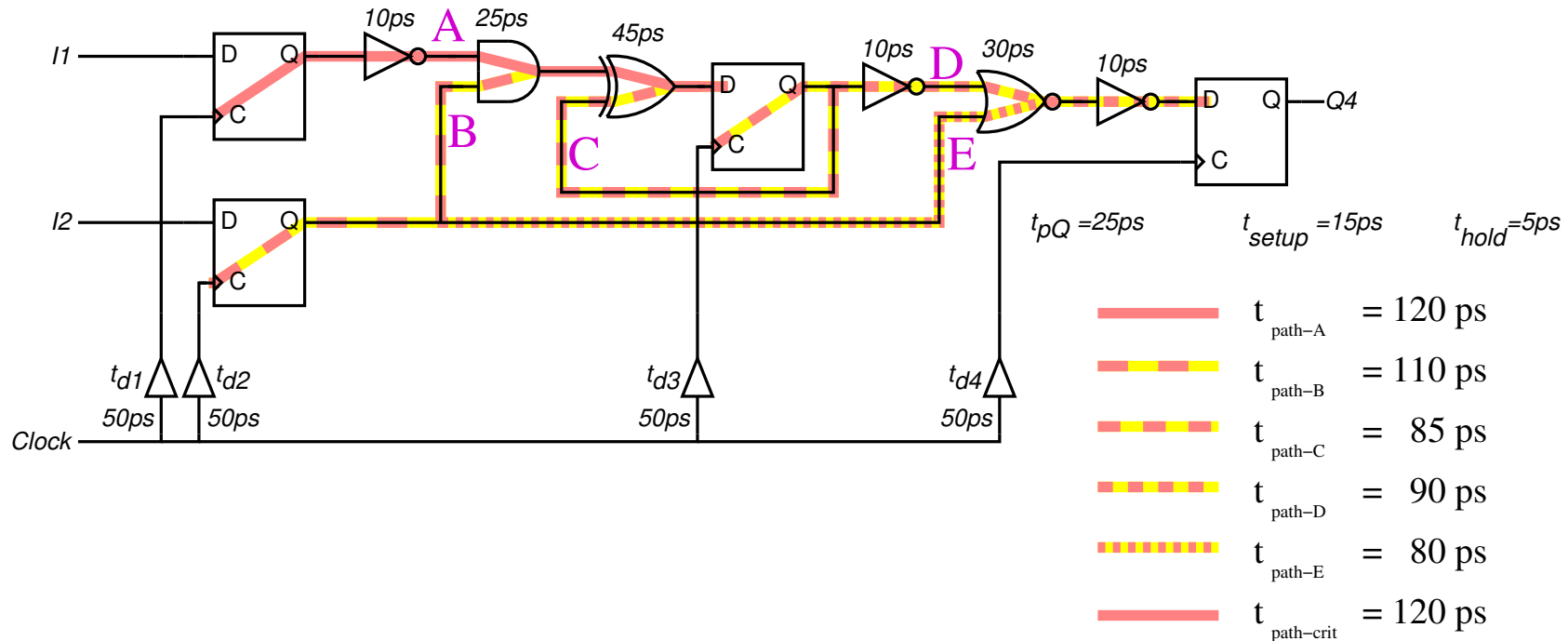
20105

Synchronous Systems - Static Timing Analysis (inc. clock skew)

- Calculate f_{max} in the presence of intentional clock skew.

- Suggest suitable values for t_{d1}, t_{d2}, t_{d3}, t_{d4}

⇒ Identify longest timing paths

$$t_{path} = t_{pQ} + t_{comb} + t_{setup} + \left(t_{d_{launch}} - t_{d_{capture}}\right)$$

20105

Synchronous Systems - Static Timing Analysis (inc. clock skew)

$t_{pQ} = 25ps$ $t_{setup} = 15ps$ $t_{hold} = 5ps$

$t_{d1} = 50$ ps $t_{d2} = 50$ ps

$t_{d3} = 50$ ps $t_{d4} = 50$ ps

$t_{comb-A} = 80$ ps

$ClockPeriod_{min} = 120$ ps

$f_{max} \cong 8.3$ GHz
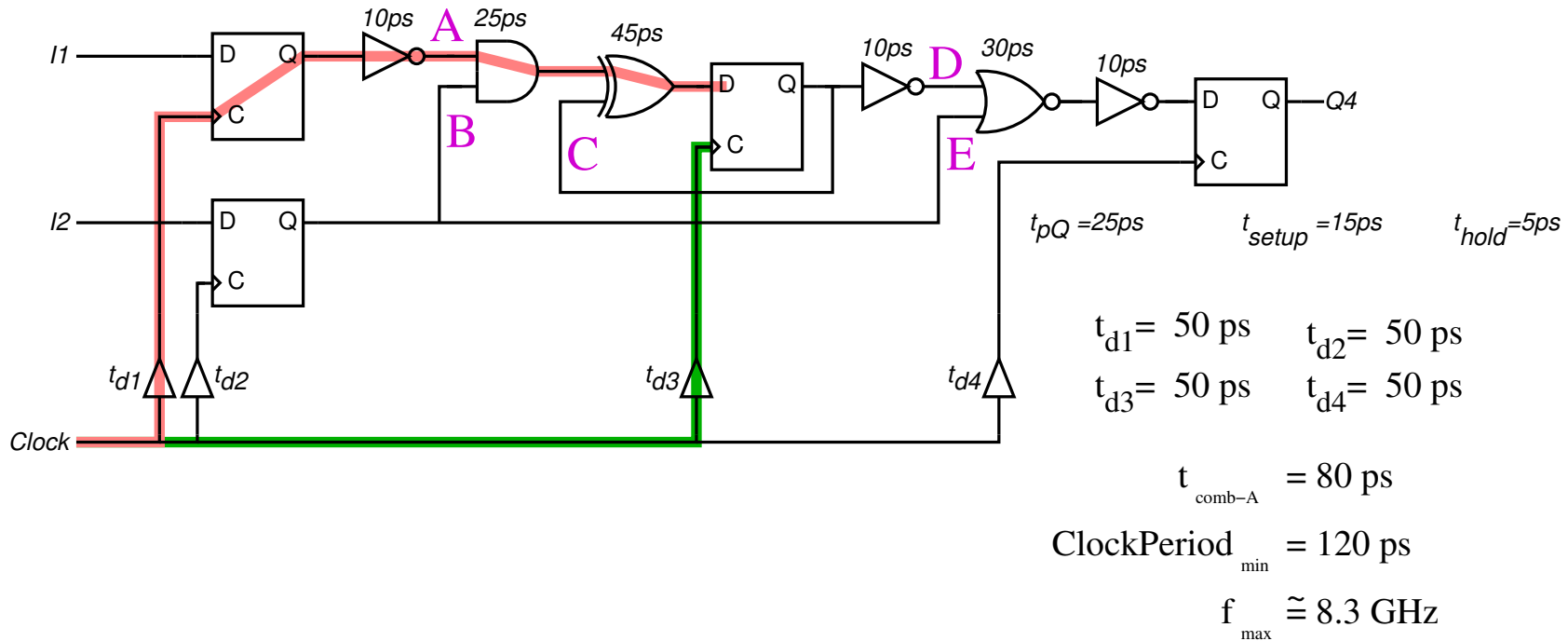
$$ClockPeriod > t_{pQ} + t_{comb-A} + t_{setup} + (t_{d1} - t_{d4})$$

$$f_{max} = \frac{1}{t_{pQ} + t_{comb-A} + t_{setup} + (t_{d1} - t_{d3})}$$

20106

10ps A 25ps

45ps

10ps D 30ps

10ps

I1 — D Q

C

B

C

D Q

C

E

D Q

C

Q4

I2 — D Q

C

t_{pQ} =25ps

t_{setup} =15ps

t_{hold}=5ps

t_{d1}

t_{d2}

t_{d3}

t_{d4}

Clock

$t_{d1}=$ ps $t_{d2}=$ ps

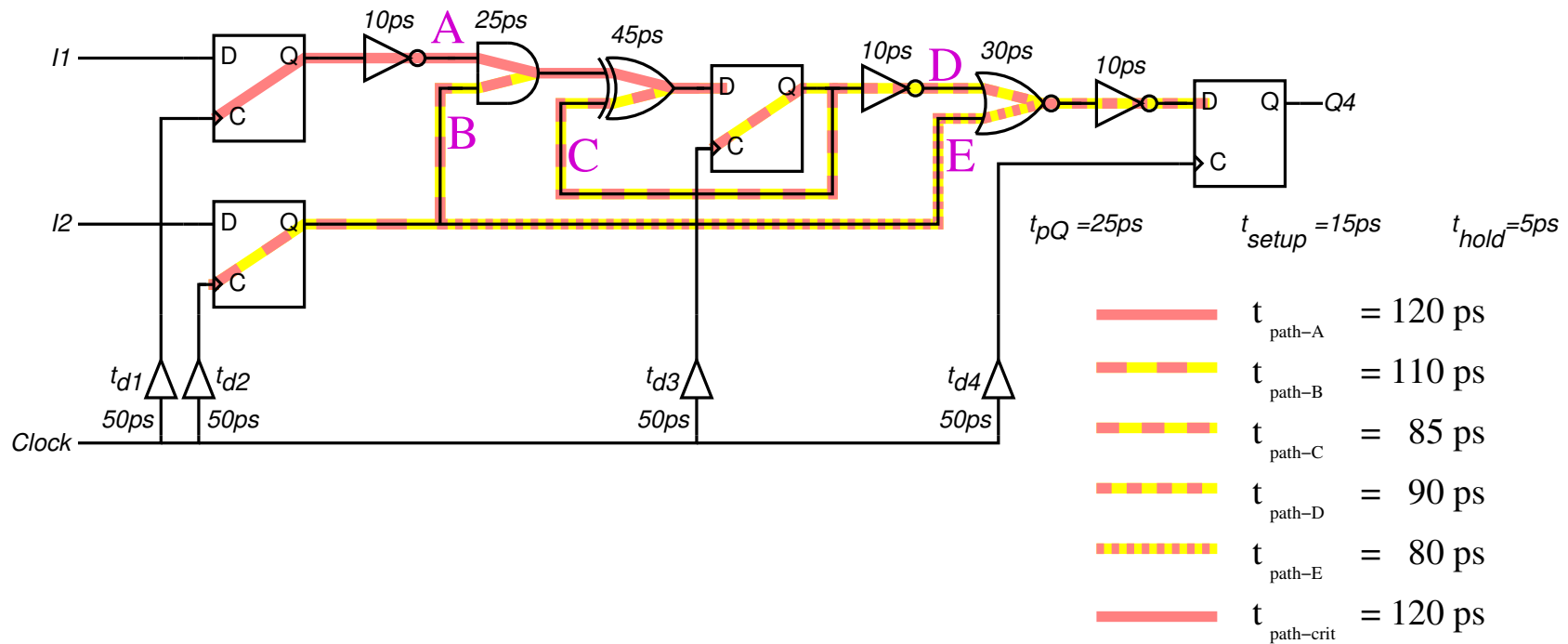$t_{d3}=$ ps $t_{d4}=$ ps
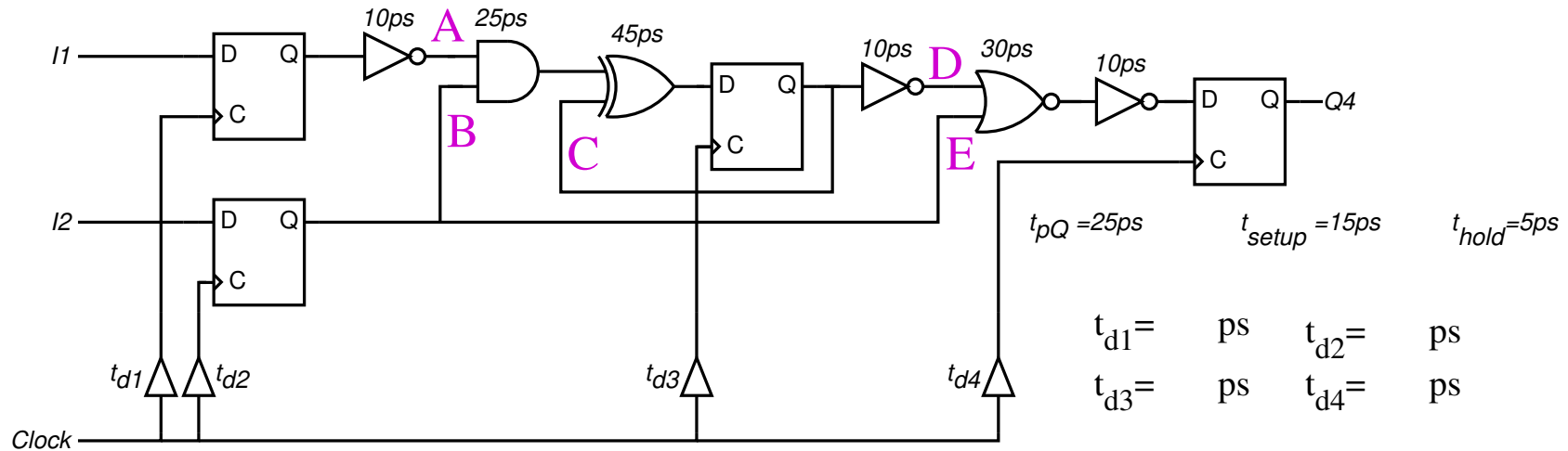
$ClockPeriod_{min} =$ ps

$f_{max} \cong$ GHz

$$ClockPeriod > t_{pQ} + t_{comb-crit} + t_{setup} + (t_{d_{launch}} - t_{d_{capture}})$$

$$f_{max} = \frac{1}{t_{pQ} + t_{comb-crit} + t_{setup} + (t_{d_{launch}} - t_{d_{capture}})}$$

20107

t_{pQ} =25ps $\quad$ t_{setup} =15ps $\quad$ t_{hold}=5ps

———	t_{path-A}	= 120 ps
– – –	t_{path-B}	= 110 ps
– – –	t_{path-C}	= 85 ps
– · – ·	t_{path-D}	= 90 ps
··········	t_{path-E}	= 80 ps
———	$t_{path-crit}$	= 120 ps

$\Rightarrow$ Initially try increasing t_{d3} by 30ps[1]

_____

[1]to ease the timing on paths A and B

20108

Synchronous Systems - Static Timing Analysis (inc. clock skew)

$t_{pQ} = 25ps$ $t_{setup} = 15ps$ $t_{hold} = 5ps$

▬▬▬▬	t_{path-A}	$= 90$ ps
▬ ▬ ▬	t_{path-B}	$= 80$ ps
▬ ▬ ▬	t_{path-C}	$= 85$ ps
▬ ▬ ▬	t_{path-D}	$= 120$ ps
▪ ▪ ▪ ▪	t_{path-E}	$= 80$ ps
▬ ▬ ▬	$t_{path-crit}$	$= 120$ ps
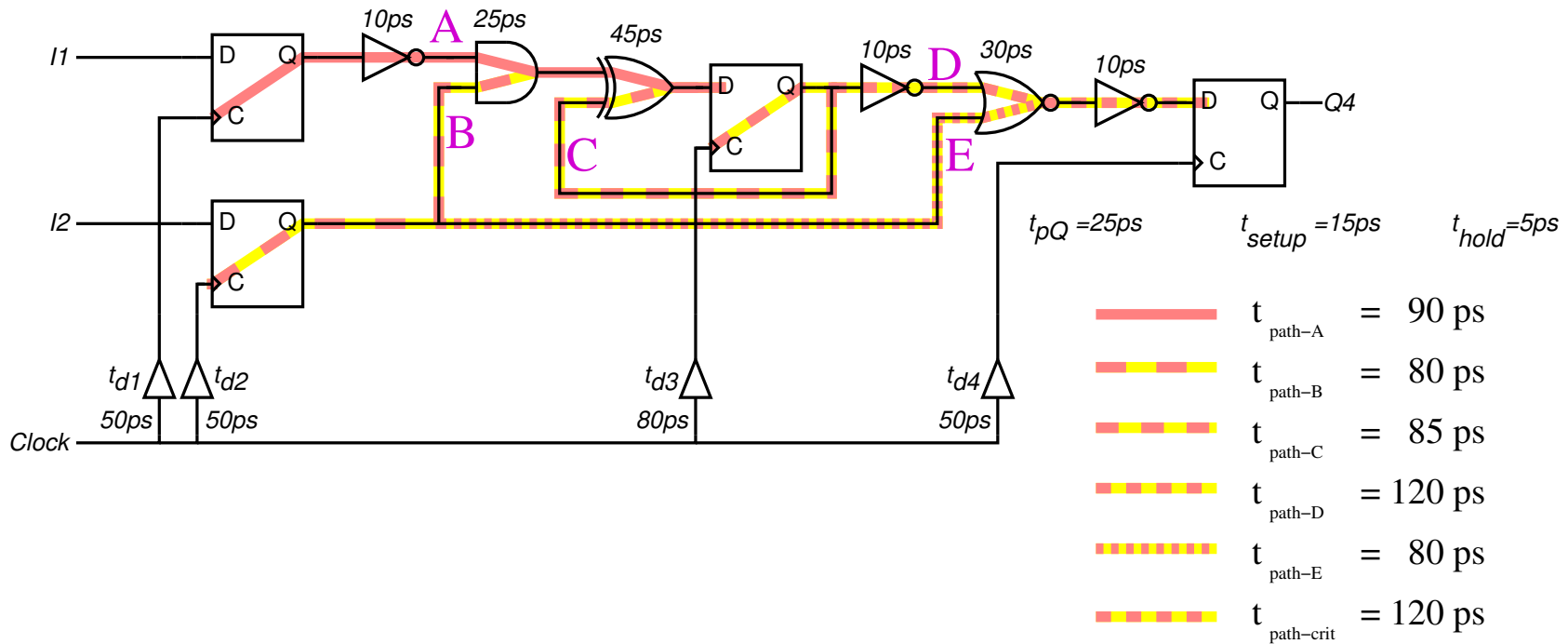
$\Rightarrow$ Increase t_{d4} by 30ps[2]

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[2]to ease the timing on path D (and E)

20109

Synchronous Systems - Static Timing Analysis (inc. clock skew)

$t_{pQ} = 25ps$	$t_{setup} = 15ps$	$t_{hold} = 5ps$

t_{path-A}	=	90 ps
t_{path-B}	=	80 ps
t_{path-C}	=	85 ps
t_{path-D}	=	90 ps
t_{path-E}	=	50 ps
$t_{path-crit}$	=	90 ps
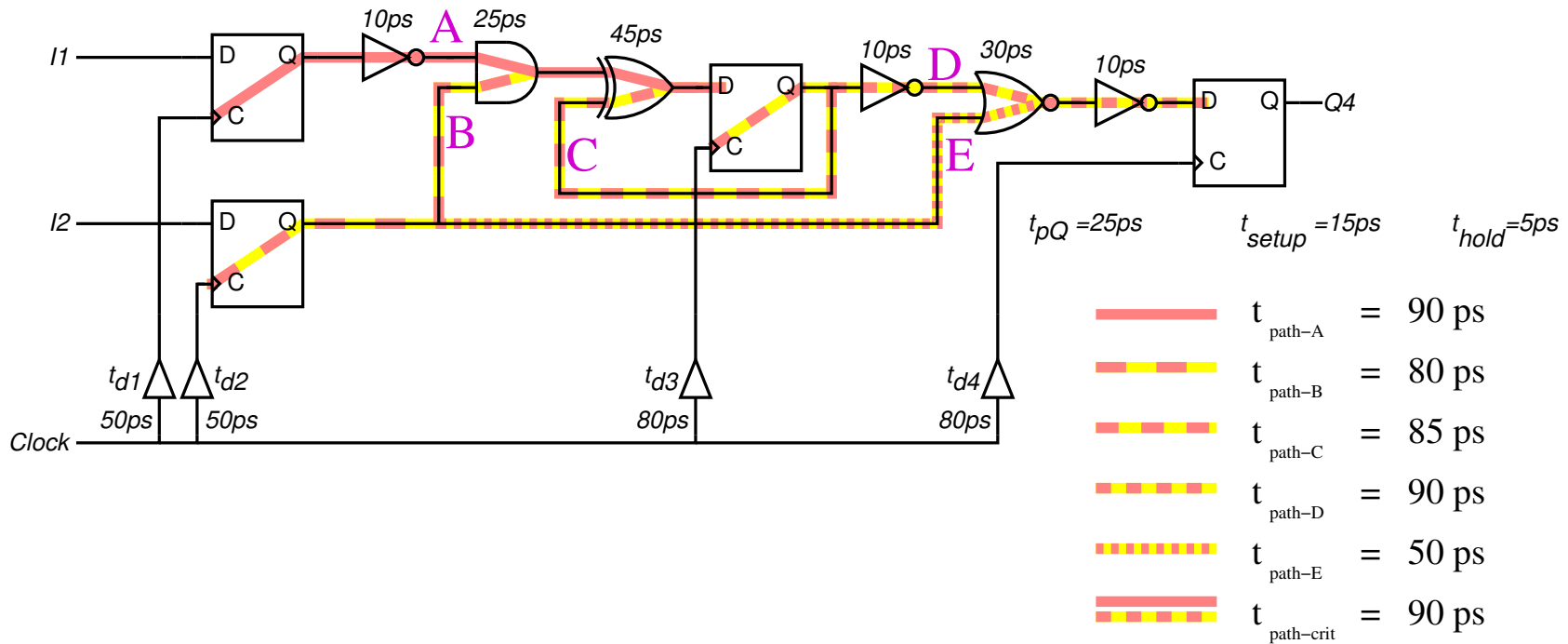
$\Rightarrow$ Increase t_{d3} by 5ps, t_{d4} by 10ps[3]

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[3]to ease the timing on paths A, (B,) D (and E)

20110

Synchronous Systems - Static Timing Analysis (inc. clock skew)

t_{path-A}	= 85 ps
t_{path-B}	= 75 ps
t_{path-C}	= 85 ps
t_{path-D}	= 85 ps
t_{path-E}	= 40 ps
$t_{path-crit}$	= 85 ps
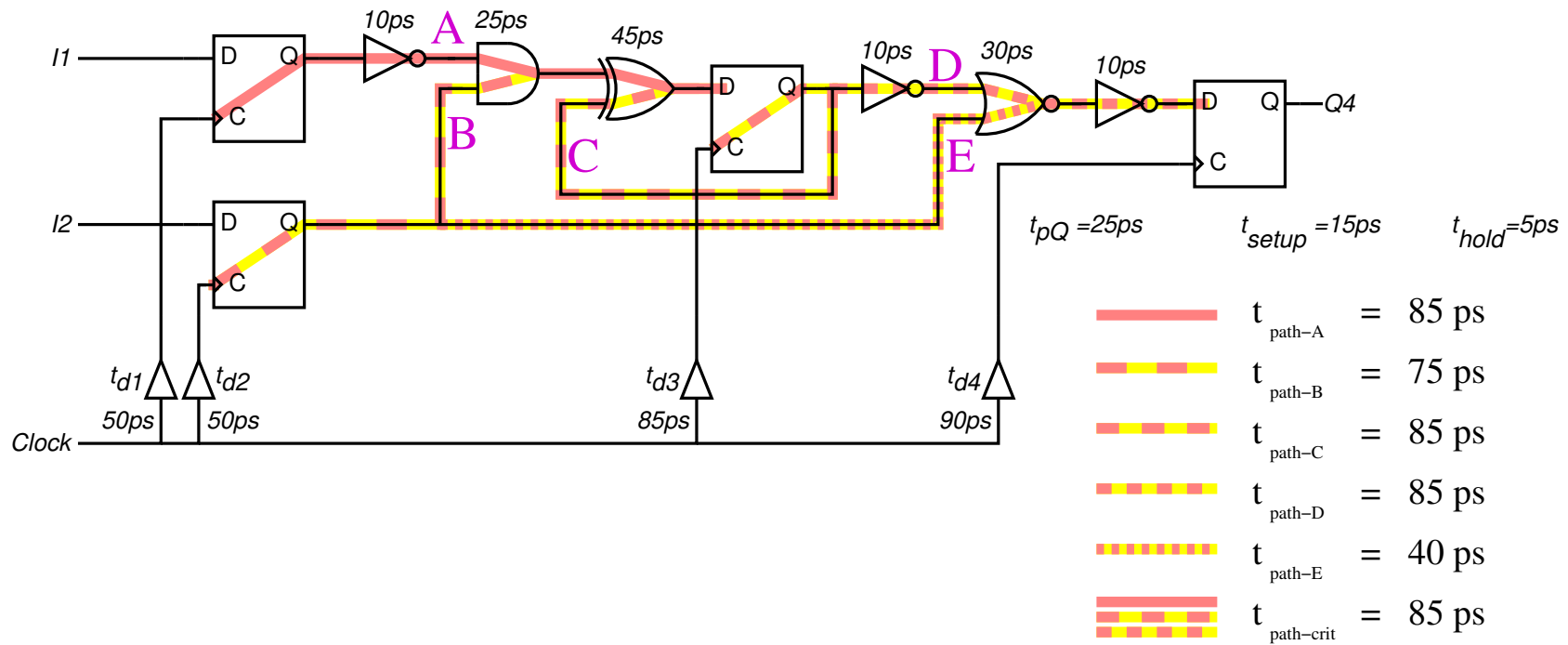
Can't now improve on t_{path-C}

20111

Synchronous Systems - Static Timing Analysis (inc. clock skew)

$t_{pQ} = 25ps$ $t_{setup} = 15ps$ $t_{hold} = 5ps$
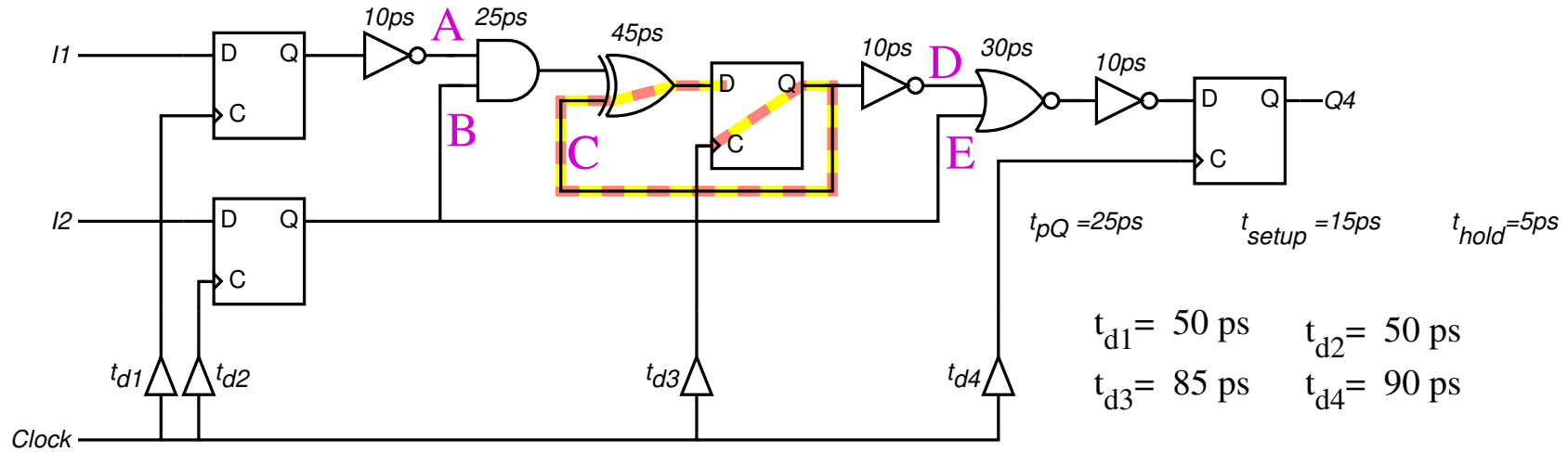
$t_{d1} = 50$ ps $t_{d2} = 50$ ps
$t_{d3} = 85$ ps $t_{d4} = 90$ ps

ClockPeriod$_{min}$ = 85 ps

f$_{max}$ $\cong$ 11.8 GHz

$$ClockPeriod > t_{pQ} + t_{comb-crit} + t_{setup} + \left(t_{d_{launch}} - t_{d_{capture}}\right)$$

$$f_{max} = \frac{1}{t_{pQ} + t_{comb-crit} + t_{setup} + \left(t_{d_{launch}} - t_{d_{capture}}\right)}$$

20112

Synchronous Systems - Static Timing Analysis (inc. clock skew)

Remember to check for hold violations

$$t_{pq} + t_{comb-A} > t_{hold} + (t_{d3} - t_{d1})$$

$$t_{pq} + t_{comb-B} > t_{hold} + (t_{d3} - t_{d2})$$

$$t_{pq} + t_{comb-C} > t_{hold}$$

$$t_{pq} + t_{comb-D} > t_{hold} + (t_{d4} - t_{d3})$$

$$t_{pq} + t_{comb-E} > t_{hold} + (t_{d4} - t_{d2})$$

In this example, path E is the worst case but even that one still has 20ps of slack before there would be a hold violation:

$$25ps + 40ps > 5ps + (90ps - 50ps)$$

20113