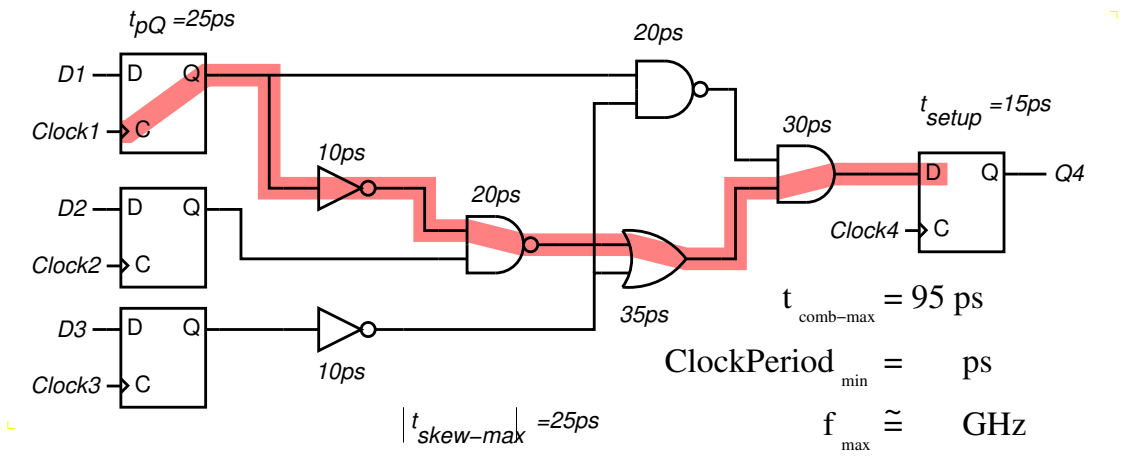
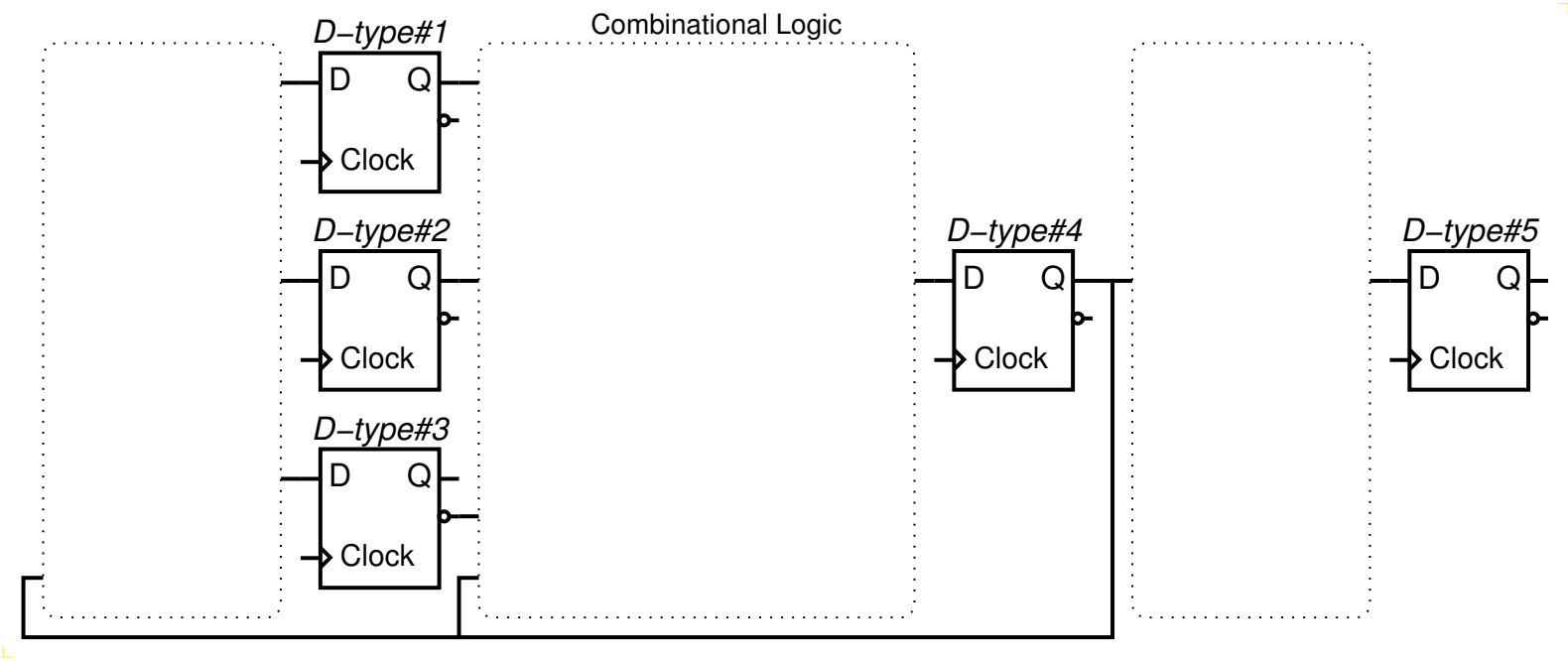


- What is the maximum operating frequency of the circuit if the clock skew is no more than 25ps?
- What is the maximum clock skew that can be tolerated before we have a potential hold violation?

Synchronous Systems - Static Timing Analysis (inc. clock skew)

Critical Path

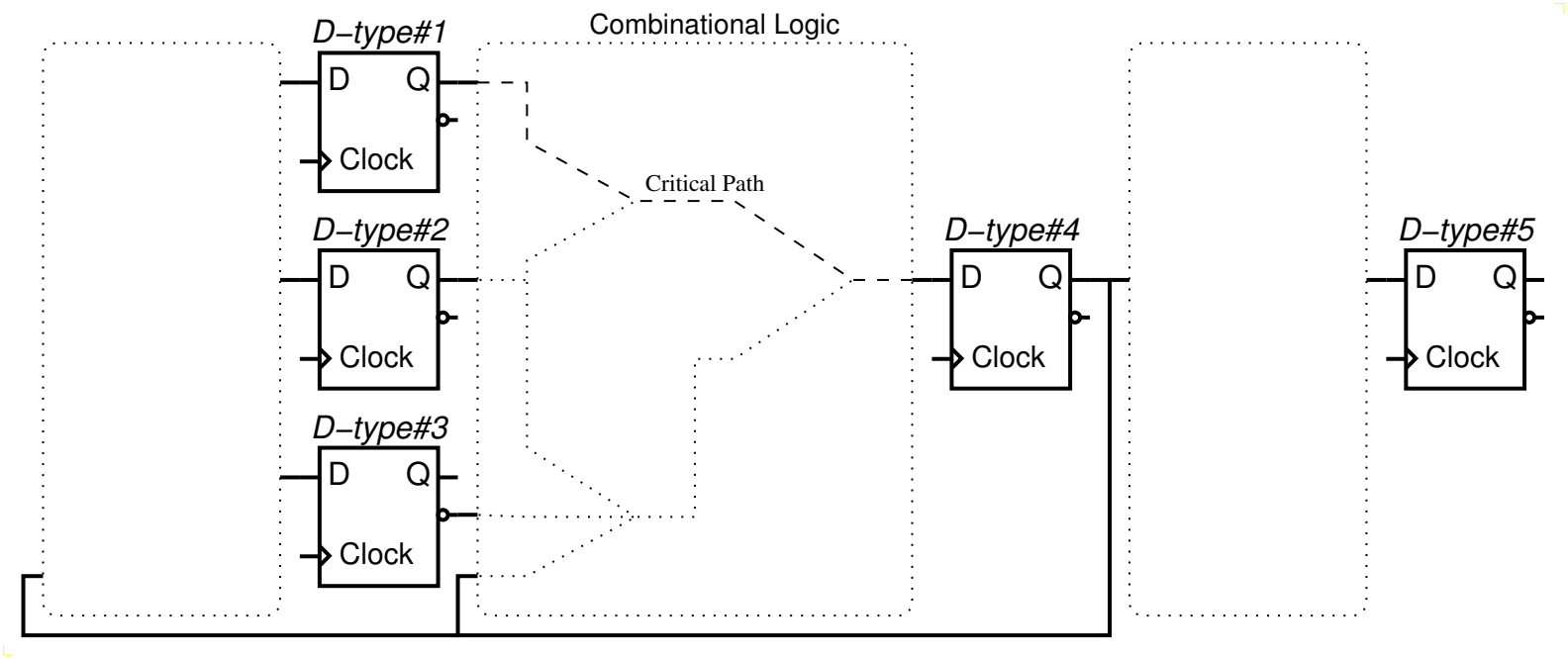


- To avoid a setup violation:

$$ClockPeriod > t_{pQ} + t_{critical\_path} + t_{setup} + t_{skew}$$

Synchronous Systems - Static Timing Analysis (inc. clock skew)

Critical Path

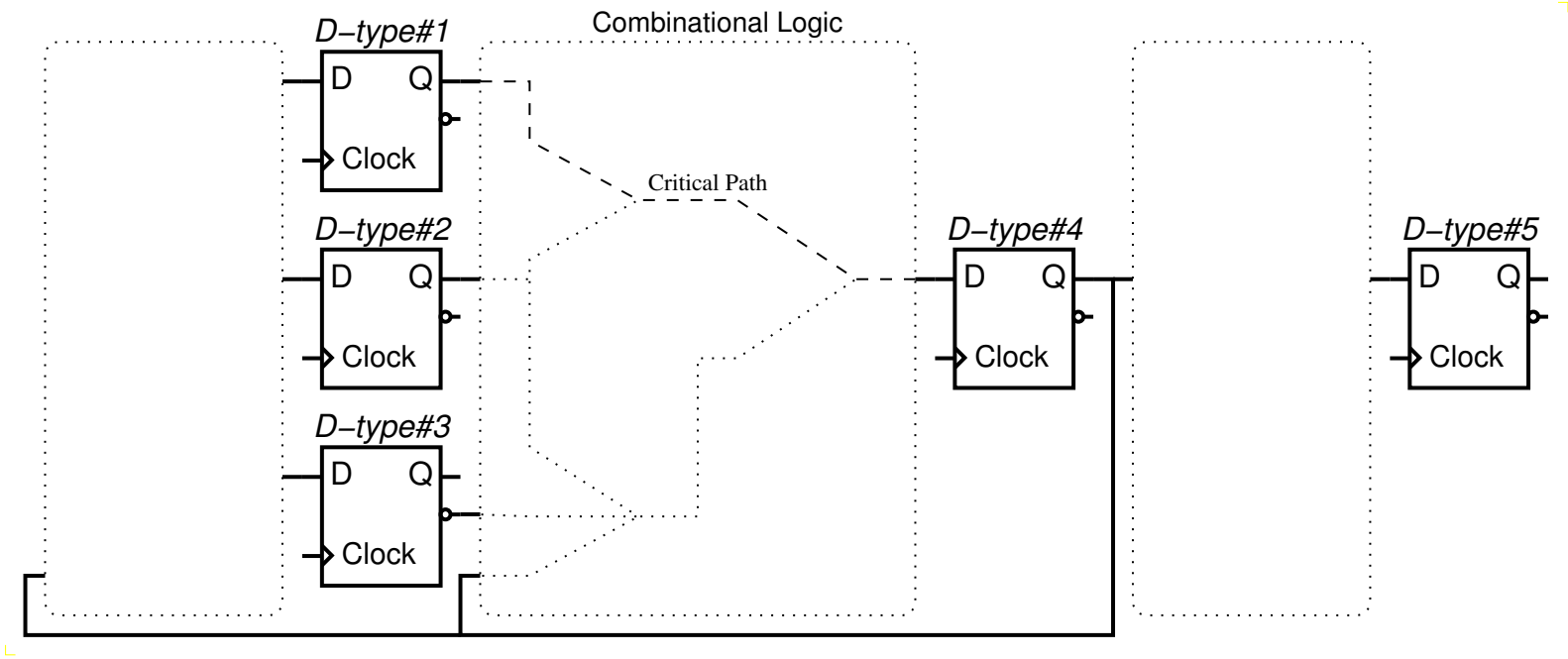


- To avoid a setup violation:

$$ClockPeriod > t_{pQ} + t_{critical\_path} + t_{setup} + (t_{d1} - t_{d4})$$

Synchronous Systems - Static Timing Analysis (inc. clock skew)

Critical Path

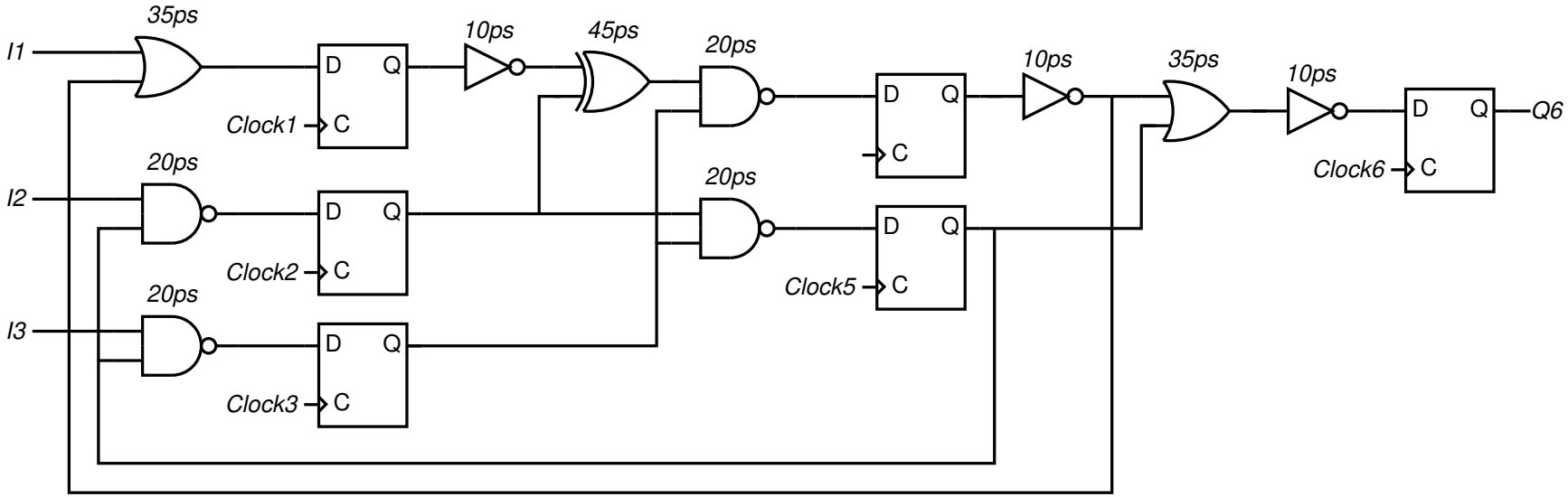


$$ClockPeriod > t_{pQ} + t_{critical\_path} + t_{setup} + (t_{d1} - t_{d4})$$

- If we can control the skew (e.g. by increasing t_{d4}), we can ease the timing constraint.[1]

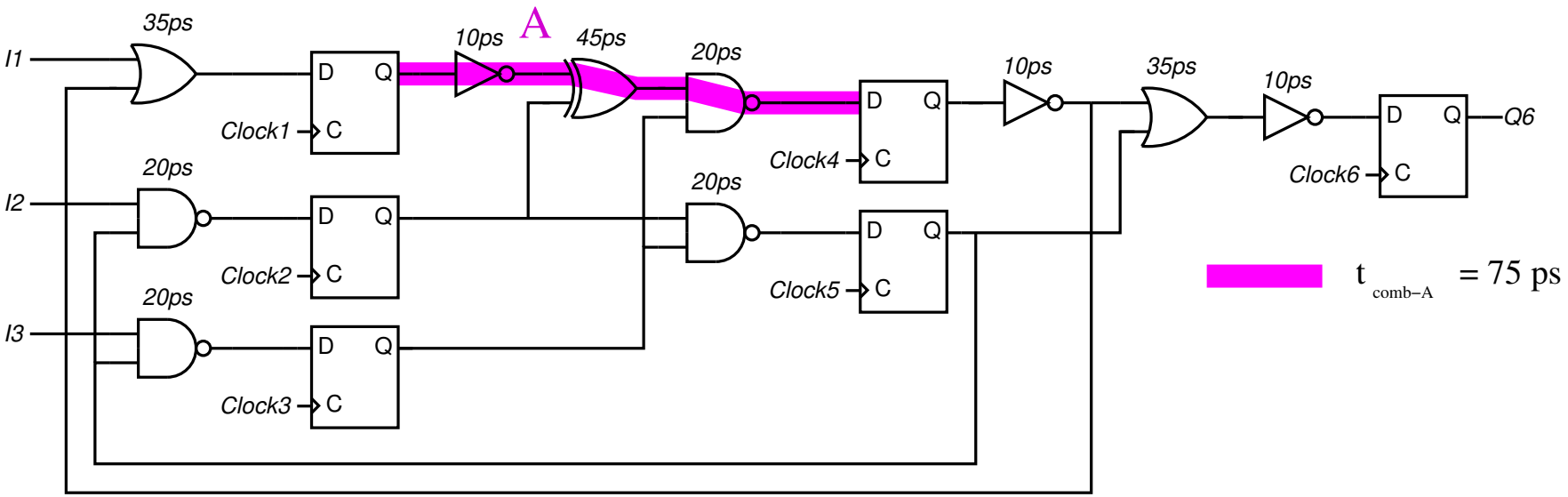
[1] this may result in the critical path moving to another part of the circuit

Synchronous Systems - Static Timing Analysis (inc. clock skew)



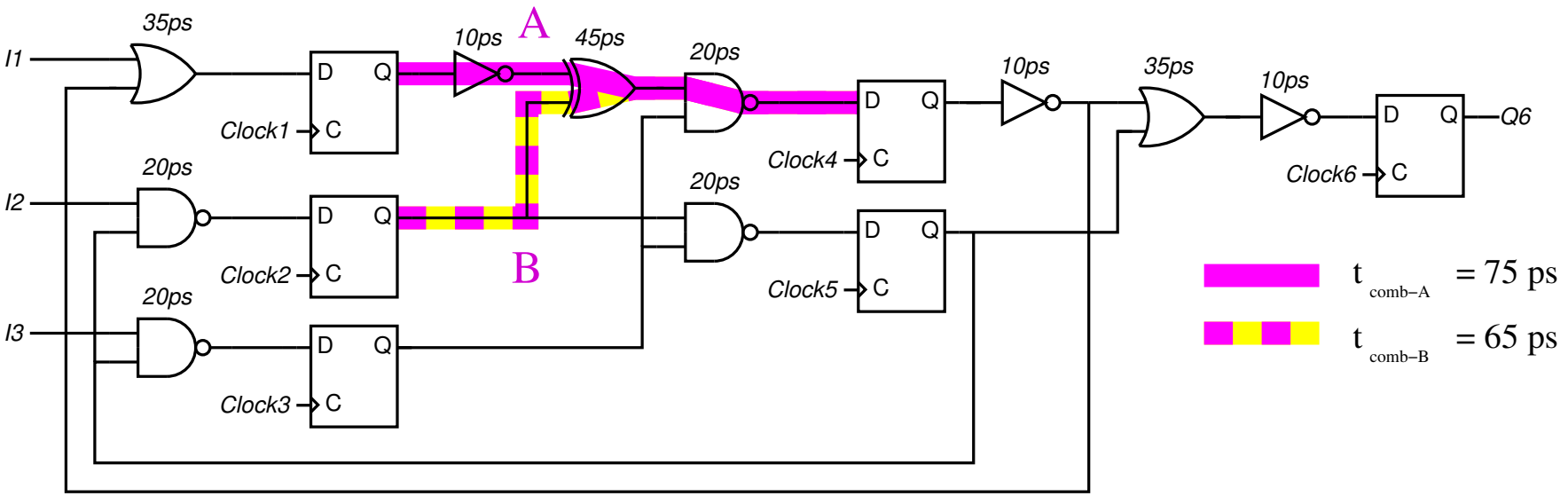
- Identify longest combinational paths

Synchronous Systems - Static Timing Analysis (inc. clock skew)



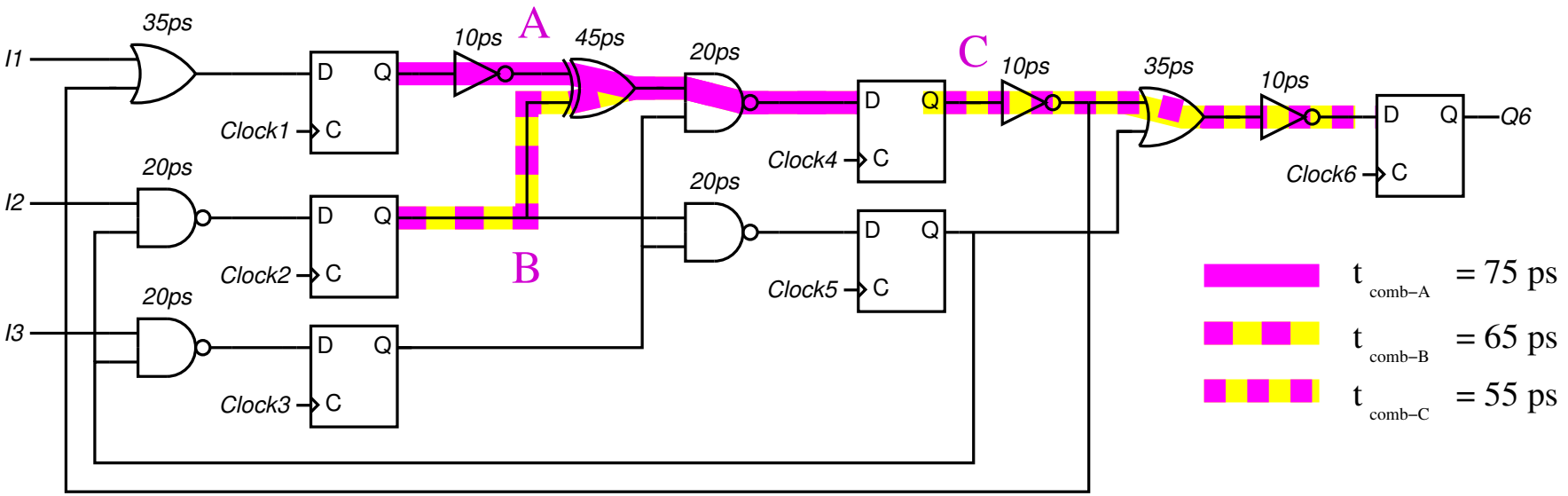
- Identify longest combinational paths

Synchronous Systems - Static Timing Analysis (inc. clock skew)



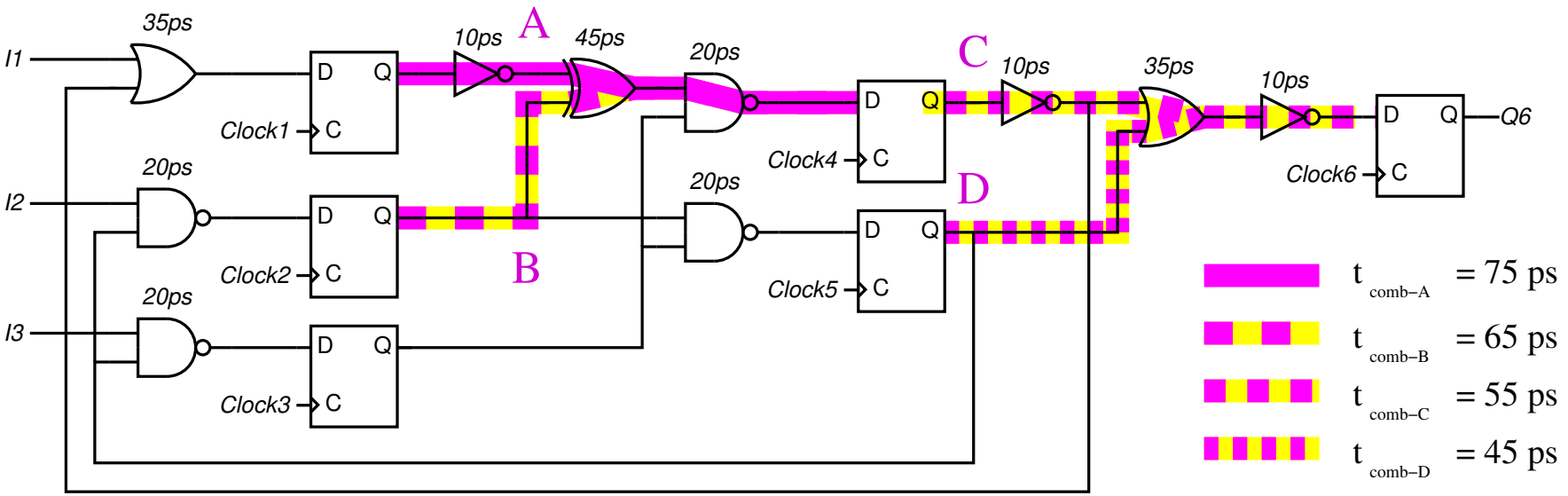
- Identify longest combinational paths

Synchronous Systems - Static Timing Analysis (inc. clock skew)



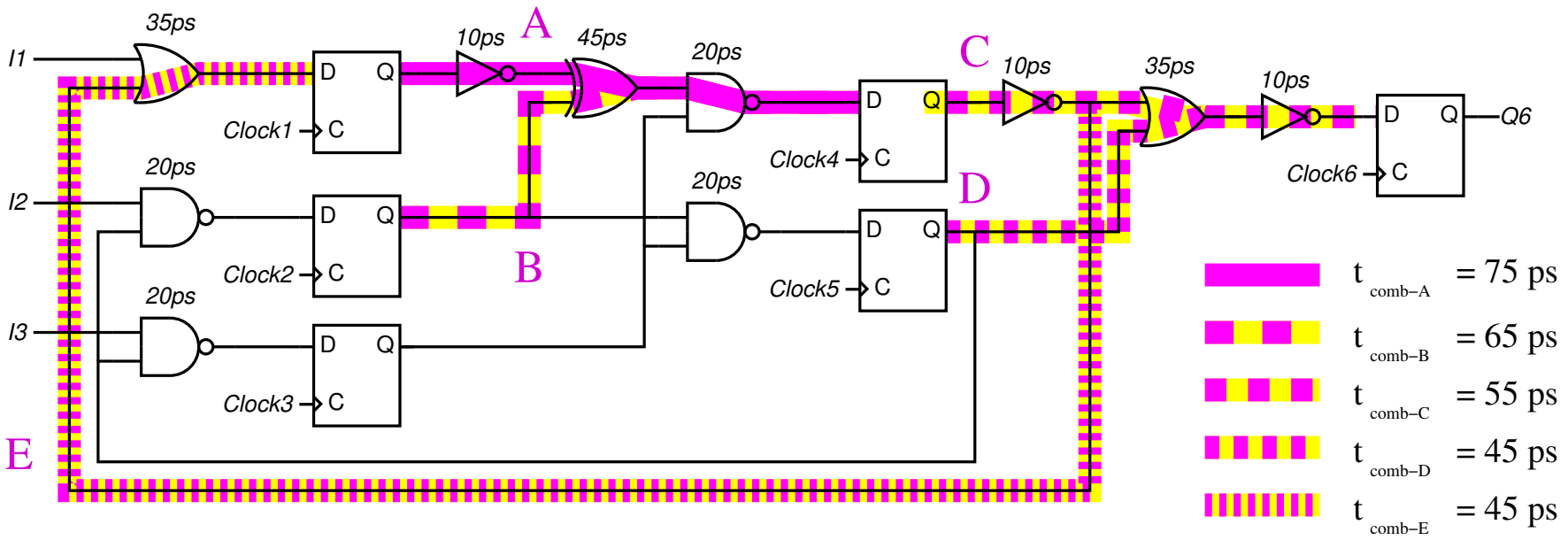
- Identify longest combinational paths

Synchronous Systems - Static Timing Analysis (inc. clock skew)



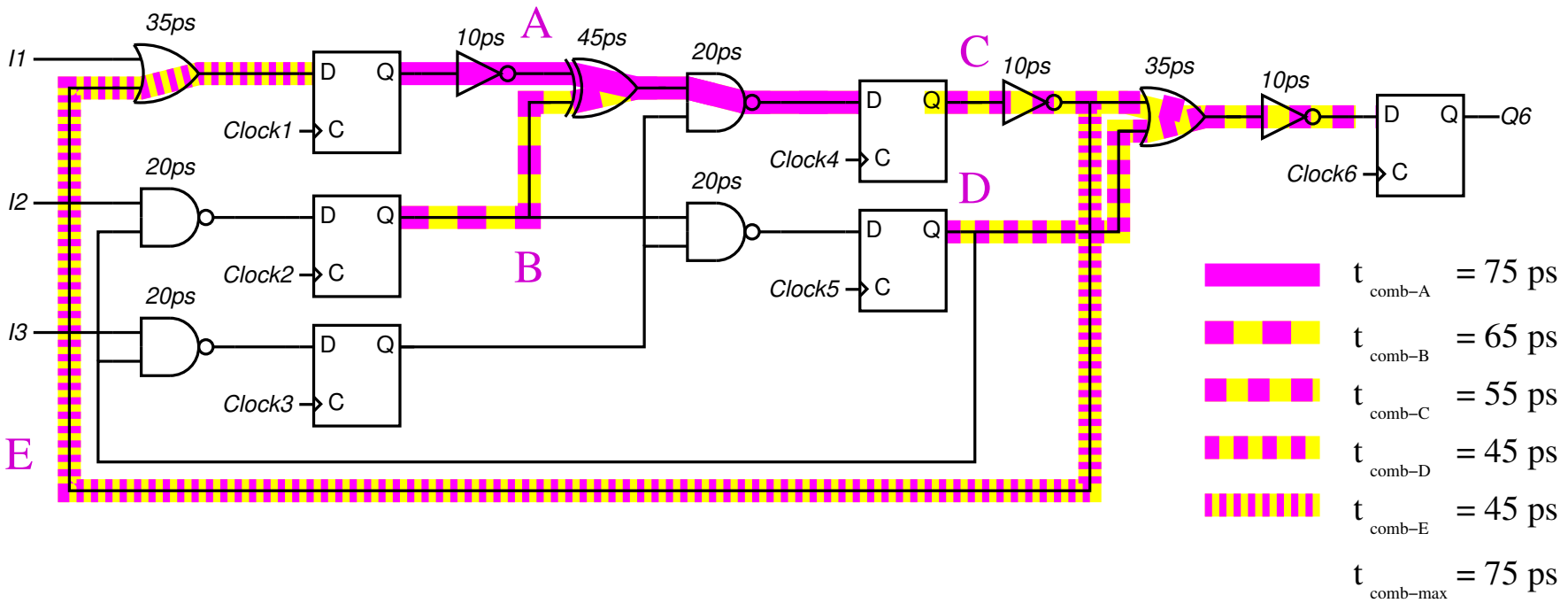
- Identify longest combinational paths

Synchronous Systems - Static Timing Analysis (inc. clock skew)



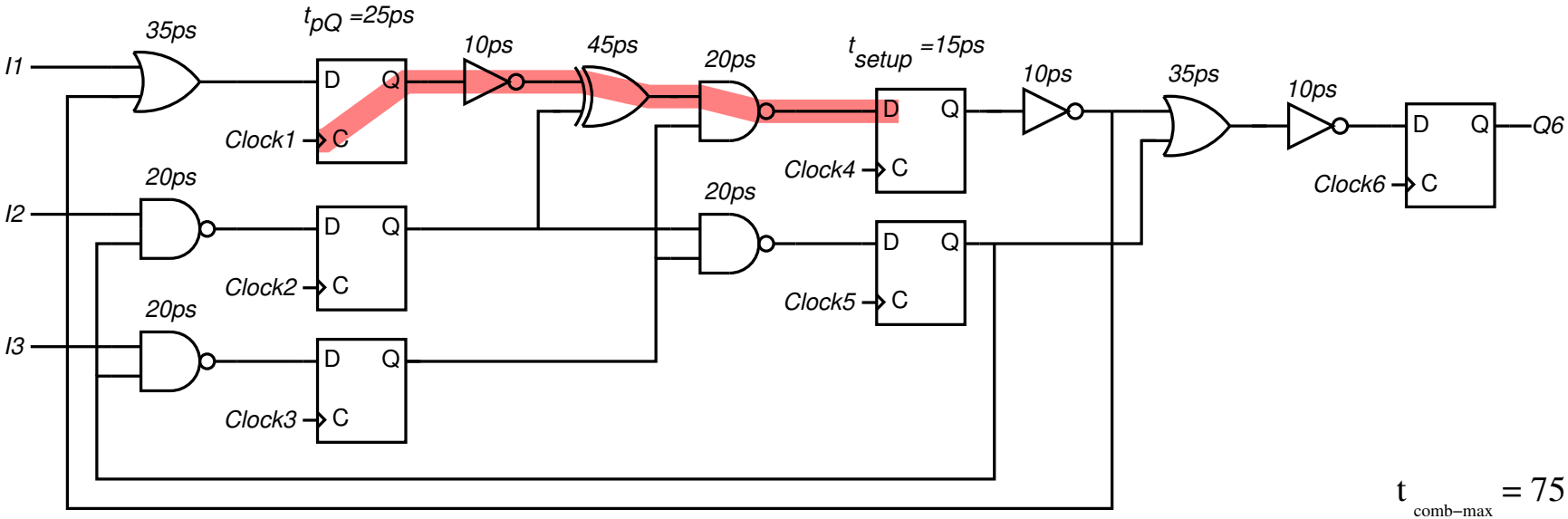
- Identify longest combinational paths

Synchronous Systems - Static Timing Analysis (inc. clock skew)



- Identify longest combinational paths

Synchronous Systems - Static Timing Analysis (inc. clock skew)



$t_{comb-max}$ = 75 ps

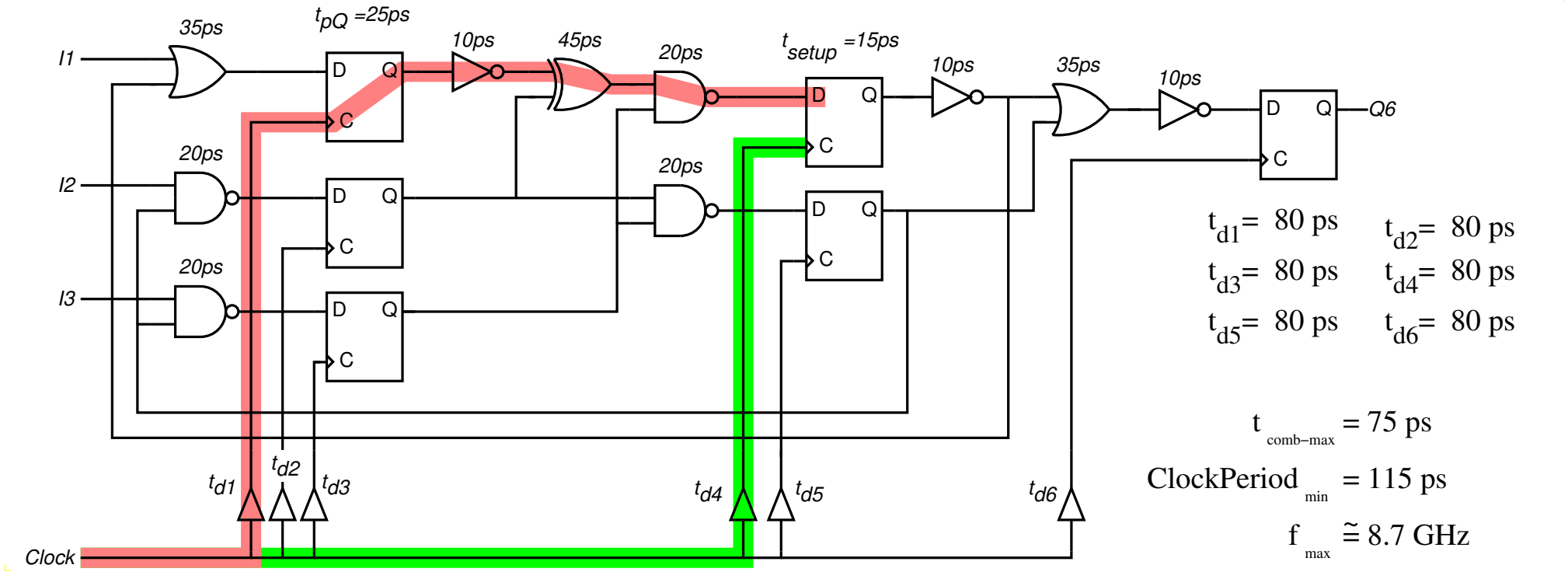
$ClockPeriod_{min}$ = 115 ps

f_{max} ≅ 8.7 GHz

$$ClockPeriod > t_{pQ} + t_{comb-max} + t_{setup} + (t_{d1} - t_{d4})$$

$$f_{max} = \frac{1}{t_{pQ} + t_{comb-max} + t_{setup} + (t_{d1} - t_{d4})}$$

Synchronous Systems - Static Timing Analysis (inc. clock skew)



t_{d1} = 80 ps t_{d2} = 80 ps

t_{d3} = 80 ps t_{d4} = 80 ps

t_{d5} = 80 ps t_{d6} = 80 ps

$t_{comb-max}$ = 75 ps

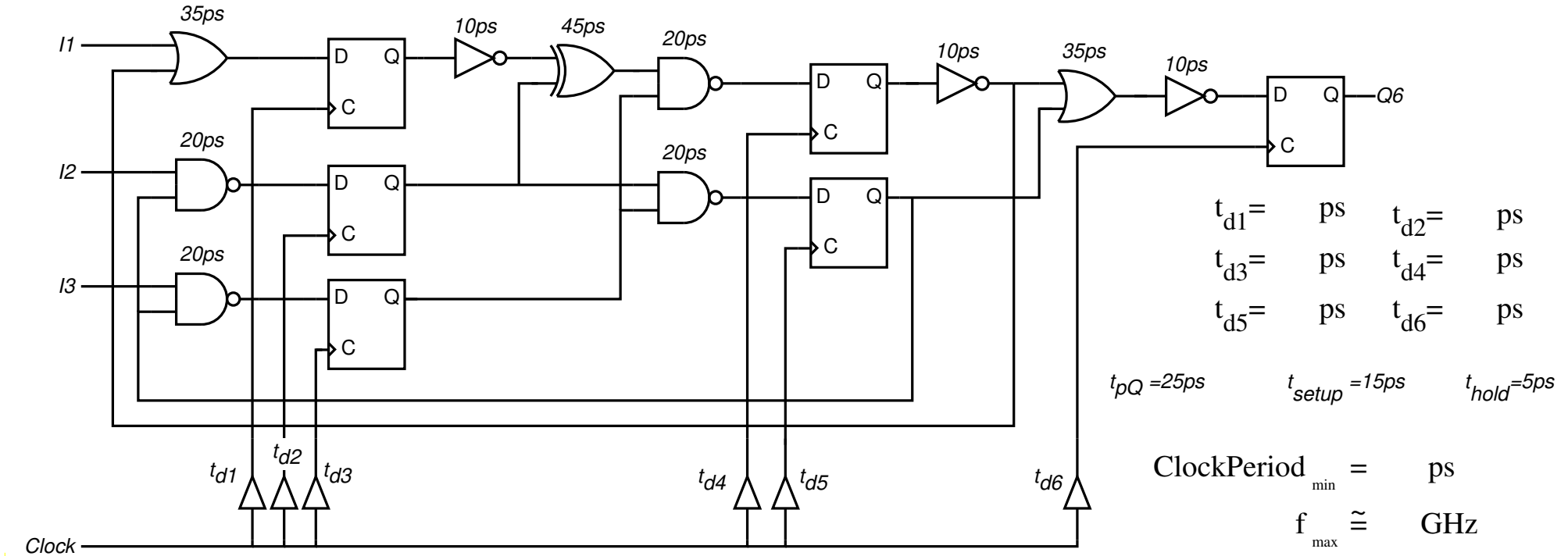
$ClockPeriod_{min}$ = 115 ps

f_{max} ≅ 8.7 GHz

$$ClockPeriod > t_{pQ} + t_{comb-max} + t_{setup} + (t_{d1} - t_{d4})$$

$$f_{max} = \frac{1}{t_{pQ} + t_{comb-max} + t_{setup} + (t_{d1} - t_{d4})}$$

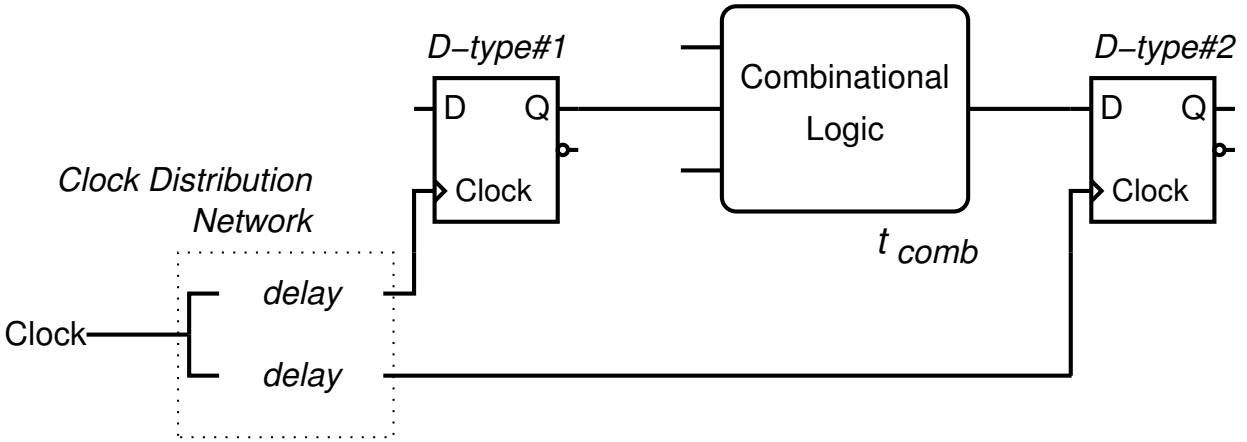
Synchronous Systems - Static Timing Analysis (inc. clock skew)



$$ClockPeriod > t_{pQ} + t_{comb-crit} + t_{setup} + (t_{ds} - t_{dd})$$

$$f_{max} = \frac{1}{t_{pQ} + t_{comb-crit} + t_{setup} + (t_{ds} - t_{dd})}$$

Synchronous Systems - Jitter



- Jitter

  Jitter is the cycle-by-cycle variation in the arrival time of the clock.

- Caused by
  - Variation in frequency/phase of clock source[2]
  - Power supply noise affecting clock distribution
  - Cross-talk affecting clock distribution
- Jitter may cause unexpected timing violations

[2]primary clock source or Phase-Locked Loop (PLL)