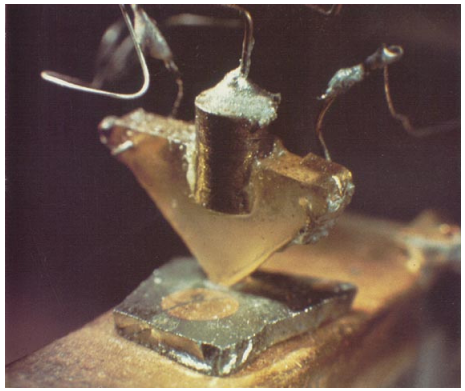
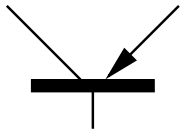
1947 Point Contact transistor

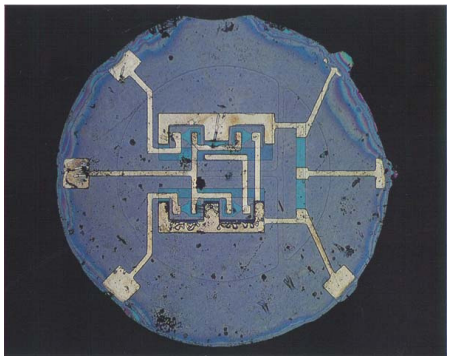


Source: Bell Labs

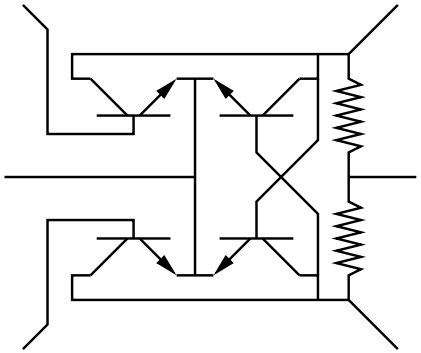


1961 Fairchild Bipolar RTL RS Flip–Flop

(4 Transistors)

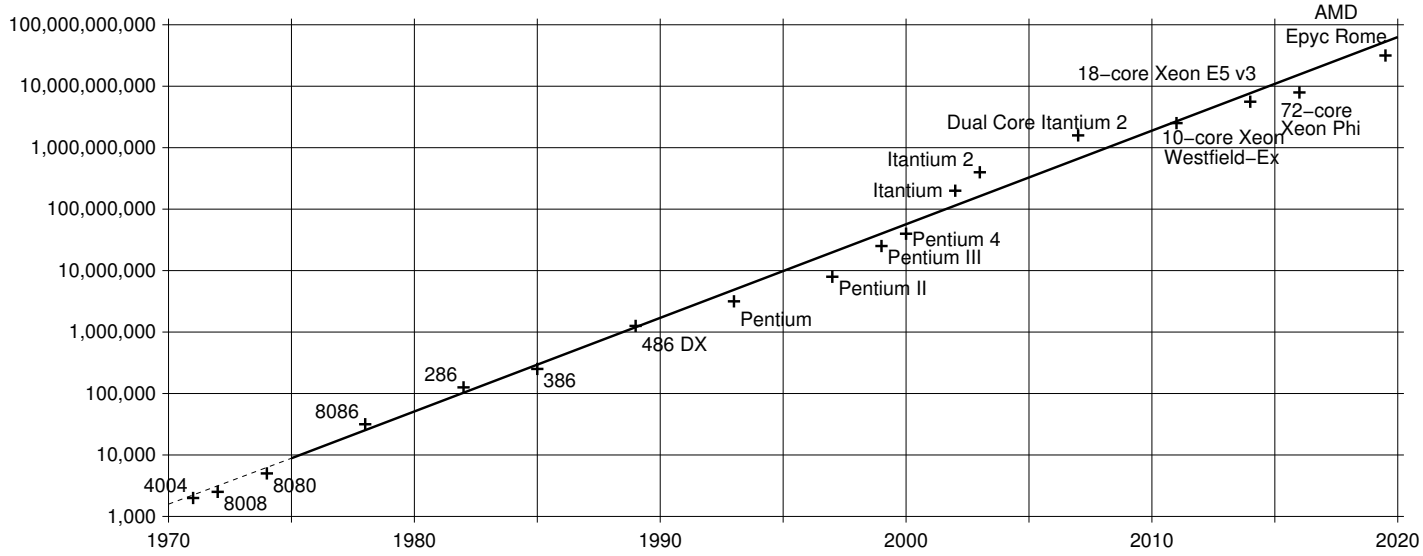


Source: Fairchild



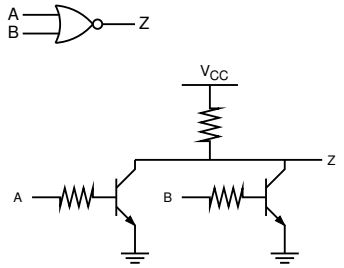
Moore's Law (1965) Number of components has doubled every year and will continue to do so until 1975

Moore's Law (1975) Number of components will double every two years

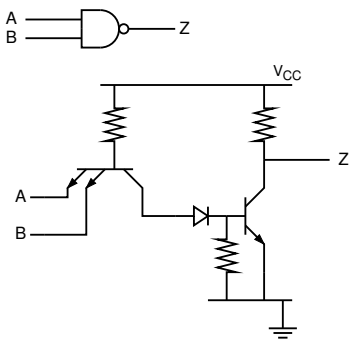


Self–fulfilling Prophecy

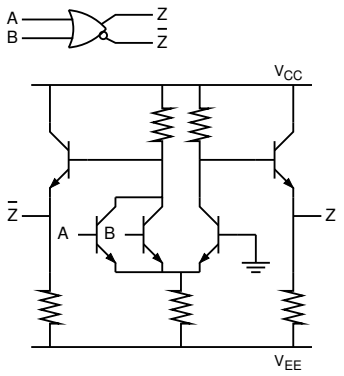
RTL NOR Gate



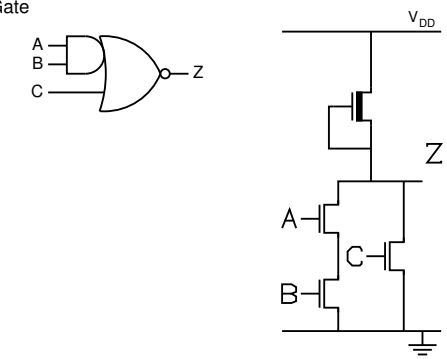
TTL NAND Gate



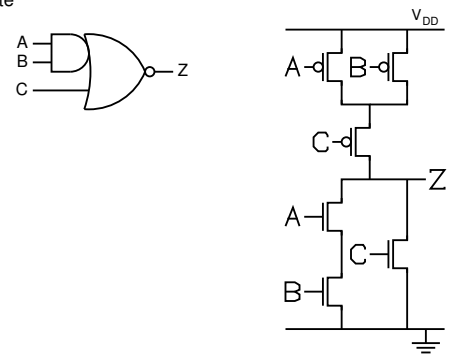
ECL OR/NOR Gate



NMOS Compund Gate



CMOS Compund Gate



- Bipolar Transitors with Resistors - MSI/LSI

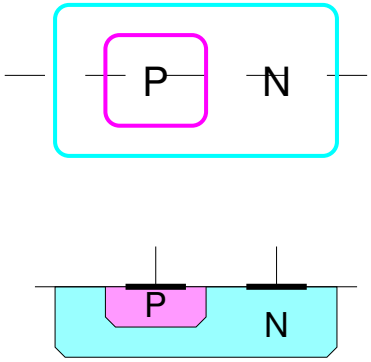
  RTL - NOR TTL - NAND ECL - OR/NOR

- MOS Transistors (no resistors) - VLSI

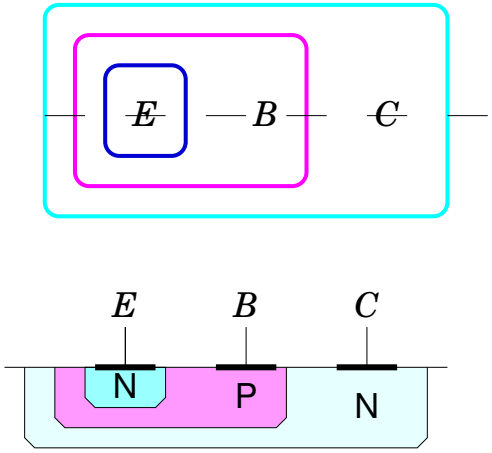
  NMOS CMOS - No static power!

Both allow construction of NOR, NAND & Compound gate (always inverting)

Diode

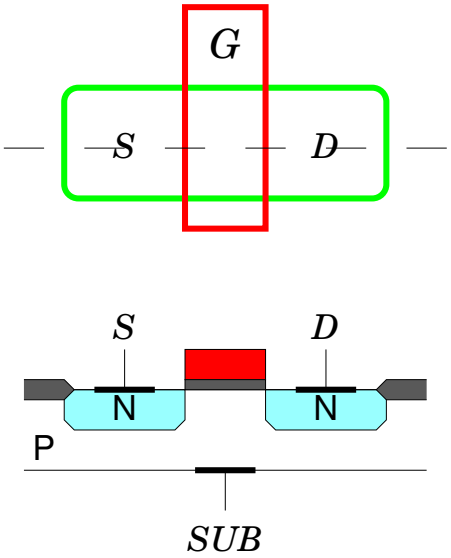


NPN Transistor

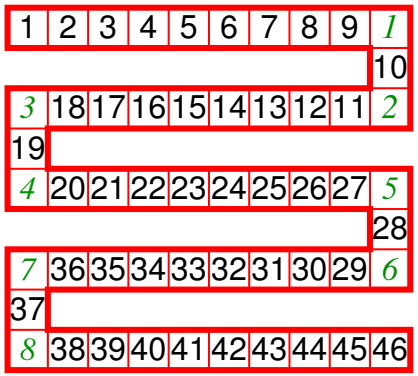


NMOS Enhancement transistor

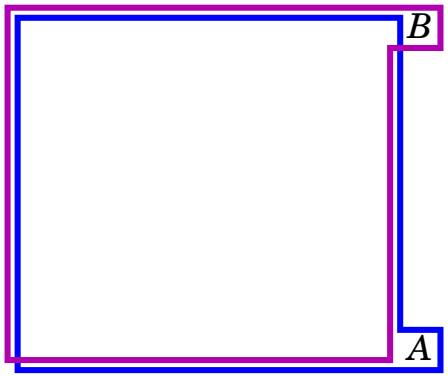
NMOS Process

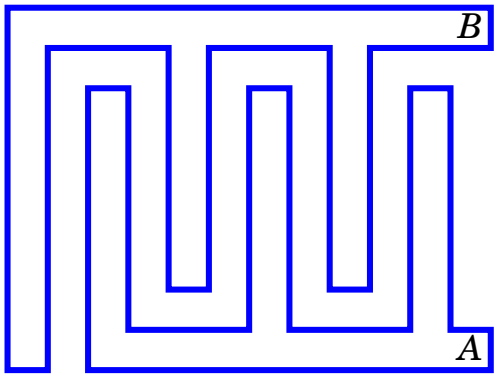


Resistor



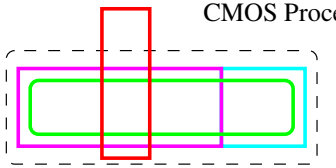
Capacitors



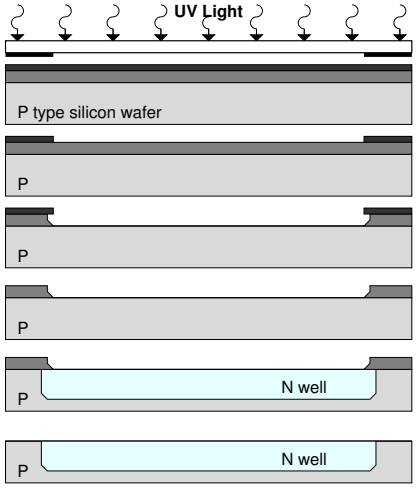


PMOS Enhancement transistor

CMOS Process

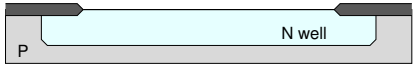


N Well

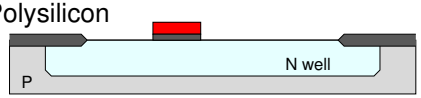


many steps for a single mask

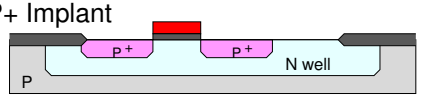
Active Area



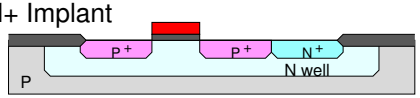
Polysilicon



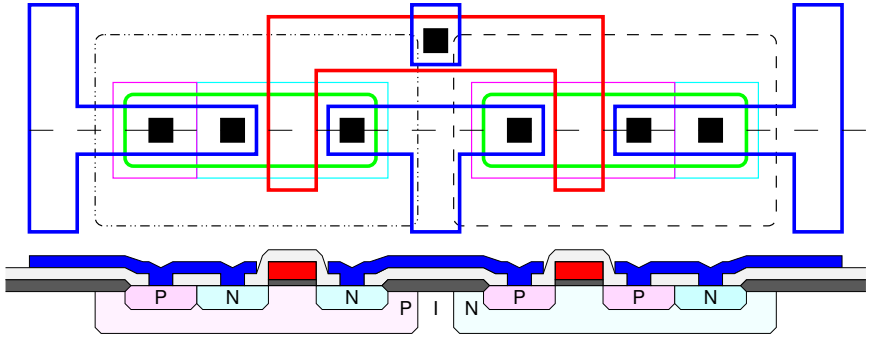
P+ Implant



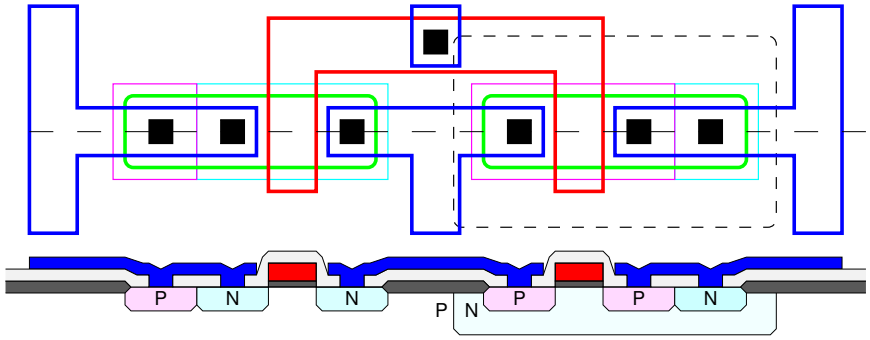
N+ Implant



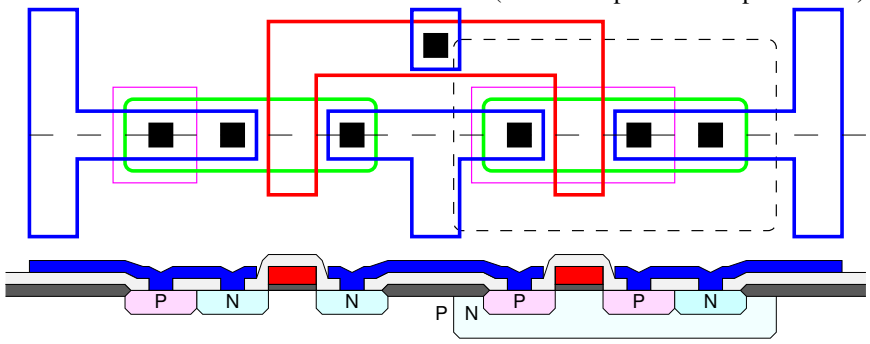
CMOS Inverter Twin Tub CMOS Process



CMOS Inverter N–Well CMOS Processs (with explicit N+ implant mask)

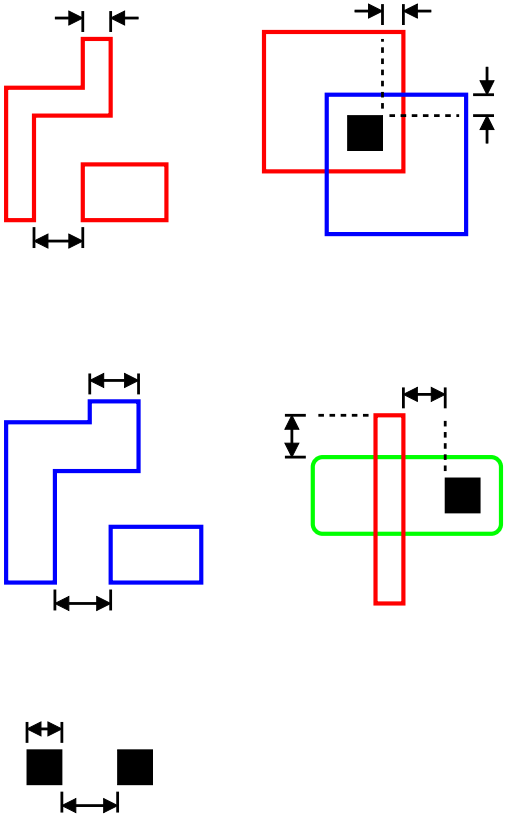


CMOS Inverter N–Well CMOS Processs (without explicit N+ implant mask)

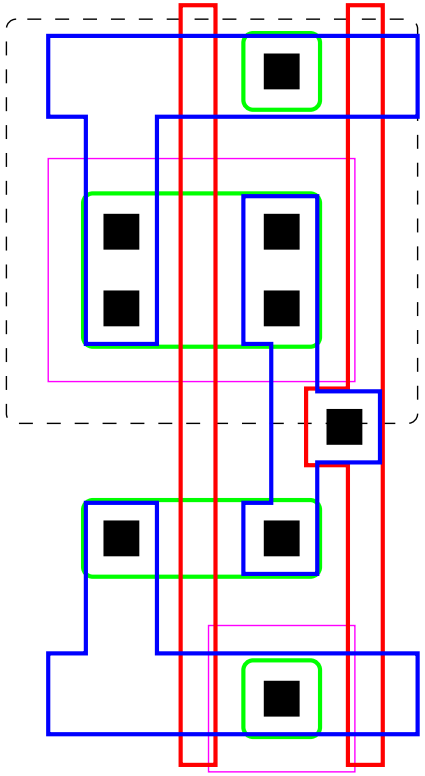


Features may be determined by a number of masks
e.g. NMOS source drain: ActiveArea AND NOT(NWell OR Poly OR PImplant)

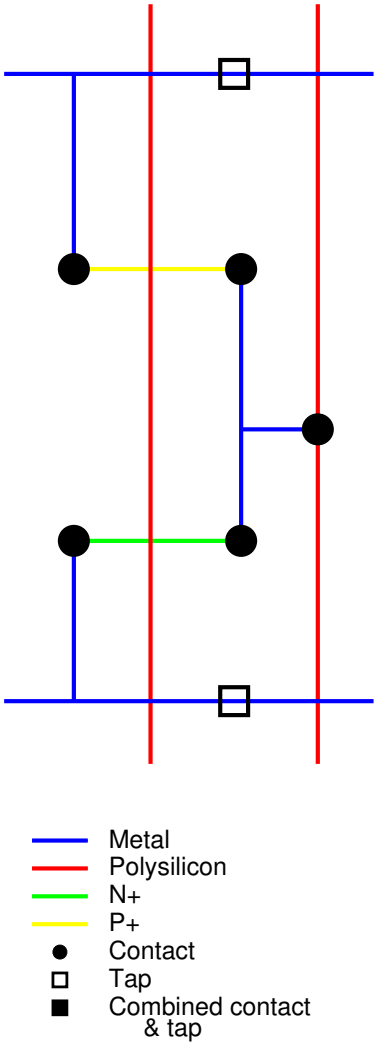
Design Rules – width, separation, overlap



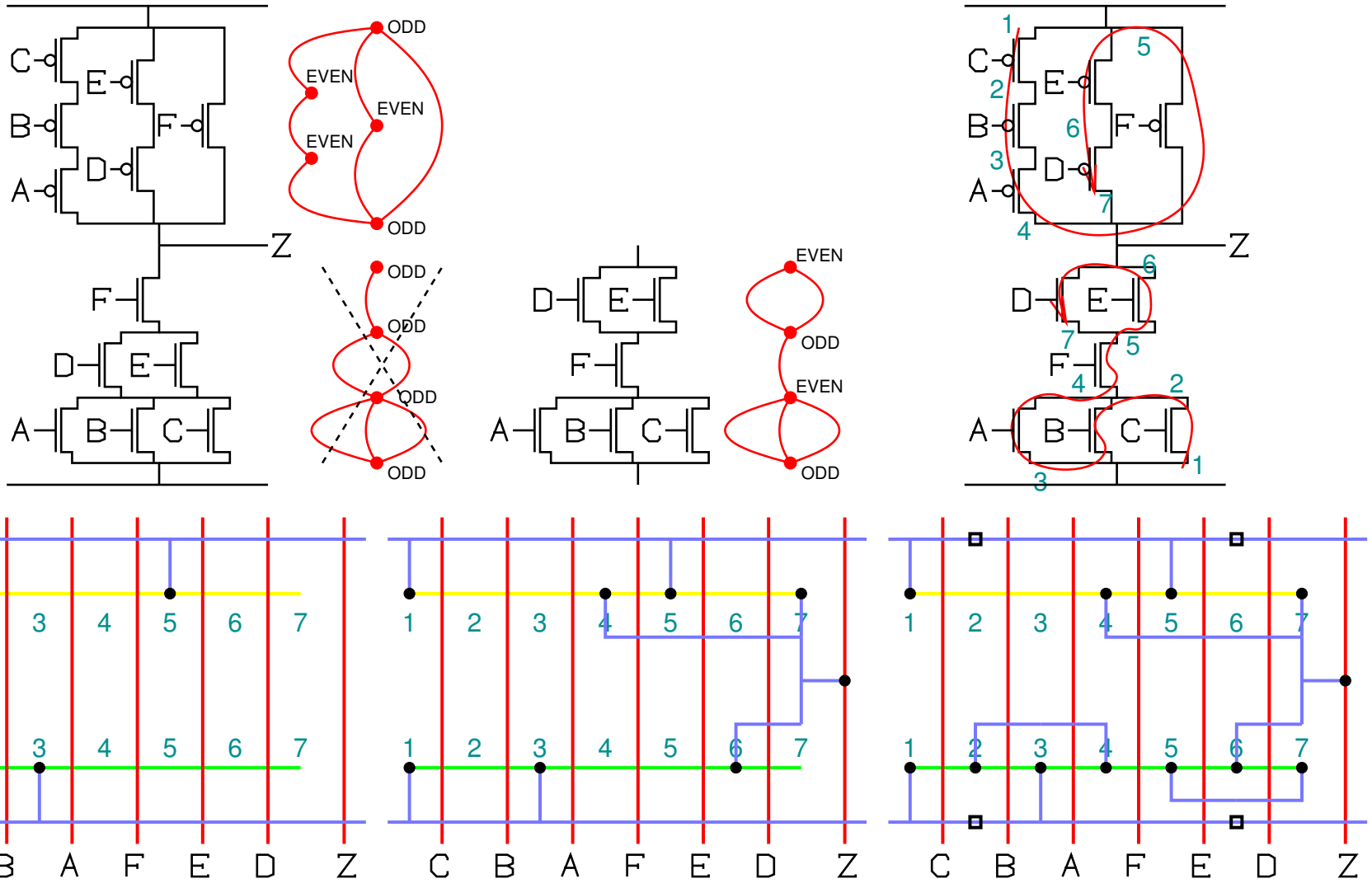
Optimised Mask Layout



Equivalent Stick Diagram



Investigation of Euler paths leads to more efficient layout*



*not all gates will support a common Euler path for both PMOS and NMOS

LAYOUT

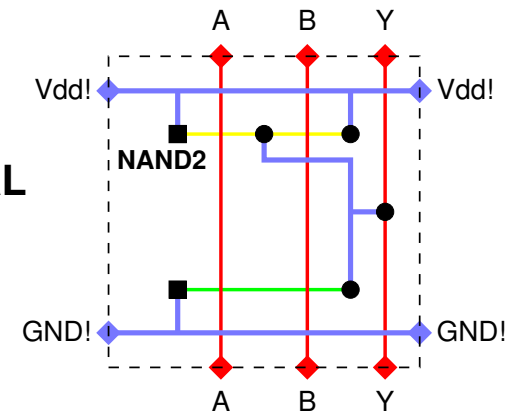
ABSTRACT

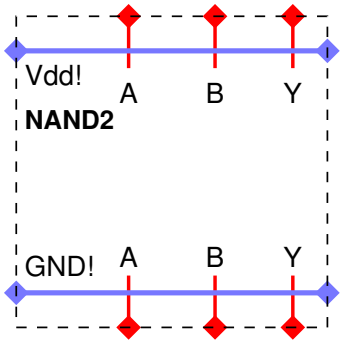
ROUTING

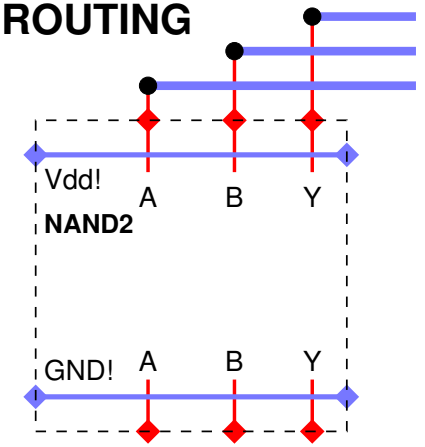
1 METAL LAYER

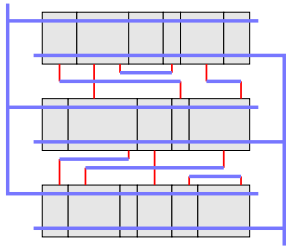
2 METAL LAYERS

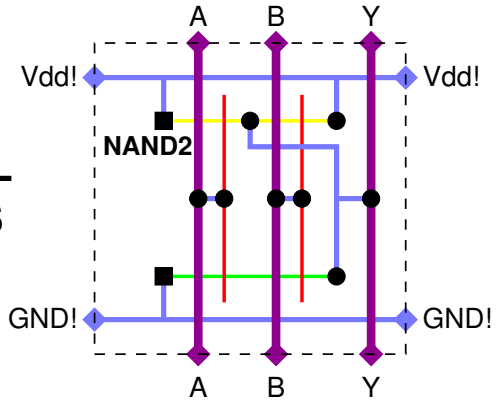
3 METAL LAYERS

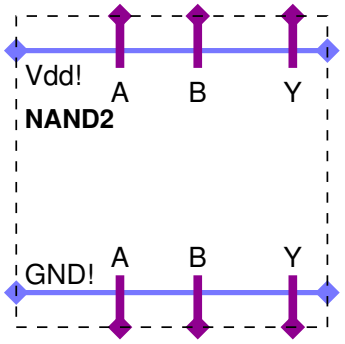


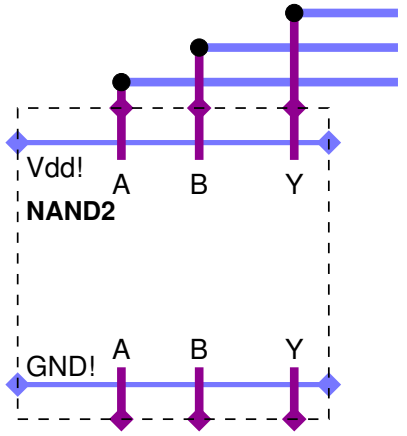


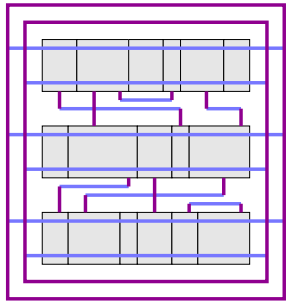


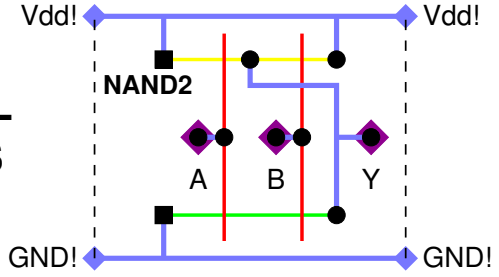


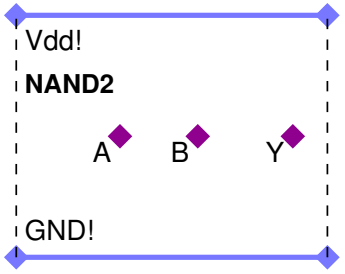


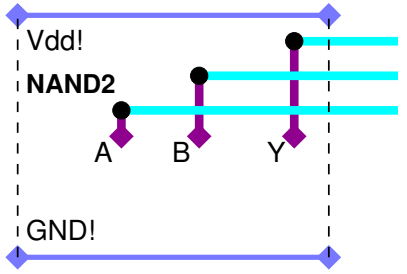


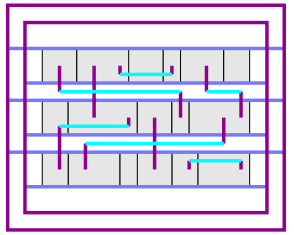


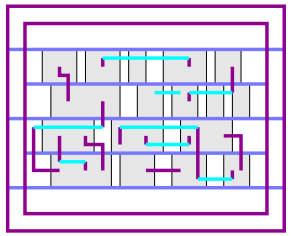




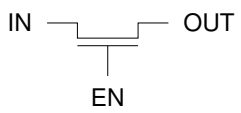




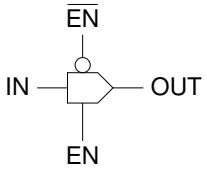


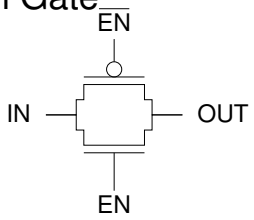


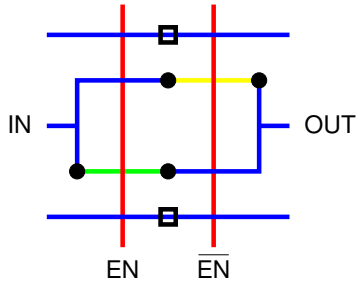
Pass Transistor



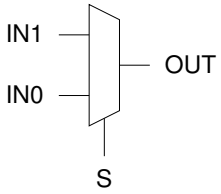
CMOS Transmission Gate

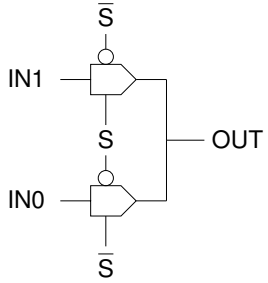


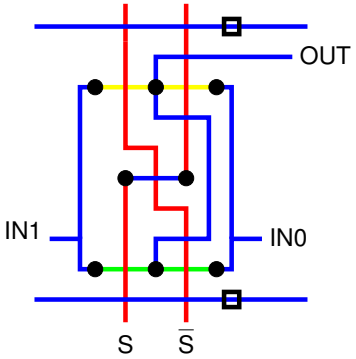




Transmission Gate Multiplexor

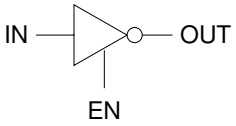


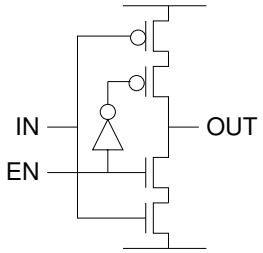


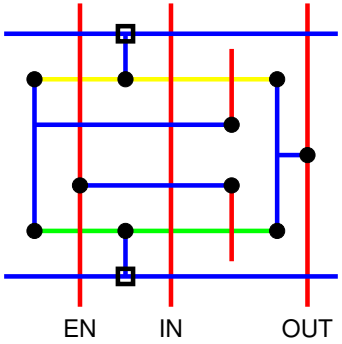


*note distictive polysilicon crossover

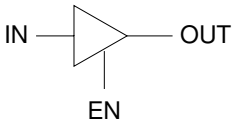
Tri–state Inverter

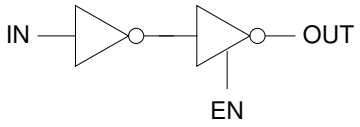






Tri–state Buffer

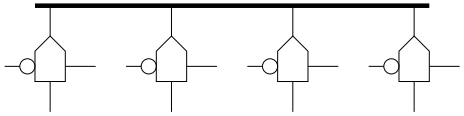




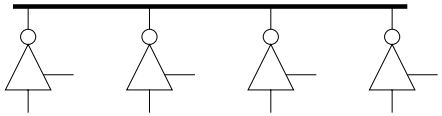
Tri–state gates are used for Multiplexing

Distributed Multiplexing

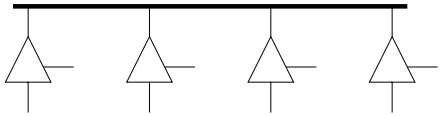
using transmission gates



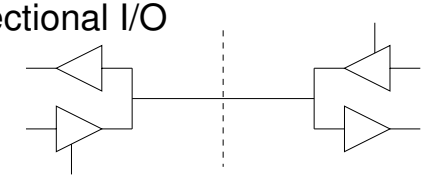
using tri–state inverters



using tri–state buffers

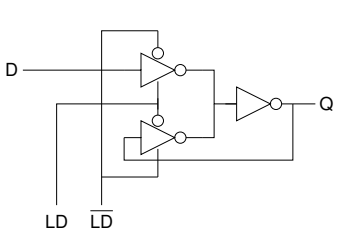


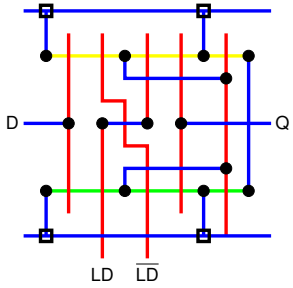
Bi–directional I/O

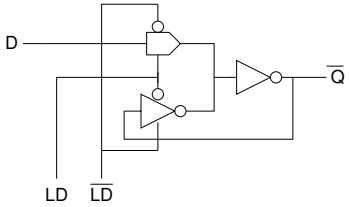


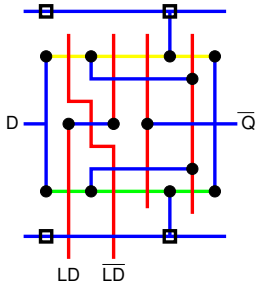
*this is another form of multiplexing

Latch

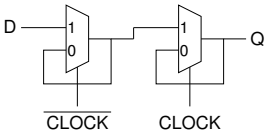


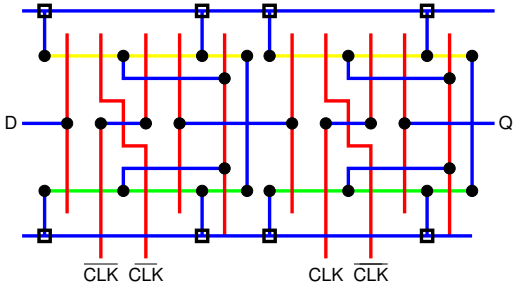


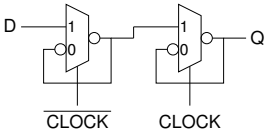


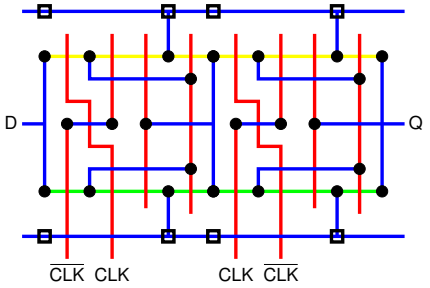


Master Slave D–Type Flip–Flop



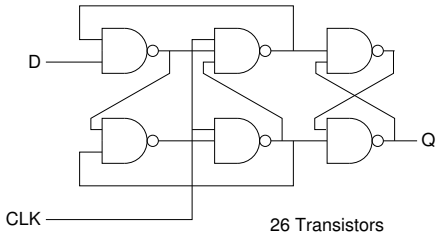


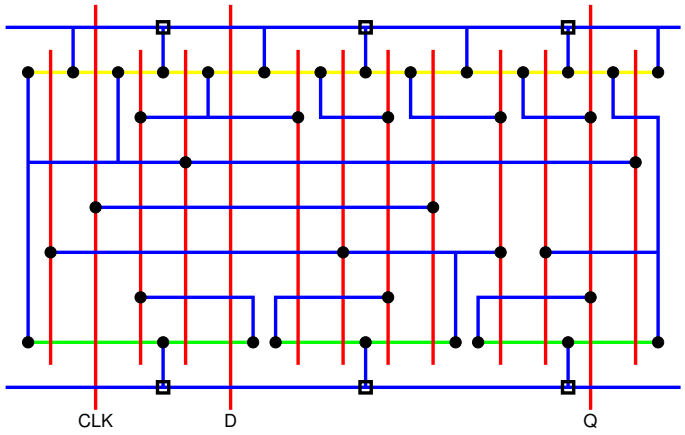




*muliplexor based latches and flip–flops include distictive polysilicon crossover

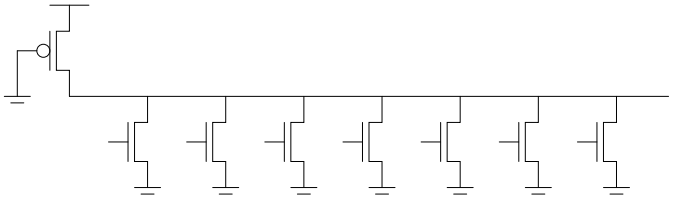
Edge Triggered D–Type Flip–Flop

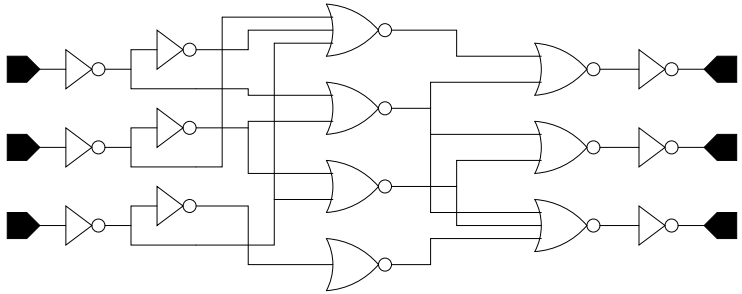


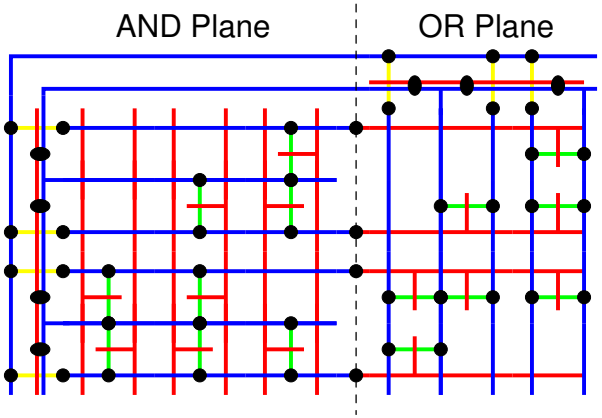


Euler path analysis is applied creatively to these multi–gate cells – gates are often linked via the common gnd/pwr node
Final layouts will be more complex where clock buffers, reset circuitry and metal 2 i/o are included

PLA and ROM





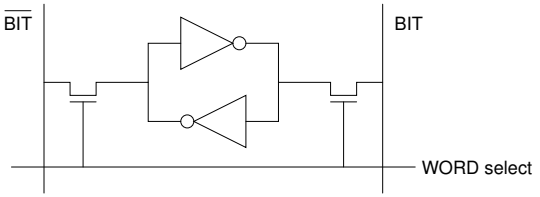


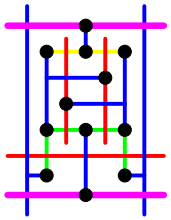
ROM is PLA with

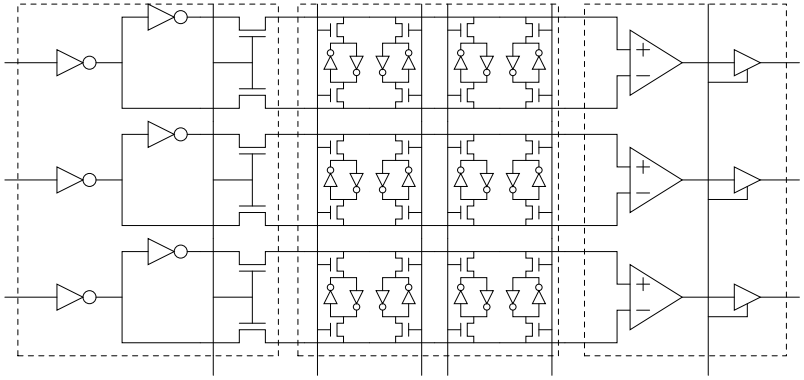
fixed AND (decoder) plane

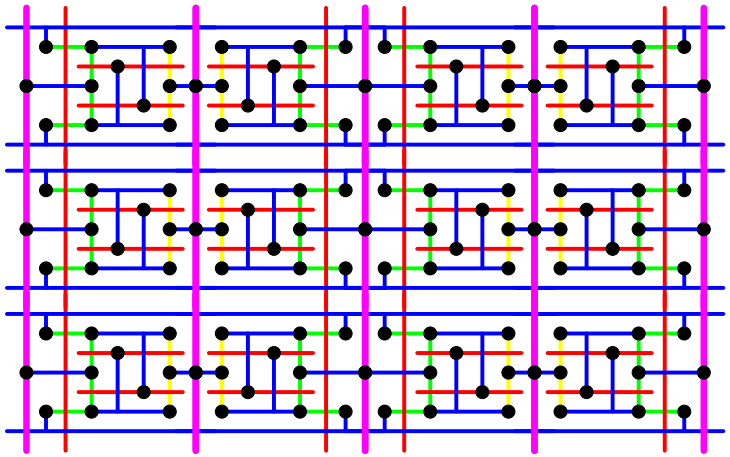
programmable OR (data) plane

SRAM



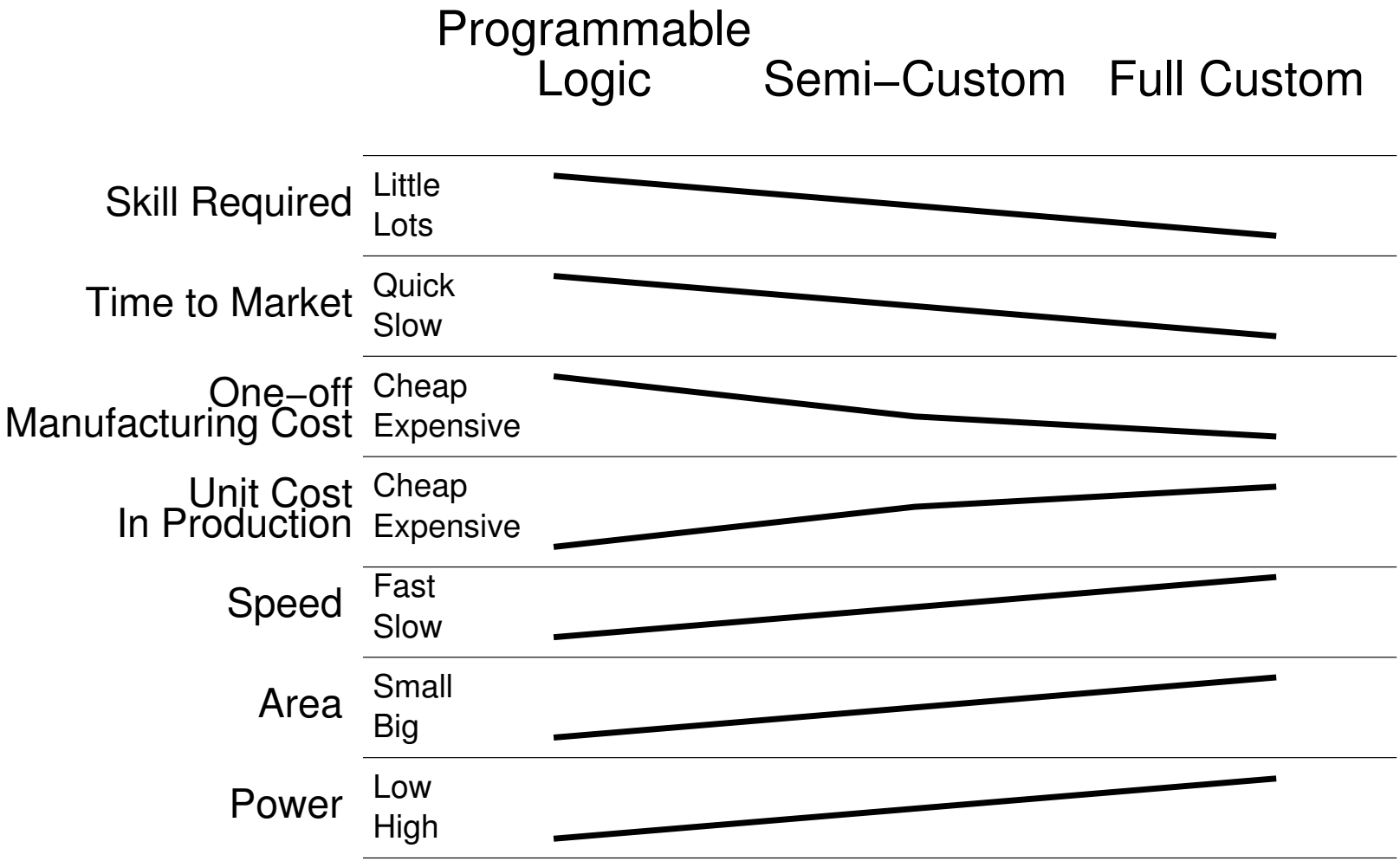






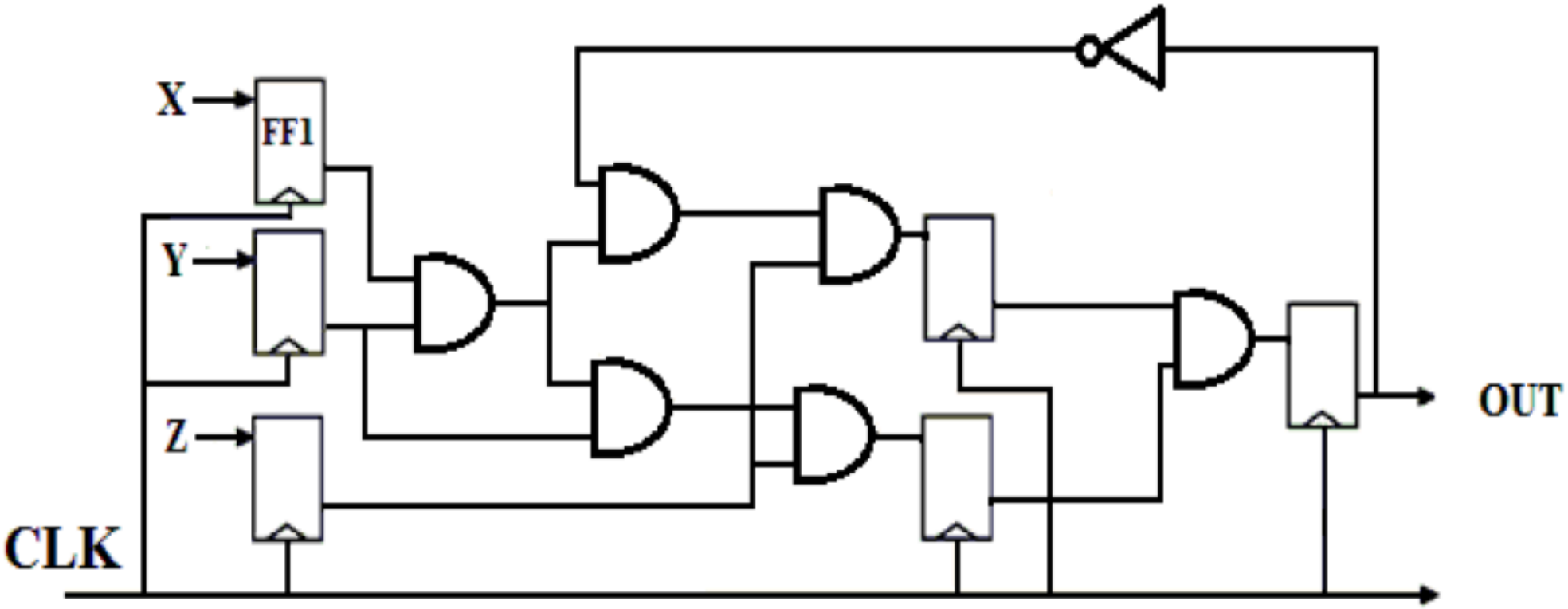
Cells are designed to butt together in two dimensions leading to efficient layout

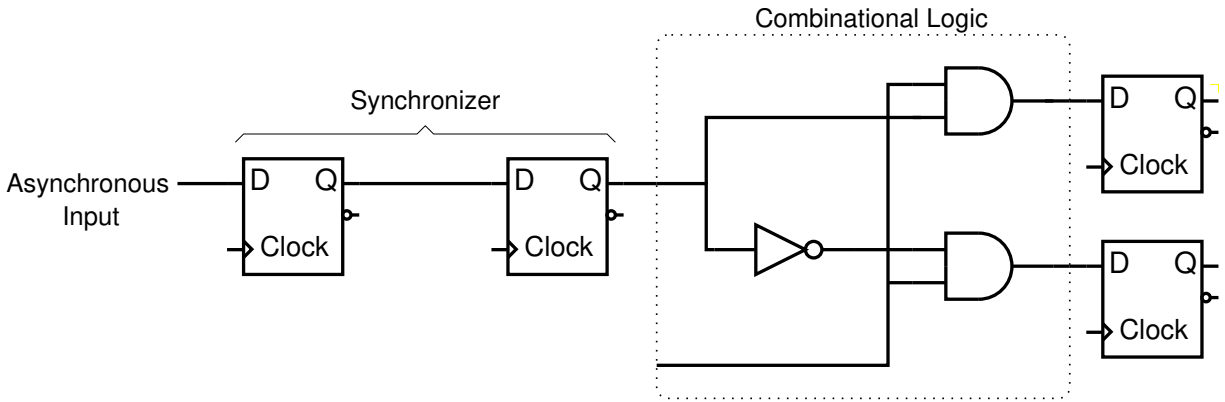
PLA layout efficiency will depend on the actual function implemented (e.g. number of common product terms)

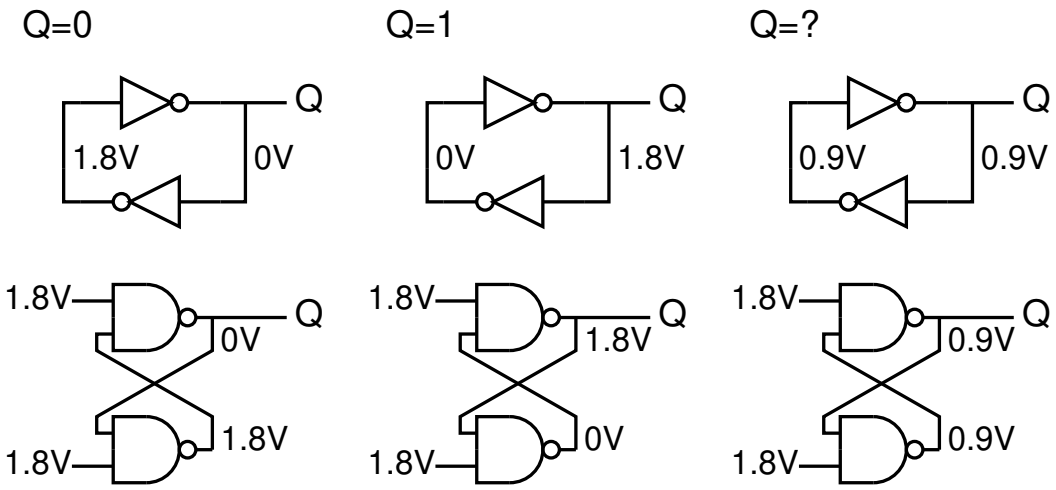


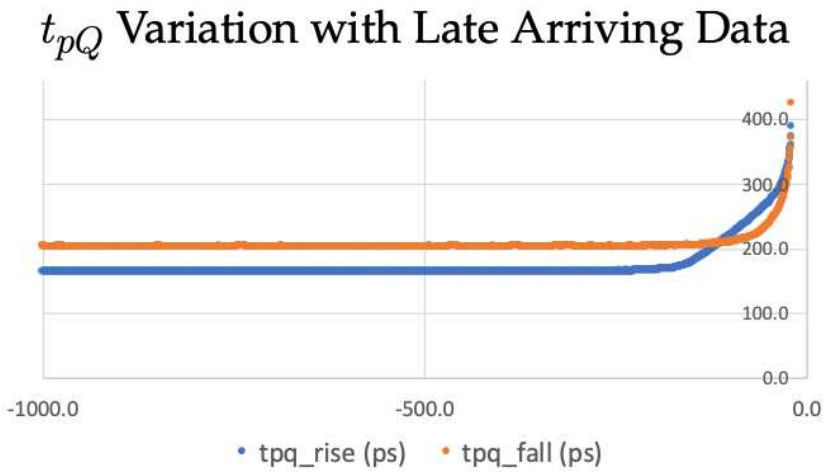
All design styles need full custom designers

A large ASIC (especially SoC) may mix Semi–Custom and Full Custom


X
FF1
Y
Z
CLK
OUT


Combinational Logic
Synchronizer
Asynchronous Input
D
Q
Clock
D
Q
Clock
D
Q
Clock
D
Q
Clock


Q=0
Q=1
Q=?
Q
1.8V
0V
Q
0V
1.8V
Q
0.9V
0.9V
1.8V
1.8V
0V
1.8V
Q
1.8V
1.8V
0V
1.8V
Q
1.8V
0V
1.8V
Q
1.8V
0.9V
1.8V
0.9V


t_{pQ} Variation with Late Arriving Data
400.0
300.0
200.0
100.0
0.0
-1000.0
-500.0
0.0
tpq_rise (ps)
tpq_fall (ps)