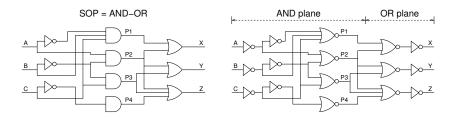
PLAs, ROMs and RAMs

PLA structures

Programmable Logic Array structures provide a logical and compact method of implementing multiple SOP (Sum of Products) or POS expressions.

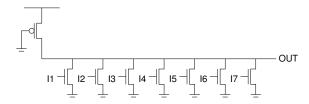


Most PLA structures employ pseudo-NMOS NOR gates using a P-channel device in place of the NMOS depletion load.

10001

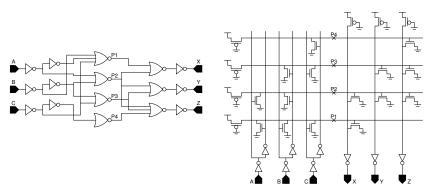
PLAs, ROMs and RAMs

Pseudo-NMOS NOR gate



- Unlike complementary CMOS circuits, these gates will dissipate power under static conditions (since the P device is always on).
- The P and N channel devices must be ratioed in order to create the required low output voltage.
- This ratioing results in a slower gate, although there is a trade-off between gate speed and static power dissipation.

PLA structure

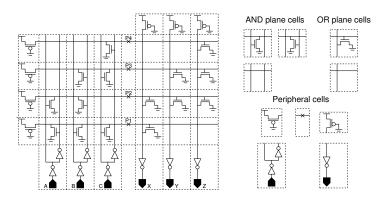


 A regular layout is employed, with columns for inputs and outputs and rows for intermediate expressions.

10003

PLAs, ROMs and RAMs

PLA structure



• Layout is simply a matter of selecting and placing rectangular cells from a limited set.

PLAs, ROMs and RAMs

PLA structure VDD GND VDD GND P4 P4 P2 P2 P1 A B B C C Only AND plane cells are shown here

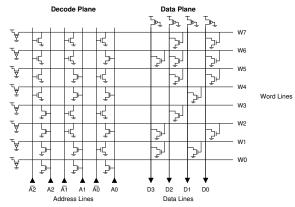
• Conversion to *sticks* is straight forward with opportunities for further optimization.

10005

PLAs, ROMs and RAMs

ROMs

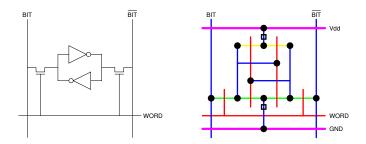
• A ROM may simply be a PLA with fixed decode plane¹ and programmable data plane.



¹RAM structures can make use of the same decode plane.

Static RAM

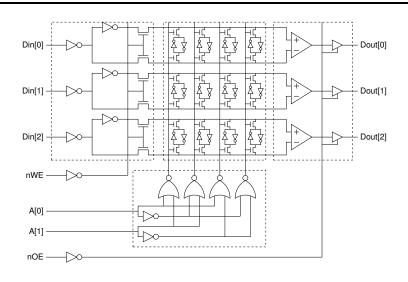
- Used for high density storage on a standard CMOS process.
- Short lived conflict during write NMOS transistors offer stronger path.
- Differential amplifiers are used for speedy read.

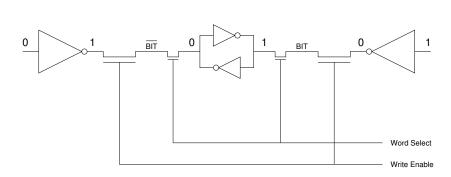


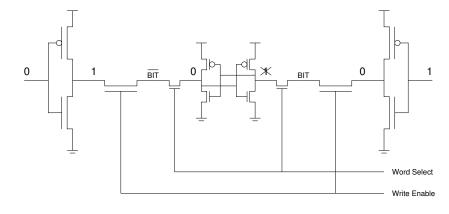
Standard 6 transistor static RAM cell.

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SRAM Structure







10010

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