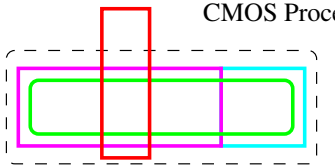
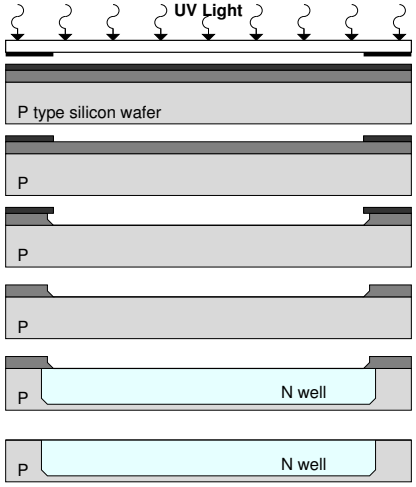
PMOS Enhancement transistor

CMOS Process

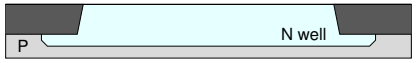


N Well

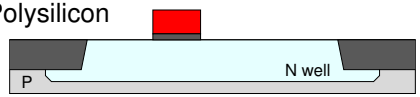


many steps for a single mask

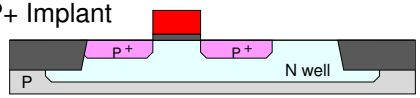
Active Area



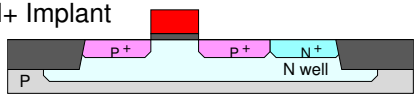
Polysilicon



P+ Implant

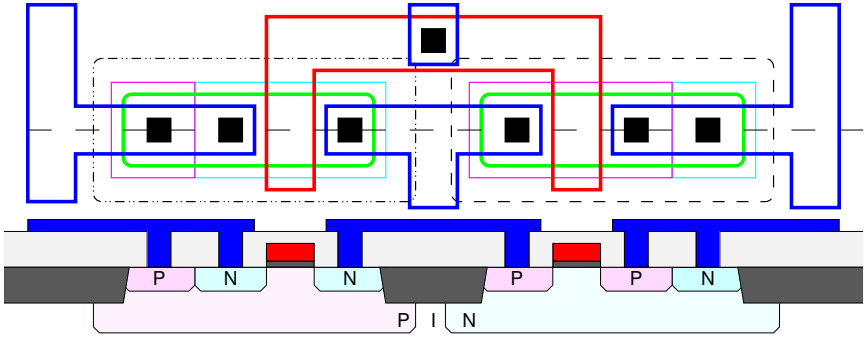


N+ Implant



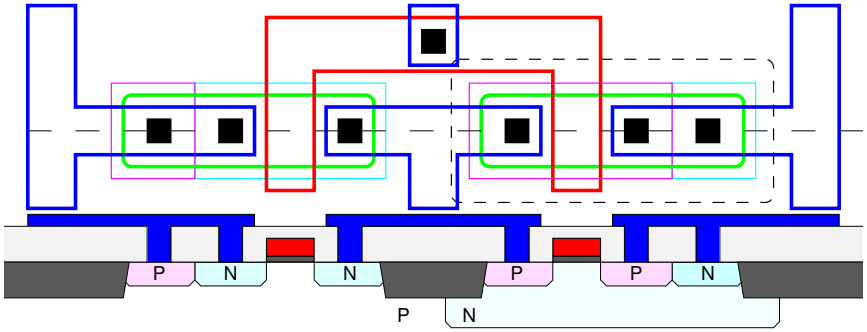
CMOS Inverter

Twin Tub CMOS Process



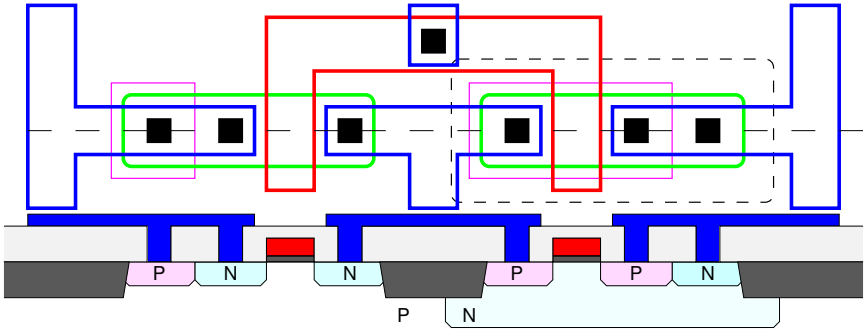
CMOS Inverter

N–Well CMOS Processs (with explicit N+ implant mask)



CMOS Inverter

N–Well CMOS Processs (without explicit N+ implant mask)



Features may be determined by a number of masks
e.g. NMOS source drain: ActiveArea AND NOT(NWell OR Poly OR PImplant)