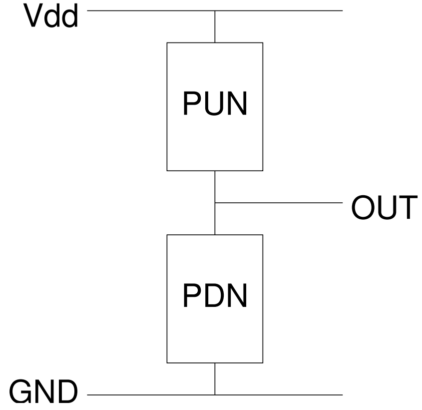
Static CMOS Complementary Gates



- **Static**

  After the appropriate propagation delay the ouput becomes valid and remains valid.[1]

- **Complementary**

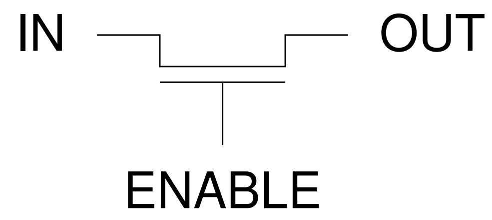
  For any set of inputs there will exist either a path to Vdd or a path to GND.

  Where this condition is not met we have either a high impedence output or a conflict in which the strongest path succeeds. Static CMOS **Non-complementary** gates make use of these possibilities.

[1] c.f. Dynamic logic which uses circuit capicitance to store state for a short time.

Pass Transistor Circuits

- Pass Transistor



  - Provides very compact circuits.
  - Good transmission of logic ‘0’.
  - Poor transmission of logic ‘1’.

    - - slow rise time

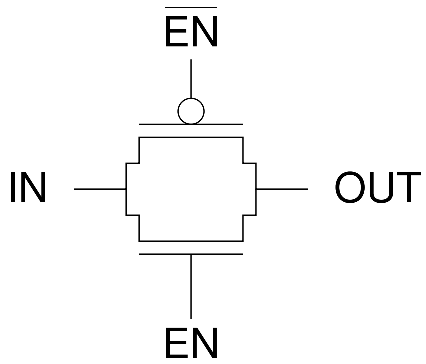
    - - degradation of logic value

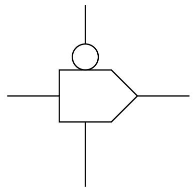
The pass transistor is used in many dynamic CMOS circuits[2].

[2]where pull-up is performed by an alternative method

Pass Transistor Circuits

- Transmission Gate
  - For static circuits we would normally use a CMOS transmission gates:

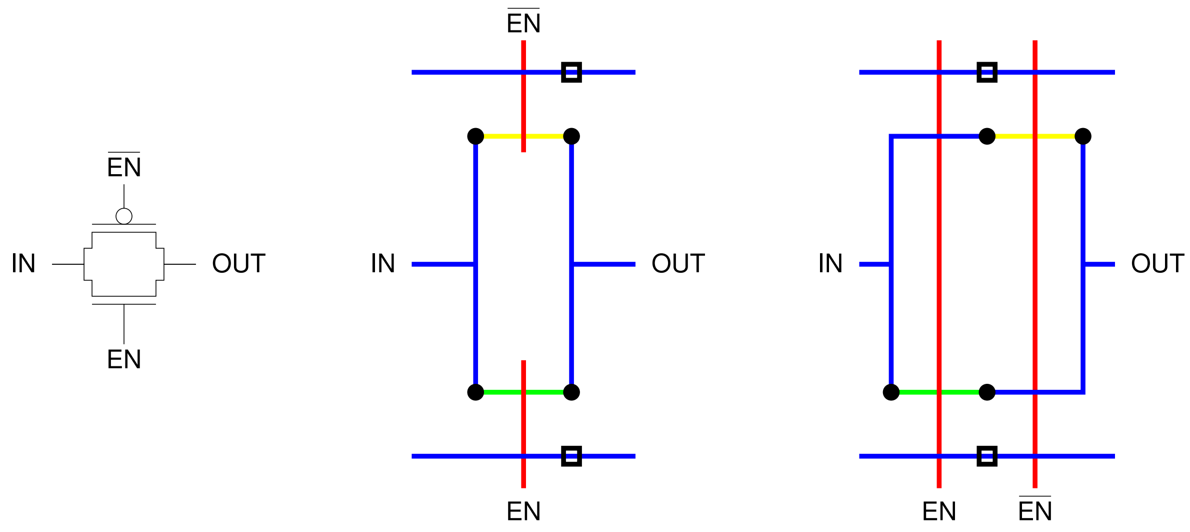




- - balanced *n* and *p* pass transistors
- - faster pull-up
- - slower pull-down

Pass Transistor Circuits

- Transmission Gate Layout

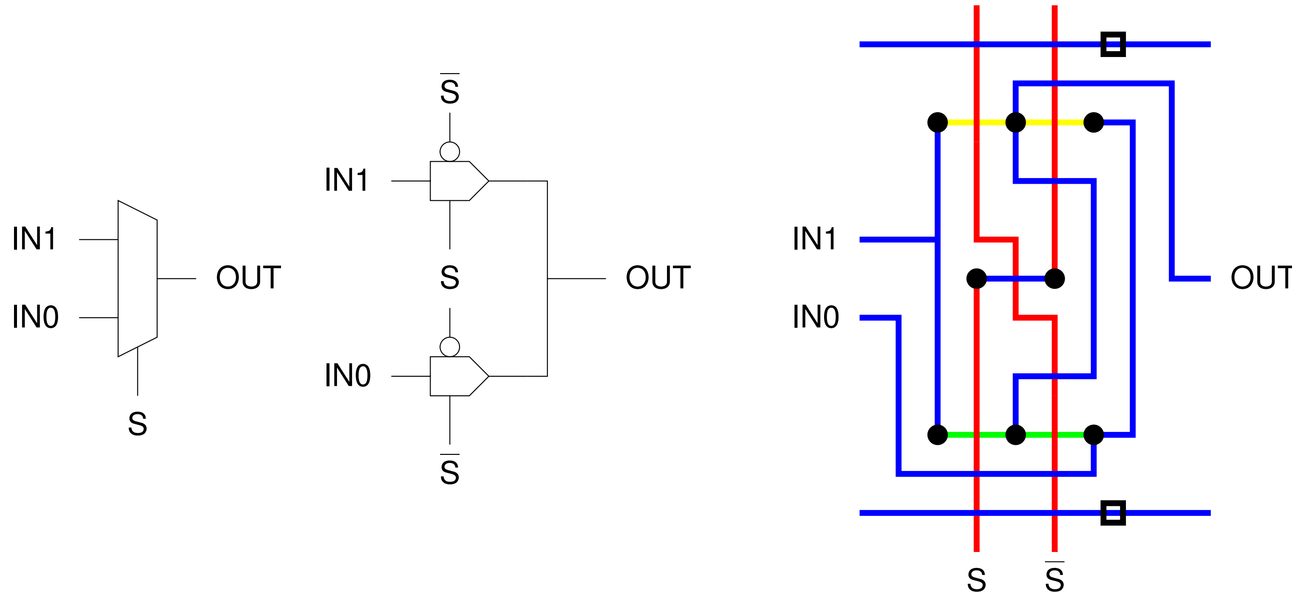


  - note that these circuits are not fully complementary[3] hence they do not immediately lend themselves to a *line of diffusion* implementation.

[3] since there are sets of inputs for which the output is neither pulled low nor high

Pass Transistor Circuits

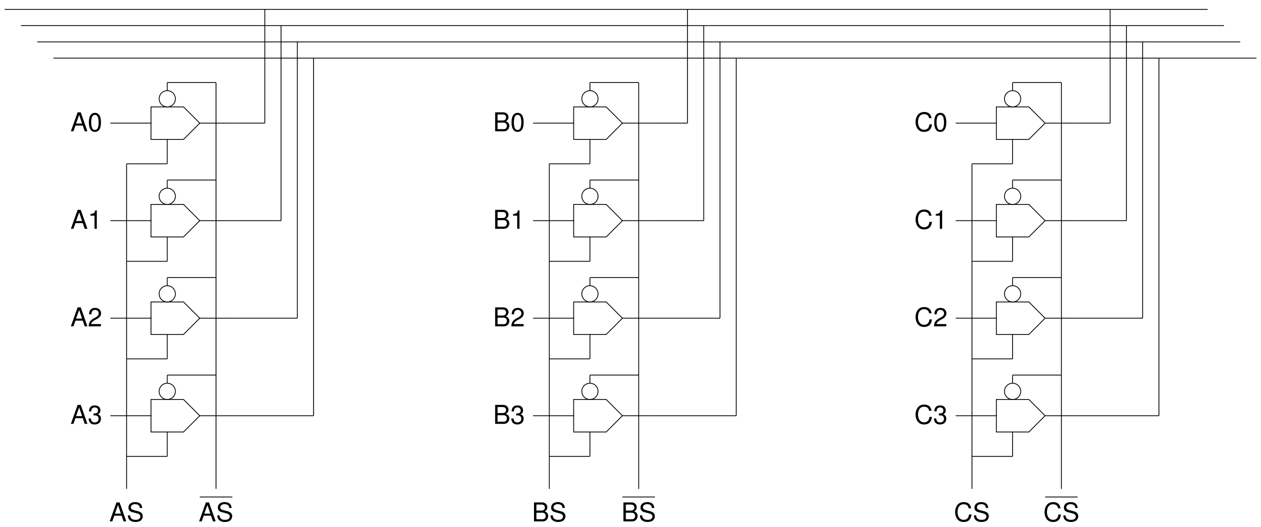
- Transmission Gate Multiplexor



  - very few transistors 4 (+2 for inverter)
  - difficult layout may offset this advantage
    - - prime candidate for 2 level metal

Pass Transistor Circuits

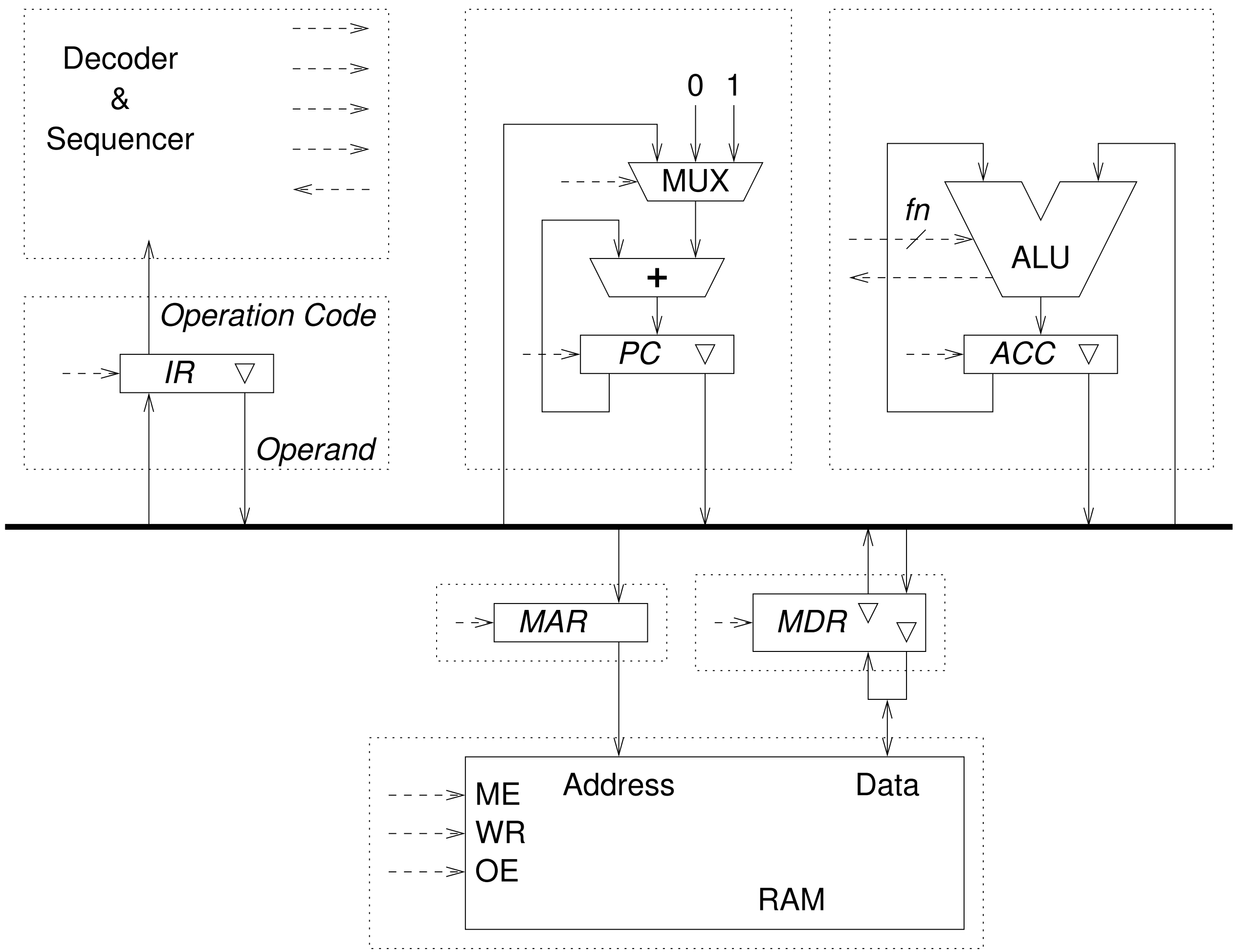
- Bus Wiring



  - distributed multiplexing[4]
  - only one inverter required per bank of transmission gates
  - greatly simplifies global wiring

[4] internal chip bus should never be allowed to float high impedance

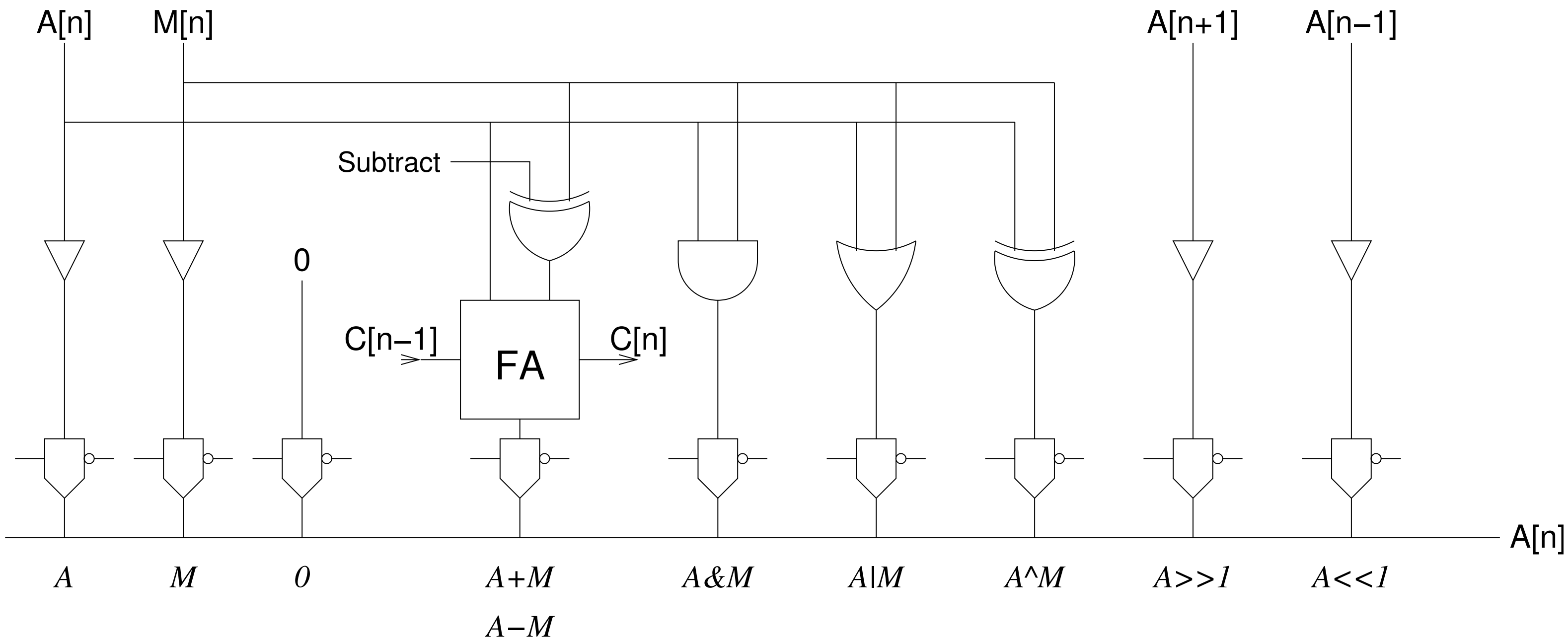
Bus Distributed Multiplexing



Ideal for signals with many drivers from different modules.

Bus Distributed Multiplexing

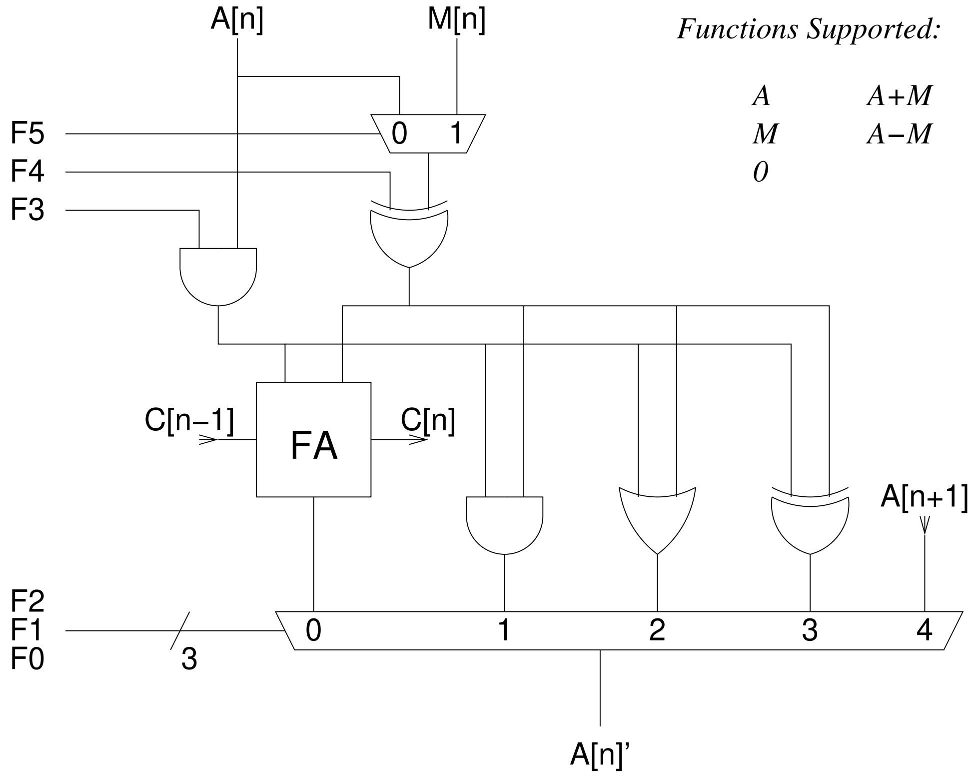
Implementation of bitslice ALU:[5]



- Separate circuit for each function
- Connected via distributed multiplexor

[5]Note that transmission gates have no drive capability in themselves. Here a good drive is ensured by providing buffers.

Bus Distributed Multiplexing



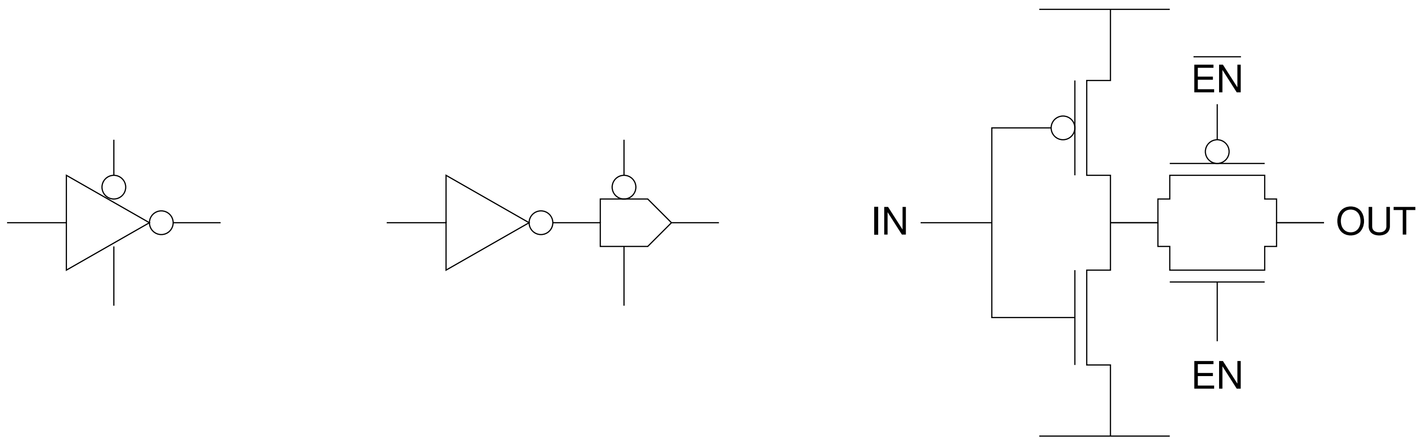
Functions Supported:

A	*A+M*	*A>>1*	*~A*
M	*A−M*	*A<<1*	*~M*
0			*A&M*
			A|M
			A^M
			~(A^M)
			A&~M
			A|~M

- Single optimized ALU module
- Multiplexing is not distributed
- Multiplexor implementation may use transmission gates

Pass Transistor Circuits

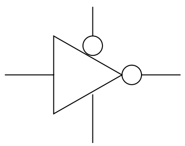
- Tristate Inverter

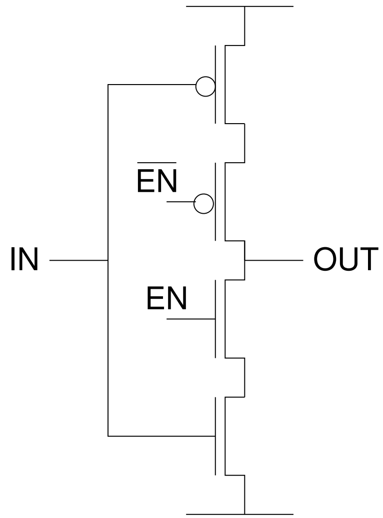


  - Any gate may have a tri-state output by combining it with a transmission gate.

Pass Transistor Circuits

- Tristate Inverter





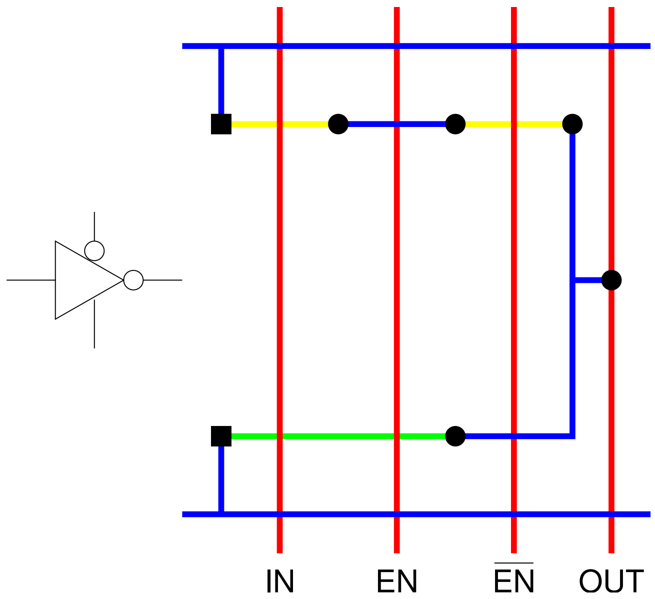
  - Alternatively the transmission gate may be incorporated into the gate.

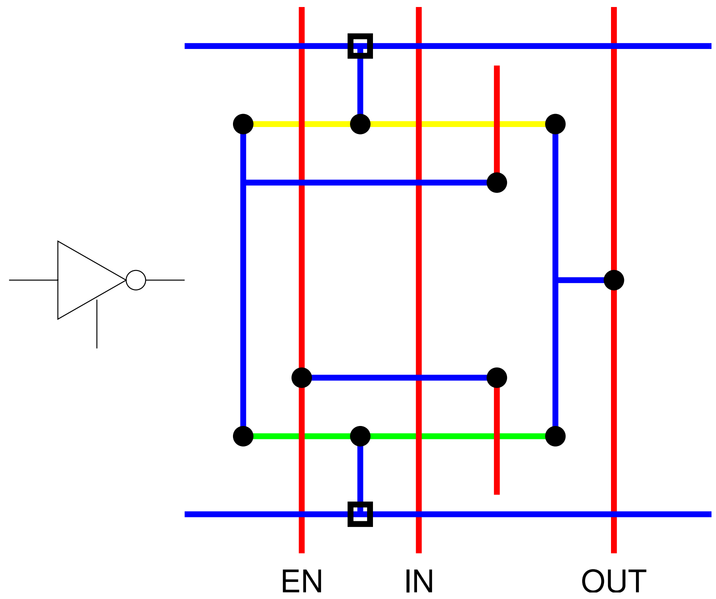
    - - one connection is removed - easier to layout

    - - also easier to simulate!

Pass Transistor Circuits

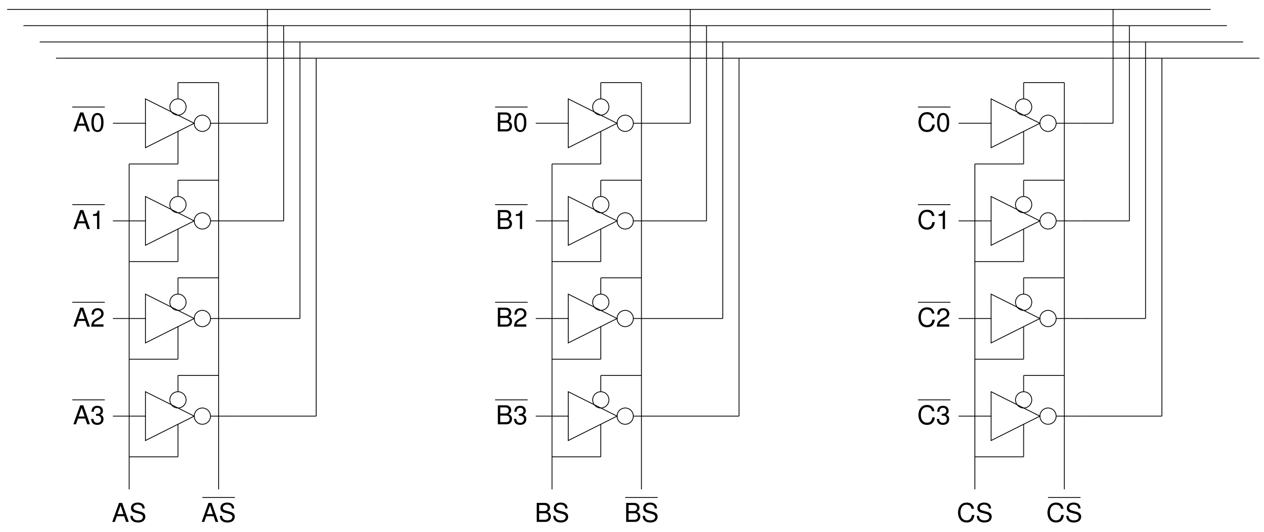
- Tristate Inverter Layout





Pass Transistor Circuits

- Tristate Inverter Bus Driver



  - a tristate inverting buffer is often used to drive high capacitance bus signals
  - transistors may be sized as required