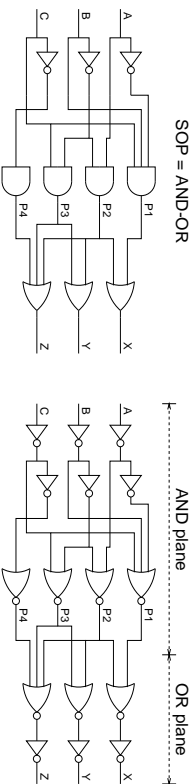# PLAs, ROMs and RAMs

PLA structures

Programmable Logic Array structures provide a logical and compact method of implementing multiple SOP (Sum of Products) or POS expressions.
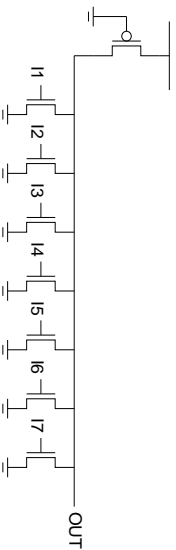

Most PLA structures employ pseudo-NMOS NOR gates using a P-channel device in place of the NMOS depletion load.

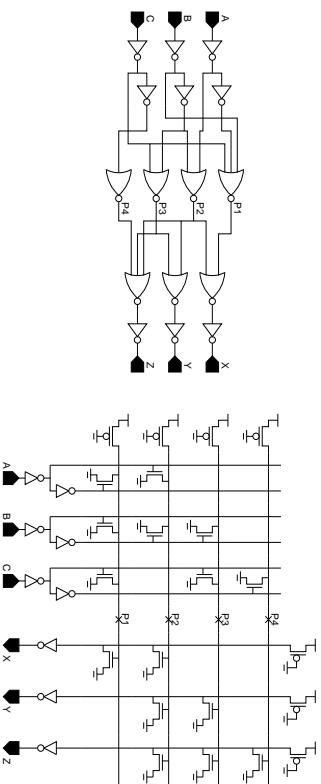
PLAs, ROMs and RAMs

Pseudo-NMOS NOR gate

- Unlike complementary CMOS circuits, these gates will dissipate power under static conditions (since the P device is always on).

- The P and N channel devices must be ratioed in order to create the required low output voltage.

- This ratioing results in a slower gate, although there is a trade-off between gate speed and static power dissipation.

PLAs, ROMs and RAMs

PLA structure

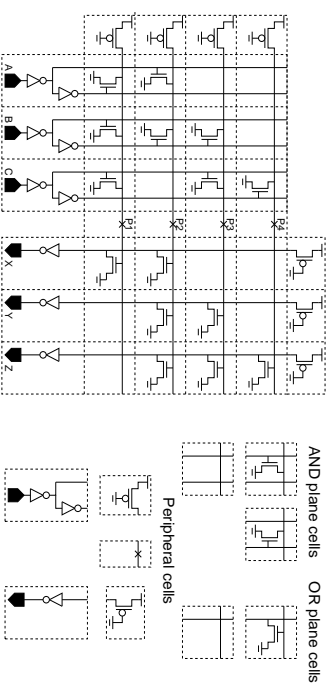
- A regular layout is employed, with columns for inputs and outputs and rows for intermediate expressions.

PLAs, ROMs and RAMs

PLA structure
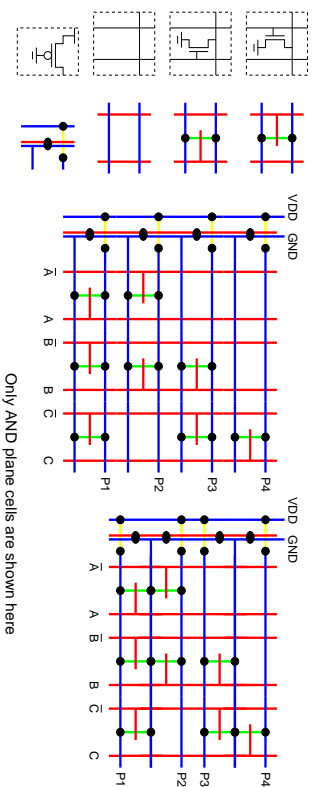

- Layout is simply a matter of selecting and placing rectangular cells from a limited set.
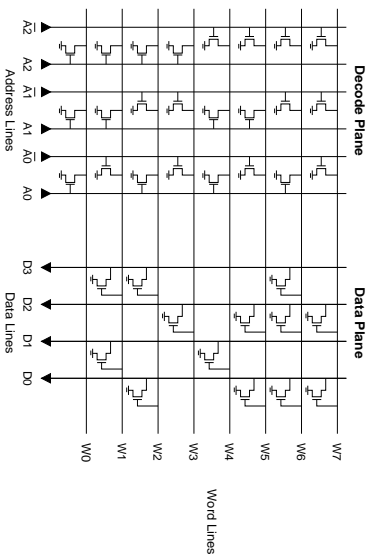
PLA structure

- Conversion to *sticks* is straight forward with opportunities for further optimization.

Only AND plane cells are shown here

VDD GND
Ā A B̄ B C̄ C
P1 P2 P3 P4

ROMs

- A ROM may simply be a PLA with fixed decoder plane[1] and programmable data plane.

Decode Plane
Data Plane

A2, A2̄, A1, A1̄, A0, A0̄
Address Lines

D3, D2, D1, D0
Data Lines

W0, W1, W2, W3, W4, W5, W6, W7
Word Lines

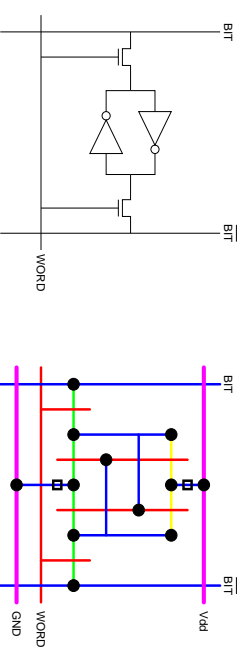[1]RAM structures can make use of the same decode plane.
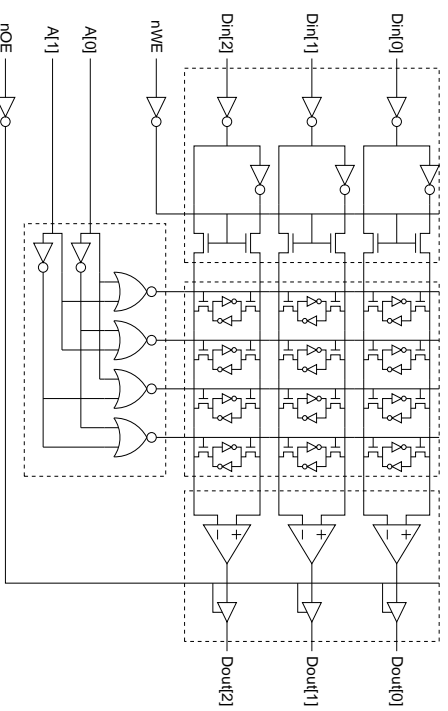
Static RAM

- Used for high density storage on a standard CMOS process.
- Short lived conflict during write - NMOS transistors offer stronger path.
- Differential amplifiers are used for speedy read.

Standard 6 transistor static RAM cell.

BIT, BIT̄, WORD, GND, Vdd

SRAM Structure

Din[2], Din[1], Din[0]
nWE
A[0]
A[1]
nOE

Dout[2], Dout[1], Dout[0]