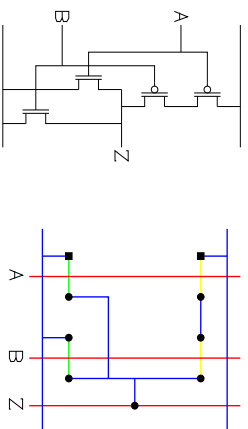


Digital CMOS Design

A logical approach to gate layout.

- All complementary gates may be designed using a single row of n-transistors above or below a single row of p-transistors, aligned at common gate connections.

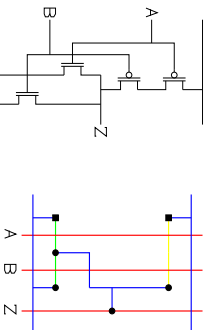


5001

Digital CMOS Design

Euler Path

- For the majority of these gates we can find an arrangement of transistors such that we can butt adjoining transistors.
 - Careful selection of transistor ordering.
 - Careful orientation of transistor source and drain.
- Referred to as *line of diffusion*.



5002

Digital CMOS Design

Finding an Euler Path

Computer Algorithms

- It is relatively easy for a computer to consider all possible arrangements of transistors in search of a suitable Euler path. This is not so easy for the human designer.

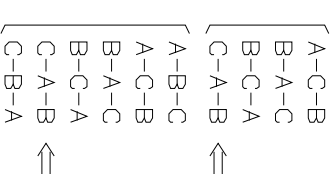
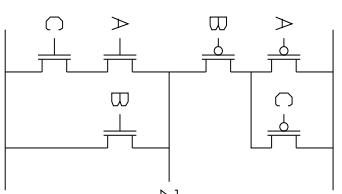
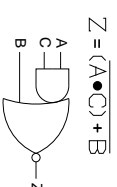
One Human Algorithm

- Find a path which passes through all n-transistors exactly once.
- Express the path in terms of the gate connections.
- Is it possible to follow a similarly labelled path through the p-transistors?
 - Yes – you've succeeded.
 - No – try again (you may like to try a p path first this time).

5003

Digital CMOS Design

Finding an Euler Path

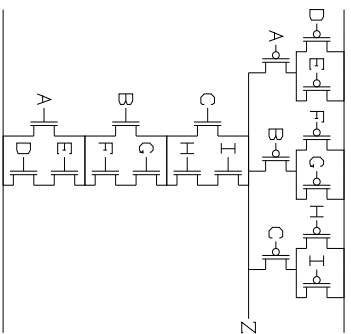
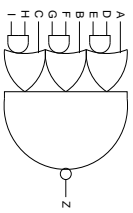


Here there are four possible Euler paths.

5004

Finding an Euler Path

$$Z = (A+(D \bullet E)) \bullet (B+(F \bullet G)) \bullet (C+(H \bullet I))$$



No possible path through P-transistors.
 No re-arrangement will create a solution!