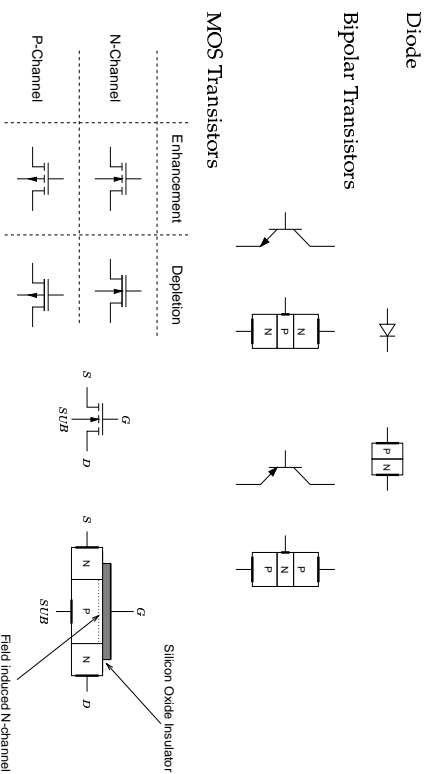


Overview of Technologies

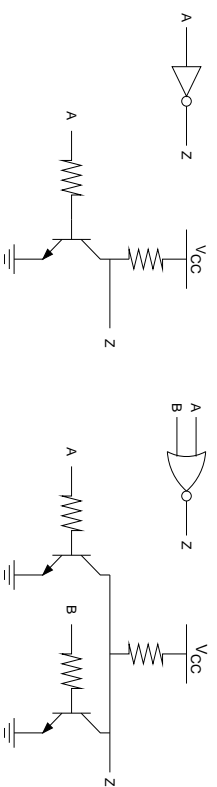
Components for Logic



2001

Overview of Technologies

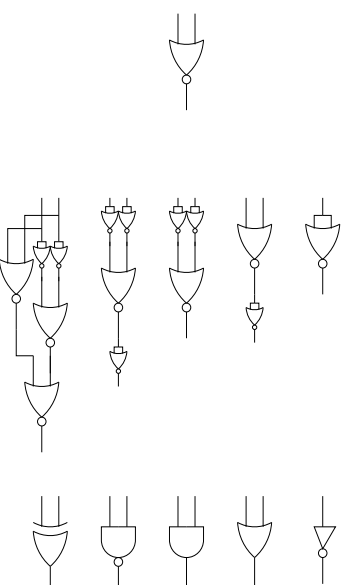
RTL Inverter and NOR gate



2002

Overview of Technologies

All functions can be realized with a single NOR base gate.¹

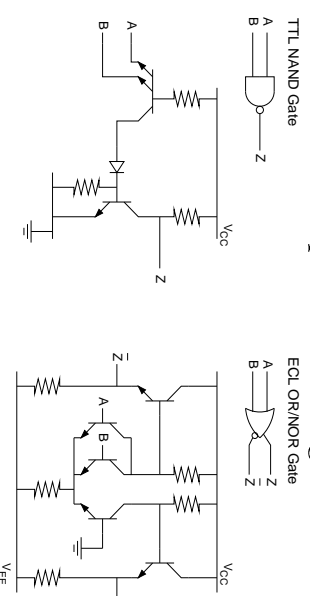


¹NAND gates could be used instead.

2003

Overview of Technologies

Other Bipolar Technologies



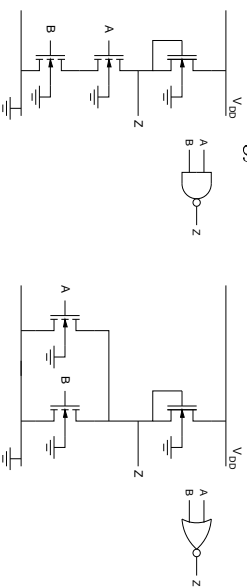
- **TTL** gives faster switching than RTL at the expense of greater complexity². The characteristic multi-emitter transistor reduces the overall component count.
- **ECL** is a very high speed, high power, non-saturating technology.

²Most TTL families are more complex than the basic version shown here

2004

Overview of Technologies

NMOS - a VLSI technology.



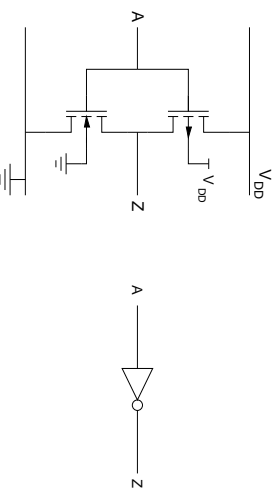
- Circuit function determined by series/parallel combination of devices.
- Depletion transistor acts as non-linear load resistor. Resistance increases as the enhancement device turns on, thus reducing power consumption.
- The low output voltage is determined by the size ratio of the devices.

2005

Overview of Technologies

CMOS logic

CMOS - state of the art VLSI.

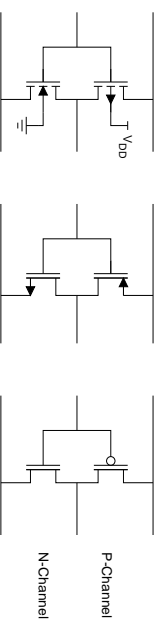


- An active PMOS device complements the NMOS device giving:
 - rail to rail output swing.
 - negligible static power consumption.

2006

Digital CMOS Circuits

Alternative representations for CMOS transistors



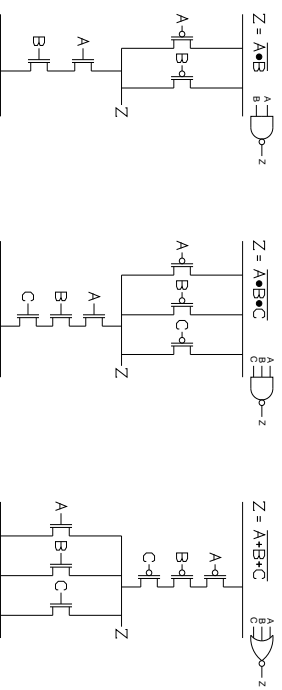
Various shorthands are used for simplifying CMOS circuit diagrams.

- In general substrate connections are not drawn where they connect to Vdd (PMOS) and Gnd (NMOS).
- All CMOS devices are enhancement mode.
- Transistors act as simple digitally controlled switches.

2007

Digital CMOS Circuits

Static CMOS complementary gates

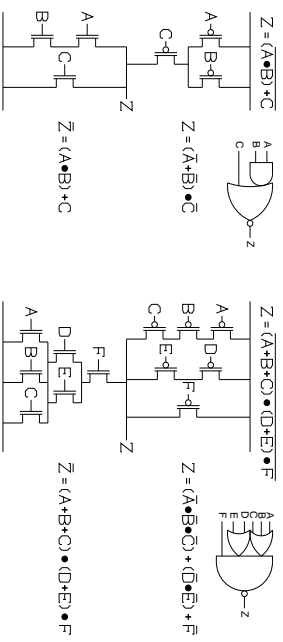


- For any set of inputs there will exist either a path to Vdd or a path to Gnd.

2008

Digital CMOS Circuits

Compound Gates



- All compound gates are inverting.
- Realisable functions are arbitrary AND/OR expressions with inverted output.

2009

Digital CMOS Circuits

Compound Gate Example

$$Z = \overline{(A \bullet B) + (C \bullet D)}$$

Pull Up Network



$$Z = f(\overline{A}, \overline{B}, \overline{C}, \overline{D})$$

$$Z = \dots$$



Pull Down Network

$$\overline{Z} = f(A, B, C, D)$$

$$\overline{Z} = (A \bullet B) + (C \bullet D)$$



2010