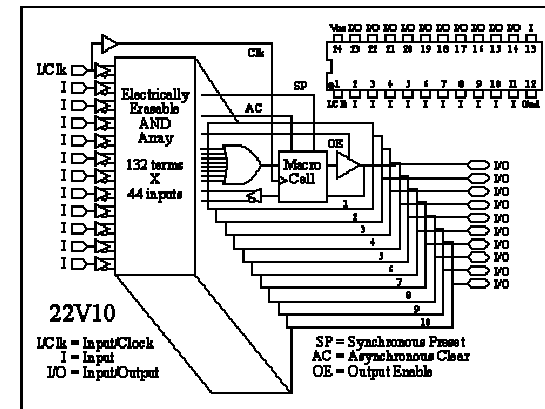


System Design Choices

- Programmable Logic
 - PLD
 - e.g. PAL 22V10, ICT PEEL22CV10, Lattice ispGAL22V10
 - Field Programmable Gate Array (FPGA)
 - e.g. Xilinx XC4013, Altera Cyclone EP1C12
- Semi-Custom Design
 - Mask Programmable Gate Array
 - e.g. ECS CMOS Gate Array
 - Altera HardCopy II structured ASICs
 - Standard Cell Design
 - e.g. Alcatel Mietec MTC45000 0.35 μ m cell library
- Full Custom Design

10001

Programmable Logic



- One time use - Fuse programmable.
- Reprogrammable - UV/Electrically Erasable.

10003

System Design Choices

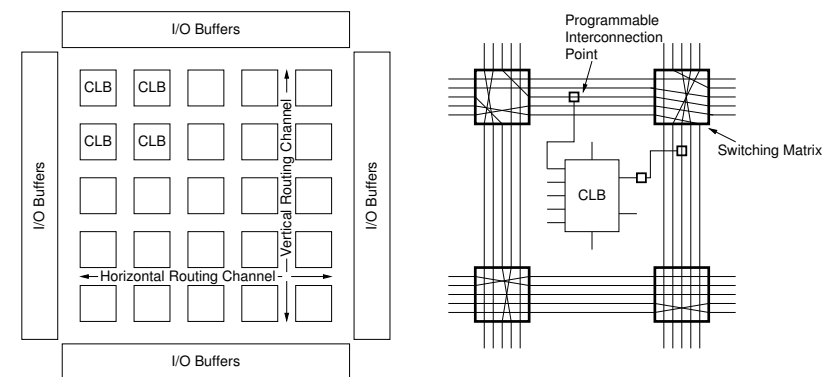
- Programmable Logic
 - Best possible design turnaround time
 - Cheapest for prototyping
 - Best time to market
 - Minimum skill required
- Semi-Custom Design
- Full Custom Design
 - Cheapest for mass production
 - Fastest
 - Lowest Power
 - Highest Density¹
 - Most skill required

START HERE

¹optimization limited by speed/power/area trade off

10002

Field Programmable Gate Array - Xilinx XC4000

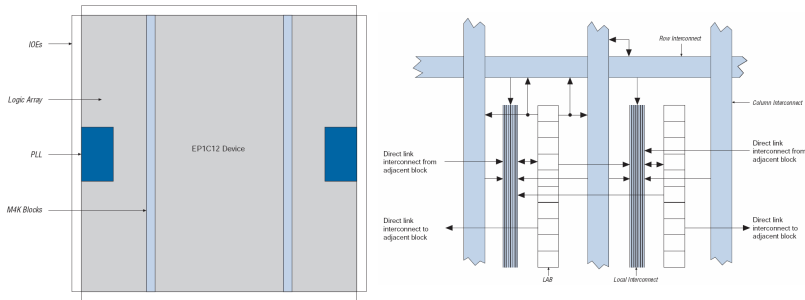


- Configurable Logic Blocks & I/O Blocks²
- Programmable Interconnect

²Xilinx XC4013 has 576 (24 x 24) CLBs and up to 192 (4 x 48) user I/O pins.

10004

Field Programmable Gate Array – Altera Cyclone

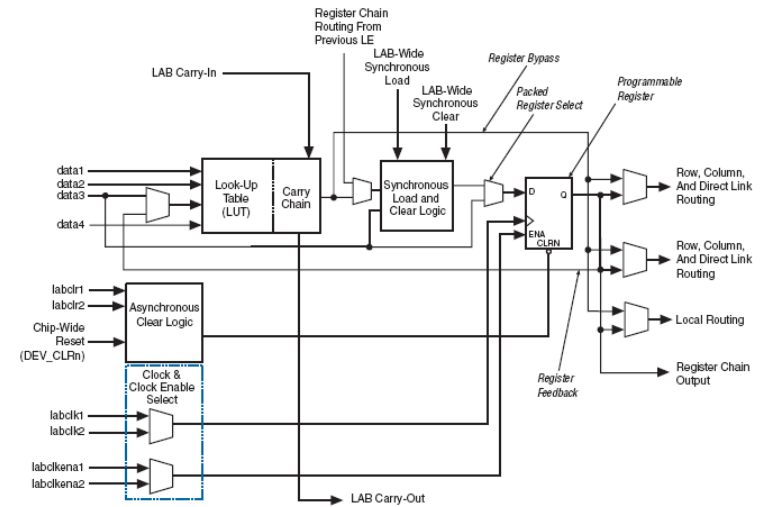


- Logic Array Blocks, M4K Ram Blocks & I/O Elements³
- Programmable Interconnect

³Altera Cyclone EP1C12 has 12060 Logic Elements (arranged as 1206 Logic Array Blocks) and up to 249 user I/O pins.

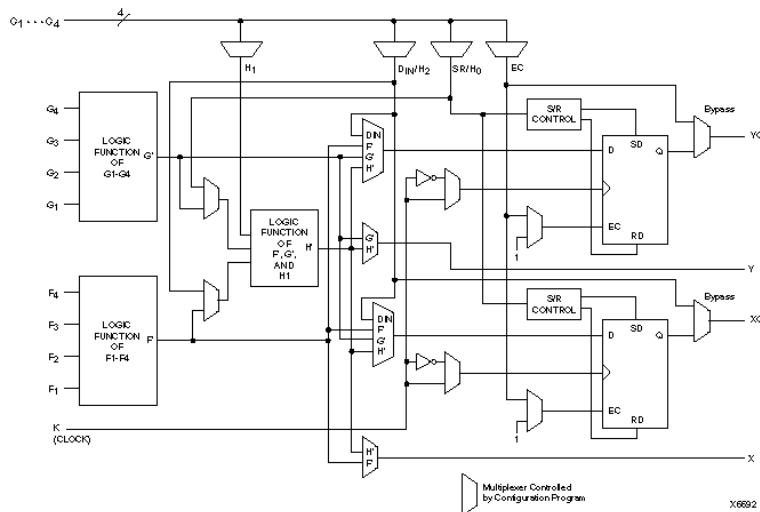
10004

Field Programmable Gate Array – Altera Cyclone LE



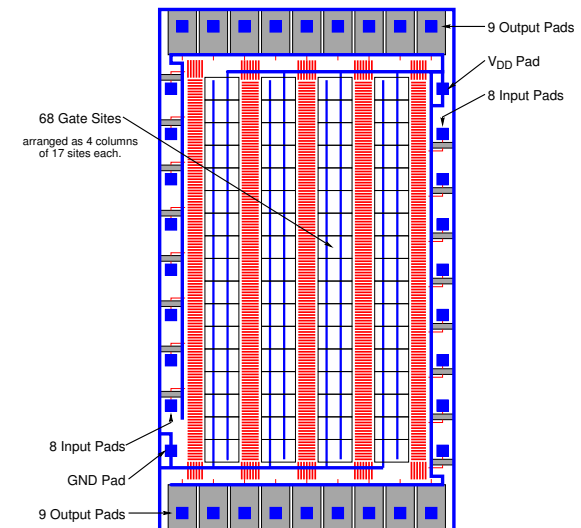
10005

Field Programmable Gate Array – Xilinx XC4000 CLB



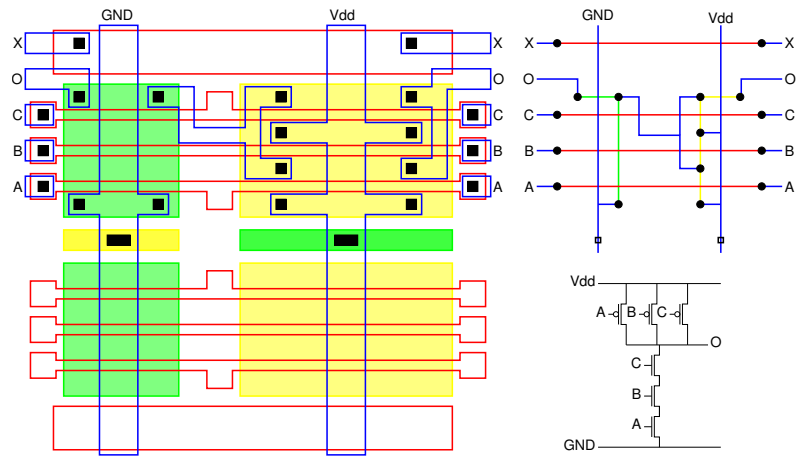
10005

Mask Programmable Gate Array



10006

Mask Programmable Gate Array



- Customize Metal and Contact Window masks only.

10007

Full Custom

All design styles need full custom designers

- to design the base programmable logic chips
- to design building blocks for semi-custom

Where large ASICs use full custom techniques they are likely to be used alongside semi-custom techniques.

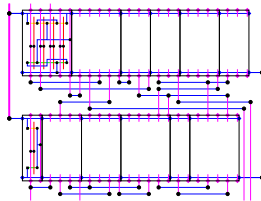
e.g. Hand-held computer game chip

- Full custom bitslice datapath
hand crafted for optimum area efficiency and low power consumption
- Standard cell controller
- Macro block RAM, ROM

10009

Standard Cell Design

- Logic Functions



- Auto Generated Macro Blocks
 - PLA
 - ROM
 - RAM
- System Level Blocks
 - Microprocessor core⁴

⁴Will support System On Chip applications.

10008