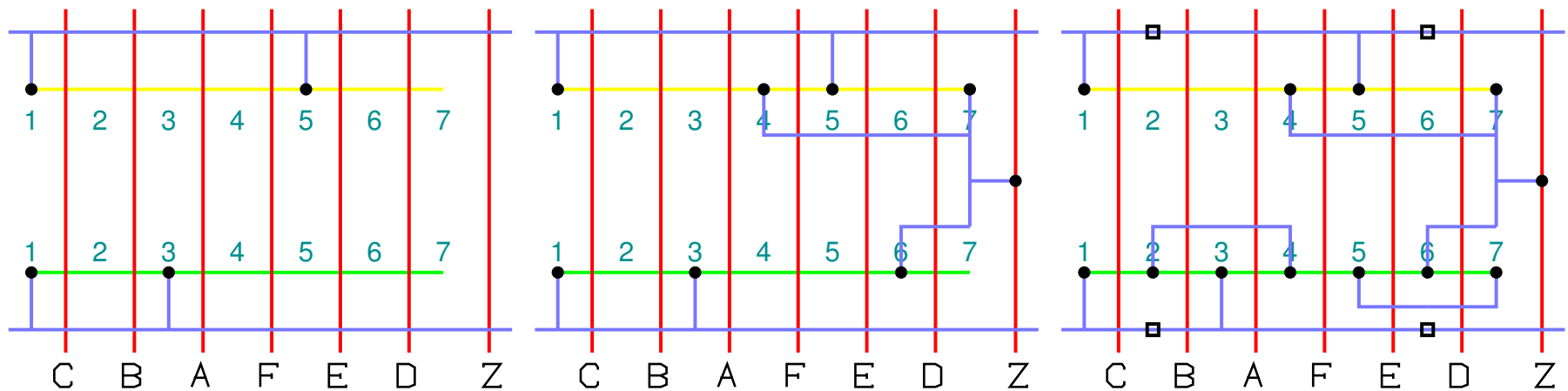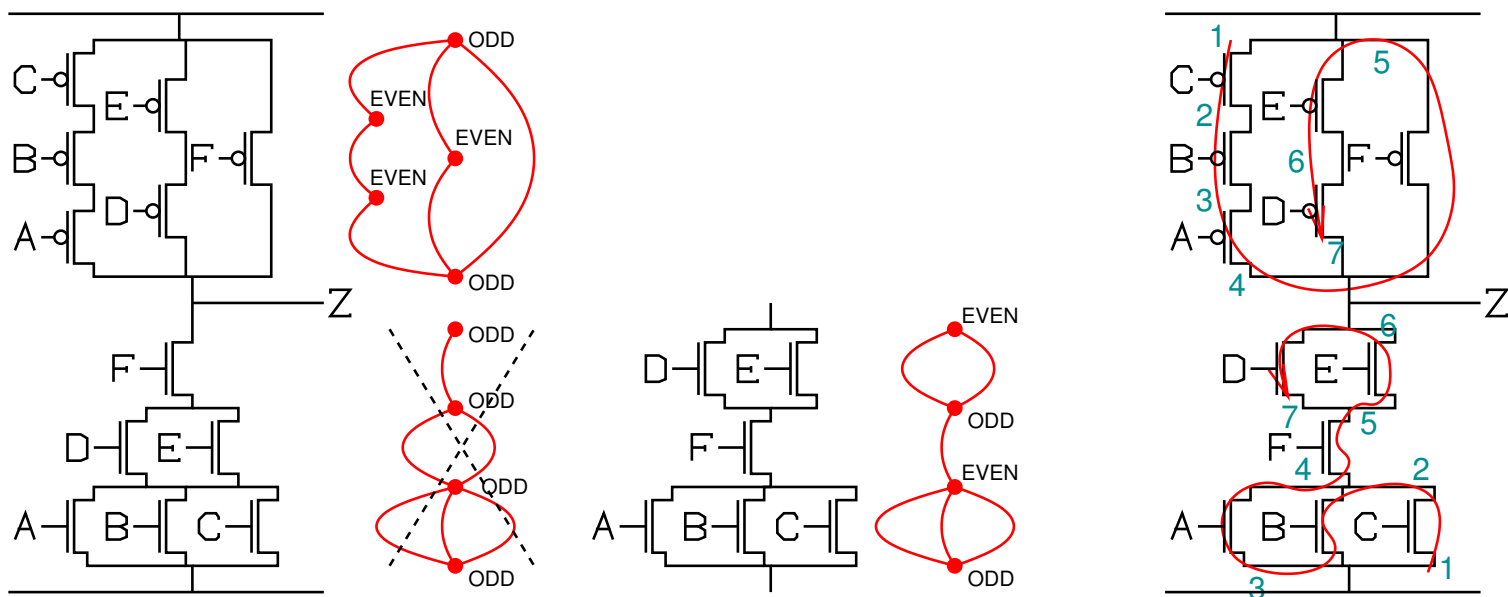# Investigation of Euler paths leads to more efficient layout*

*not all gates will support a common Euler path for both PMOS and NMOS

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