

System Design Choices

- Programmable Logic

- PLD
 - e.g. Lattice ispGAL22V10, Atmel ATF1502 CPLD
- Field Programmable Gate Array (FPGA)
 - e.g. Altera Cyclone III, Xilinx Artix-7/Zync-7000

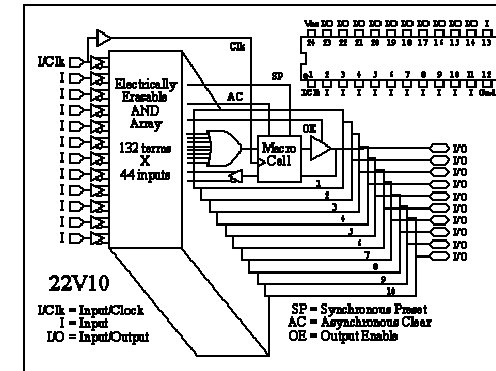
- Semi-Custom Design

- Mask Programmable Gate Array
 - e.g. ECS CMOS Gate Array
 - Altera HardCopy II structured ASICs
- Standard Cell Design
 - e.g. Alcatel Mietec MTC45000 0.35 μ m cell library

- Full Custom Design

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Programmable Logic



ICT PEEL22CV10

Source: ICT

- One time use - Fuse programmable.
- Reprogrammable - UV/Electrically Erasable.

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System Design Choices

- Programmable Logic

- Best possible design turnaround time
- Cheapest for prototyping
- Best time to market
- Minimum skill required

START HERE

- Semi-Custom Design

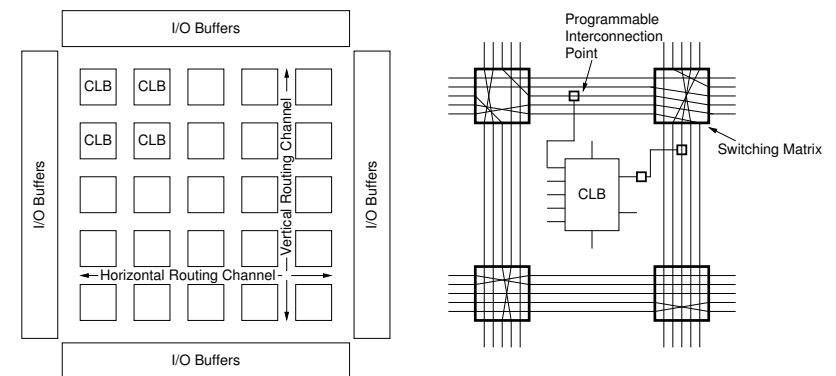
- Full Custom Design

- Cheapest for mass production
- Fastest
- Lowest Power
- Highest Density¹
- Most skill required

¹optimization limited by speed/power/area trade off

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Field Programmable Gate Array – Xilinx XC4000

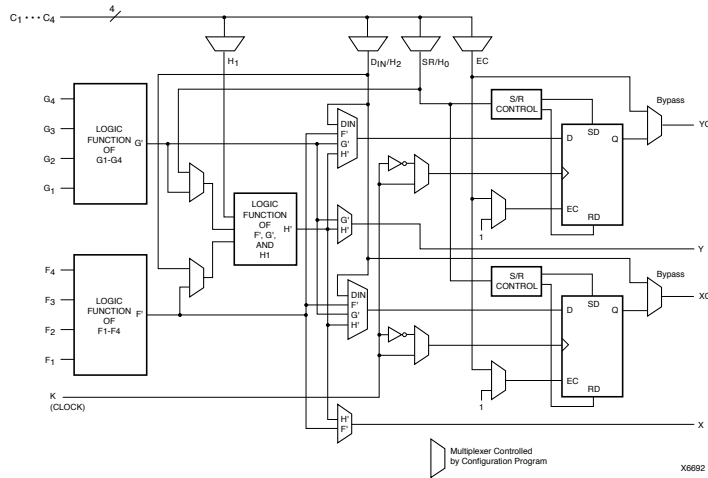


- Configurable Logic Blocks (CLBs) & I/O Blocks²
- Programmable Interconnect

²Xilinx XC4013 has 576 (24 × 24) CLBs and up to 192 (4 × 48) user I/O pins.

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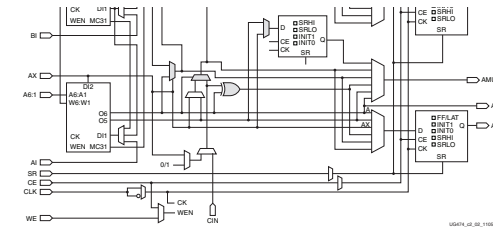
Field Programmable Gate Array – Xilinx XC4000 CLB



Source: Xilinx

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Xilinx Artix-7 – SLICEM CLB³



Source: Xilinx

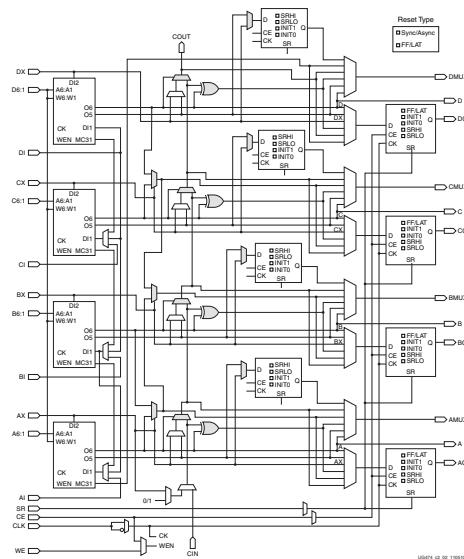
- 4x 6-input Look-Up Tables (LUTs) for combinational logic
- Carry chain supporting fast carry lookahead
- 8x storage elements

LUTs can be alternatively configured as

- 256 bits RAM
- 32-bit shift register

³Xilinx XC7A200T has 16,825 CLBs (each containing 2 slices) and up to 500 user I/O pins.

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Artix-7 – SLICEM CLB

Source: Xilinx

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FPGA - System On Chip

Modern FPGAs are big enough for:

- One or more soft-core processors
- Program memory
- Data memory
- + specialist hardware

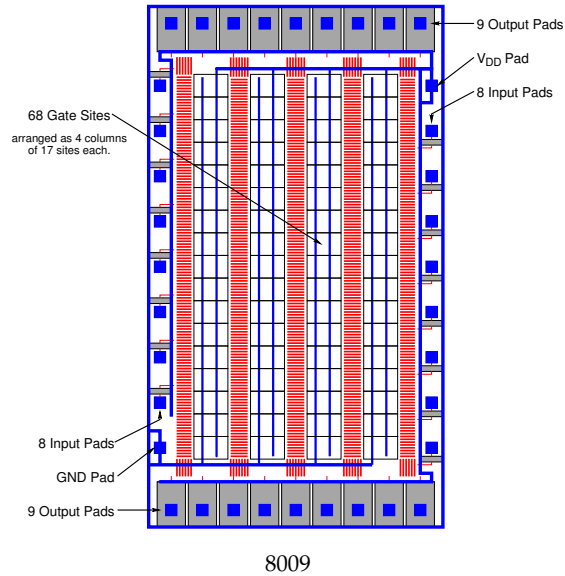
The new trend is for FPGAs with hard processors built in:

- Xilinx Zynq-7000 includes dual-core ARM A9
- Altera Arria V includes dual-core ARM A9
- Cypress PSoC 4 includes ARM Cortex-M0 and programmable digital⁴ and analog blocks

⁴here the digital block is PLD rather than FPGA

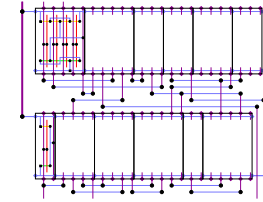
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Mask Programmable Gate Array



Standard Cell Design

- Logic Functions

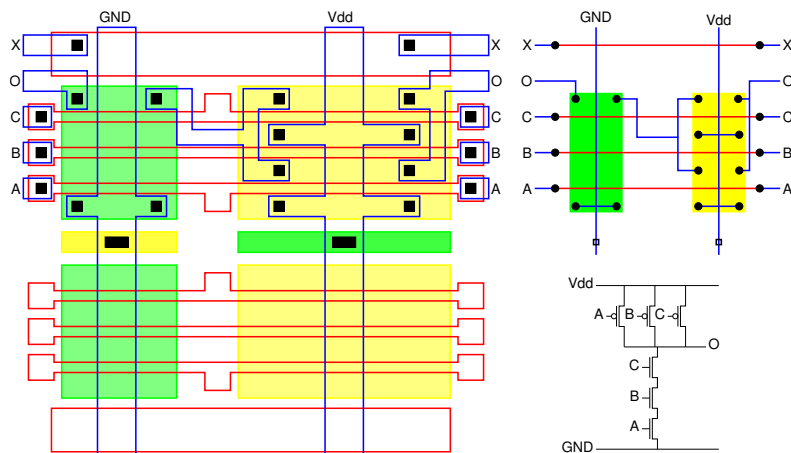


- Auto Generated Macro Blocks
 - PLA
 - ROM
 - RAM
- System Level Blocks
 - Microprocessor core⁵

⁵Will support System On Chip applications.

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Mask Programmable Gate Array



- Customize Metal and Contact Window masks only.

Full Custom

All design styles need full custom designers

- to design the base programmable logic chips
- to design building blocks for semi-custom

Where large ASICs use full custom techniques they are likely to be used alongside semi-custom techniques.

e.g. Hand-held computer game chip

- Full custom bitslice datapath
hand crafted for optimum area efficiency and low power consumption
- Standard cell controller
- Macro block RAM, ROM

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