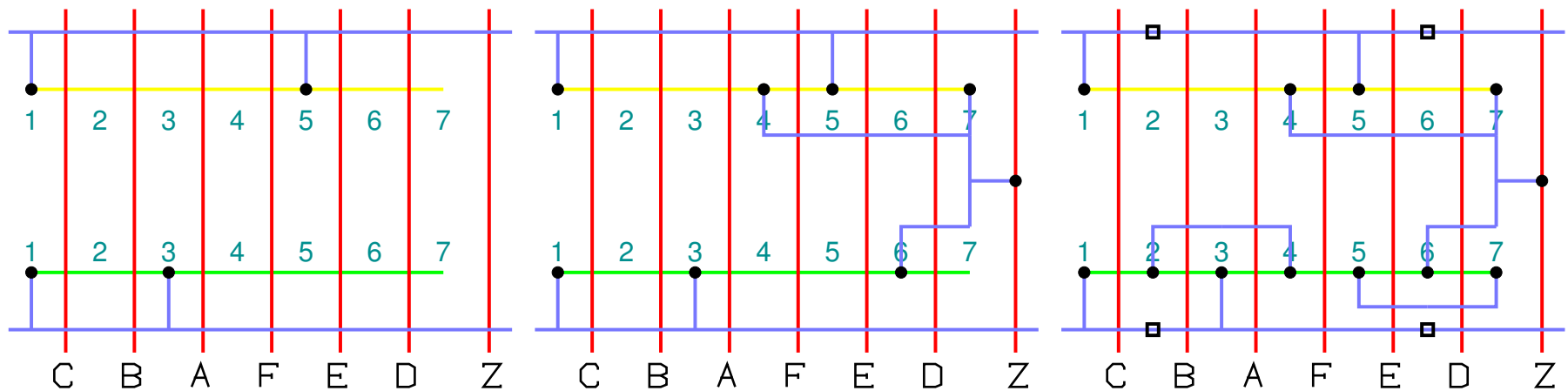
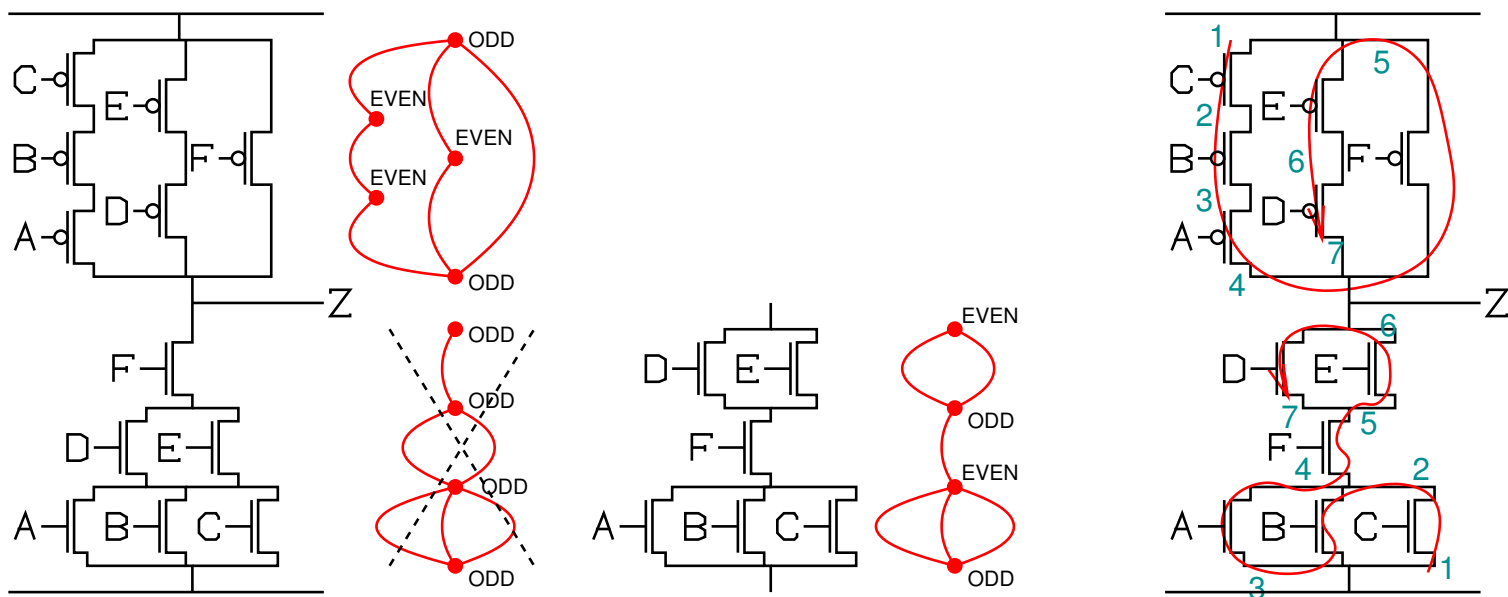


# Investigation of Euler paths leads to more efficient layout\*



\*not all gates will support a common Euler path for both PMOS and NMOS