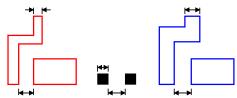
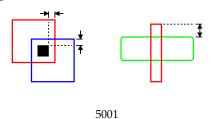
### Design Rules

To prevent chip failure, designs must conform to design rules:

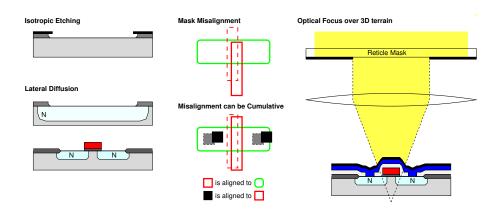
• Single layer rules



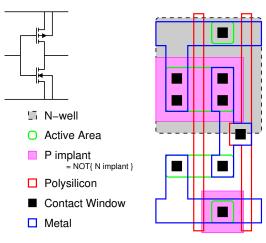
• Multi-layer rules



# Derivation of Design Rules



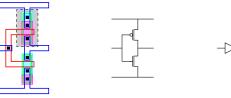
## $0.5~\mu m$ CMOS inverter



5003

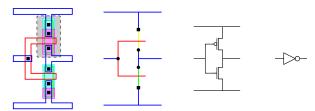
#### Abstraction

#### Levels of Abstraction



- Mask Level Design
- Laborious Technology/Process dependent.
- Design rules may change during a design!
- Transistor Level Design
- Process independent, Technology dependent.
- Gate Level Design
- $Process/Technology\ independent.$

## Abstraction - Stick Diagrams



Stick diagrams give us many of the benefits of abstraction:

- Much easier/faster than full mask specification.
- Process independent (valid for any CMOS process).
- Easy to change.

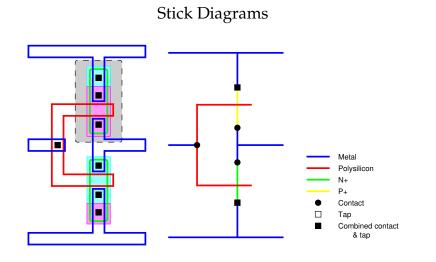
while avoiding some of the problems:

 Optimized layout may be generated much more easily from a stick diagram than from transistor or gate level designs.<sup>1</sup>

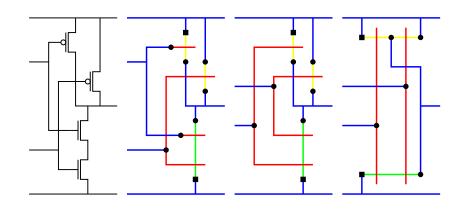
<sup>1</sup>note that all IC designs must end at the mask level.

5005

#### Digital CMOS Design



# Stick Diagrams



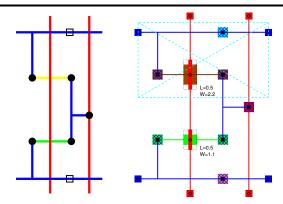
5007

#### Digital CMOS Design

#### Stick Diagrams

- Explore your Design Space.
  - Implications of crossovers.
  - Number of contacts.
  - Arrangement of devices and connections.
- Process independent layout.
- Easy to expand to a full layout for a particular process.

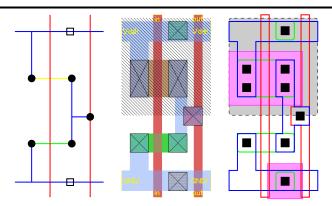
# Sticks and CAD - Symbolic Capture



- Transistors are placed and explicitly sized.
- components are joined with zero width wires.
- contacts are automatically selected as required.
- $\bullet$  A semi-automatic compaction process will create DRC correct layout.

5009

# Sticks and CAD - Magic



- Log style design (sticks with width) DRC errors are flagged immediately. again contacts are automatically selected as required.
- On-line DRC leads to rapid generation of correct designs.
- symbolic capture style compaction is available if desired.

5010