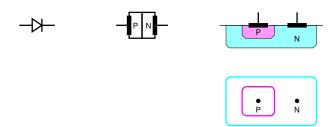
# Components for IC Design

#### Diodes and Bipolar Transistors

Diode



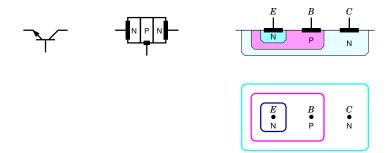
- Ideal structure 1D
- Real structure 3D
- Depth controlled implants.

3001

## Components for IC Design

#### Diodes and Bipolar Transistors

NPN Transistor

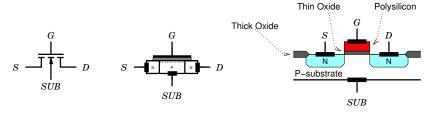


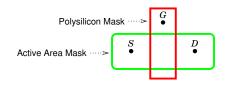
• Two n-type implants.

# Components for IC Design

#### **MOS Transistors**

Simple NMOS Transistor





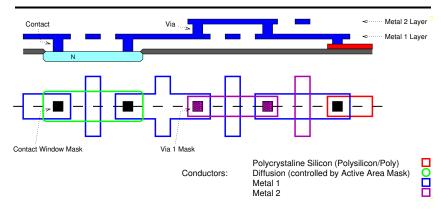
3003

# Components for IC Design

## Simple NMOS Transistor

- Active Area mask defines extent of *Thick Oxide*.
- Polysilicon mask also controls extent of *Thin Oxide* (alias *Gate Oxide*).
- N-type implant has no extra mask.
- It is blocked by thick oxide and by polysilicon.
- The implant is *Self Aligned*.
- Substrate connection is to bottom of wafer.
- All substrates to ground.
- Gate connection not above transistor area.
  - Design Rule.

#### Interconnect

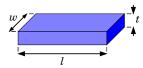


- Crossing conductors on different masks do not interact<sup>1</sup>.
- Explicit contact/via is required for connection.
- Crossing conductors on the same mask are always connected.

 $^{1}$  the exception to this rule is that polysilicon crossing diffusion gives us a transistor 3005

#### Interconnect

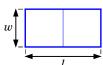
#### Resistance



$$R = \left(\frac{\rho}{t}\right) \left(\frac{l}{w}\right)$$

where  $\rho$  is the resistivity constant  $3.2\times 10^{-8}\Omega m \ \ {\rm for\ aluminium}$   $1.7\times 10^{-8}\Omega m \ \ {\rm for\ copper}$ 

Since t and  $\rho$  are fixed for a paricular mask layer, the value that is normally used is the sheet resistance:  $R_s = \binom{\rho}{t}$ .

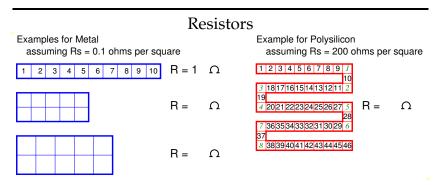


$$R = R_s \left(\frac{l}{w}\right)$$

where  $R_s$  is sheet resistance  $0.1\Omega/\Box$  for 170nm thick copper

 $R_s=$  resistance of a square (i.e. w=l) so the units for  $R_s$  are  $\Omega/\square$  (ohms per square).

## Components for IC Design

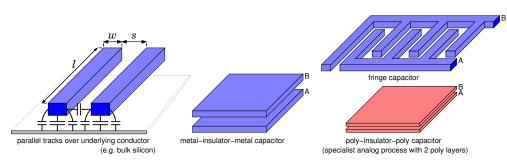


- for larger resistances we need minimum width poly (often combined with a *serpantine* shape) to save on area
- corner squares count as half<sup>2</sup> squares
- for predicatability and matching we may need wider tracks without corners

3007

## Components for IC Design

## Capacitors



- Capacitance to underlying conductor  $C = C_a w l + 2 C_f l$
- Coupling capacitance to adjacent track  $C = C_c \, l/s$ where  $C_a$ ,  $C_f$ ,  $C_c$  are constants for a given layer and process in digital designs our only aim is to minimise parasitic capacitance

<sup>&</sup>lt;sup>2</sup>effective resistance  $\approx 0.56R_s$