

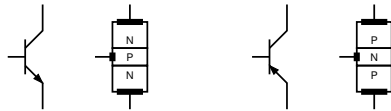
Overview of Technologies

Components for Logic

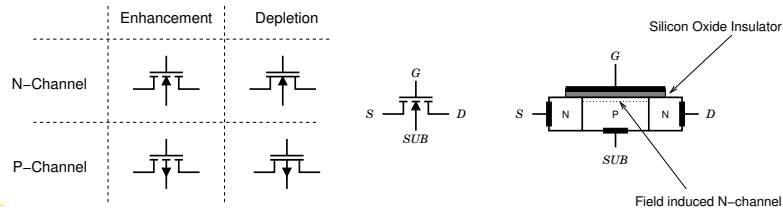
Diode



Bipolar Transistors



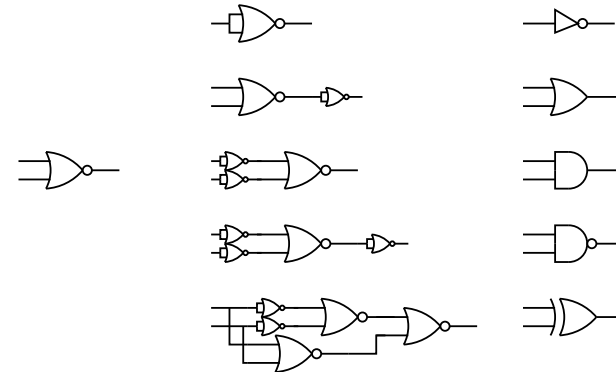
MOS Transistors



2001

Overview of Technologies

All functions can be realized with a single NOR base gate.¹

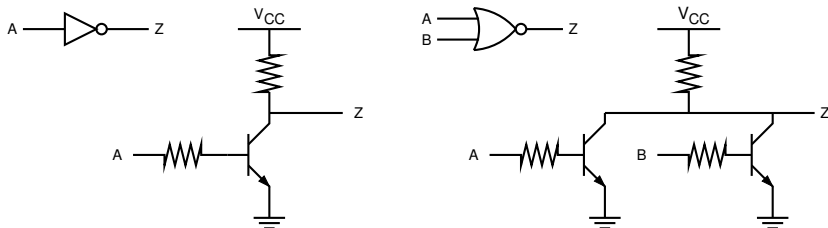


¹NAND gates could be used instead.

2003

Overview of Technologies

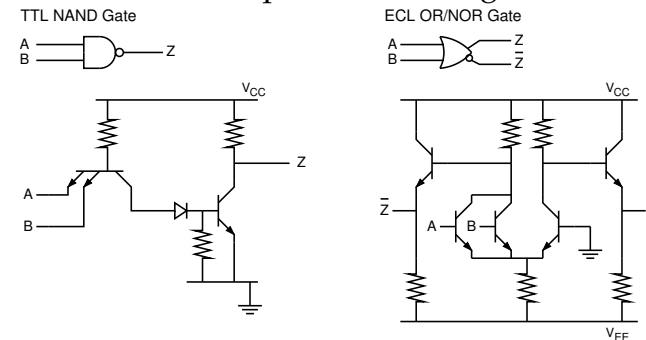
RTL Inverter and NOR gate



2002

Overview of Technologies

Other Bipolar Technologies



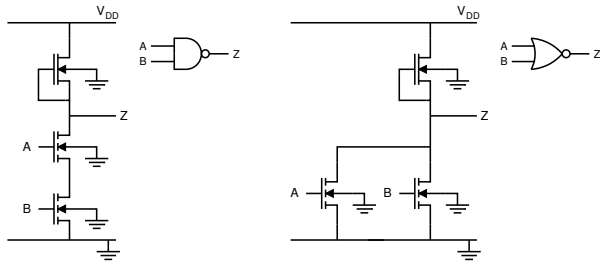
- TTL gives faster switching than RTL at the expense of greater complexity². The characteristic multi-emitter transistor reduces the overall component count.
- ECL is a very high speed, high power, non-saturating technology.

²Most TTL families are more complex than the basic version shown here

2004

Overview of Technologies

NMOS - a VLSI technology.



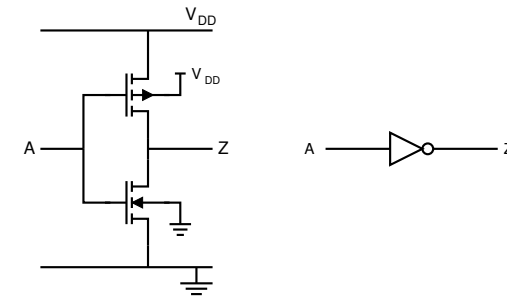
- Circuit function determined by series/parallel combination of devices.
- Depletion transistor acts as non-linear load resistor.
Resistance increases as the enhancement device turns on, thus reducing power consumption.
- The low output voltage is determined by the size ratio of the devices.

2005

Overview of Technologies

CMOS logic

CMOS - state of the art VLSI.

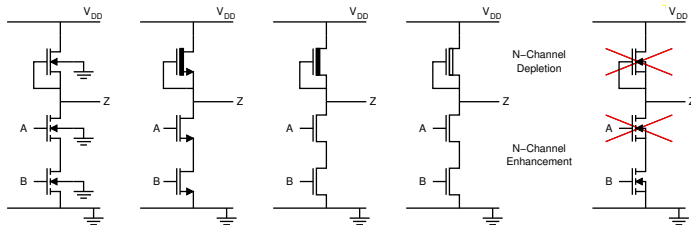


- An active PMOS device complements the NMOS device giving:
 - rail to rail output swing.
 - negligible static power consumption.

2007

Overview of Technologies

Alternative transistors representations for NMOS circuits



Various shorthands are used for simplifying NMOS circuit diagrams.

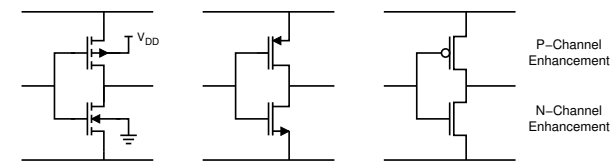
- Substrate connections need not be drawn since all must connect to Gnd.
- Since source and drain are indistinguishable in the layout, there is no need to show the source on the circuit diagram.

Note that schematic tools not designed for IC design will usually include inappropriate 3-terminal symbols.

2006

Digital CMOS Circuits

Alternative transistor representations for CMOS circuits



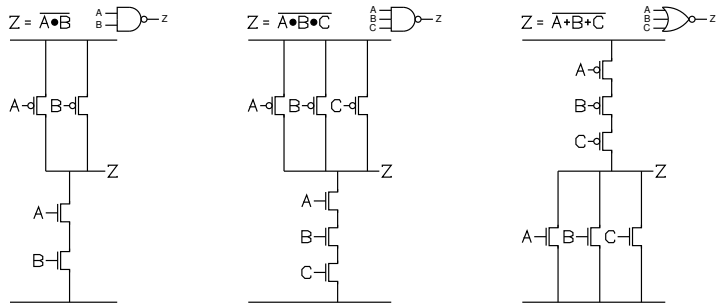
Digital CMOS circuits³ tend to use simplified symbols like their NMOS counterparts.

- In general substrate connections are not drawn where they connect to Vdd (PMOS) and Gnd (NMOS).
- All CMOS devices are enhancement mode.
- Transistors act as simple digitally controlled switches.

³in analog CMOS circuits we may have wells not connected to Vdd/GND

2008

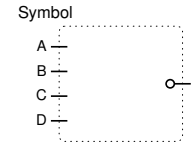
Static CMOS complementary gates



- For any set of inputs there will exist either a path to Vdd or a path to Gnd.

Compound Gate Example

$$Z = \overline{(A \cdot B) + (C \cdot D)}$$



Pull Up Network

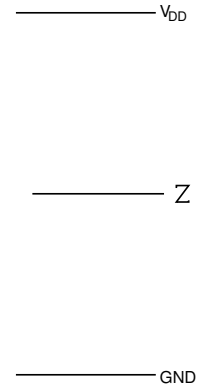
$$Z = f(\bar{A}, \bar{B}, \bar{C}, \bar{D})$$

$$Z = \dots\dots\dots$$

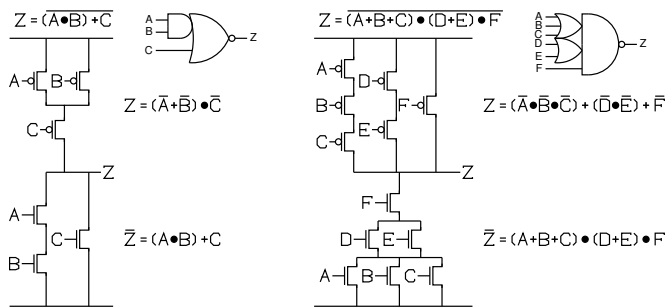
Pull Down Network

$$\bar{Z} = f(A, B, C, D)$$

$$\bar{Z} = (A \cdot B) + (C \cdot D)$$



Compound Gates



- All compound gates are inverting.
- Realisable functions are arbitrary AND/OR expressions with inverted output.