INDEX

	Description "IOACS6C3CSXE04_MT is a[n] IOACS6C3CSXE04 is a non-inverting, CMOS-level, composite IO with a 4X drive, tri-state output buffer piece with active low enable and controlled slew rate output, a programmable pull-up/pull-down/bus-hold piece, and a Schmitt trigger input buffer piece with voltage hysteresis. Contains a 76ux76u bond pad opening." ;
ioacs6c3csxe08_mt	**Description** "IOACS6C3CSXE08_MT is a[n] IOACS6C3CSXE08 is a non-inverting, CMOS-level, composite IO with a 8X drive, tri-state output buffer piece with active low enable and controlled slew rate output, a programmable pull-up/pull-down/bus-hold piece, and a Schmitt trigger input buffer piece with voltage hysteresis. Contains a 76ux76u bond pad opening." ;
ioacs6c3cxxe02_mt	**Description** "IOACS6C3CXXE02_MT is a[n] IOACS6C3CXXE02 is a non-inverting, CMOS-level composite IO with a 2X drive, tri-state output buffer piece with active low enable, a programmable pull-up/pull-down/bus-hold piece, and a Schmitt trigger input buffer piece with voltage hysteresis. Contains a 76ux76u bond pad opening." ;
ioacs6xxcsxe02_mt	**Description** "IOACS6XXCSXE02_MT is a[n] IOACS6XXCSXE02 is a non-inverting, CMOS-level composite IO with a 2X drive, tri-state output buffer piece with active low enable, controlled slew rate output, and a Schmitt trigger input buffer piece with voltage hysteresis. Contains a 76ux76u bond pad opening." ;
ioacs6xxcsxe04_mt	**Description** "IOACS6XXCSXE04_MT is a[n] IOACS6XXCSXE04 is a non-inverting, CMOS-level composite IO with a 4X drive, tri-state output buffer piece with active low enable, controlled slew rate output, and a Schmitt trigger input buffer piece with voltage hysteresis. Contains a 76ux76u bond pad opening." ;
ioacs6xxcsxe08_mt	**Description** "IOACS6XXCSXE08_MT is a[n] IOACS6XXCSXE08 is a non-inverting, CMOS-level composite IO with a 8X drive, tri-state output buffer piece with active low enable, controlled slew rate output, and a Schmitt trigger input buffer piece with voltage hysteresis. Contains a 76ux76u bond pad opening." ;
ioacstptcxte02_mt	**Description** "IOACSTPTCXTE02_MT is a[n] IOACSTPTCXTE02 is a non-inverting, 5v tolerant, CMOS-level Schmitt trigger composite IO with a 2X drive, tri-state output buffer piece with a active low enable and controlled slew rate output, a programmable pull-up/pull-down piece, and input buffer piece. Contains a 76ux76u bond pad opening." ;
ioacx6c3csxe02_mt	**Description** "IOACX6C3CSXE02_MT is a[n] IOACX6C3CSXE02 is a non-inverting, CMOS-level composite IO with at 2X drive, tri-state output buffer piece with a active low enable and controlled slew rate output, a programmable pull-up/pull-down/bus-hold piece, and input buffer piece. Contains a 76ux76u bond pad opening." ;
ioacx6c3csxe04_mt	**Description** "IOACX6C3CSXE04_MT is a[n] IOACX6C3CSXE04 is a non-inverting, CMOS-level composite IO with a 4X drive, tri-state output buffer piece with a active low enable and controlled slew rate output, a programmable pull-up/pull-down/bus-hold piece, and input buffer piece. Contains a 76ux76u bond pad opening." ;
ioacx6c3csxe08_mt	**Description** "IOACX6C3CSXE08_MT is a[n] IOACX6C3CSXE08 is a non-inverting, CMOS-level composite IO with a 8X drive, tri-state output buffer piece with a active low enable and controlled slew rate output, a programmable pull-up/pull-down/bus-hold piece, and input buffer piece. Contains a 76ux76u bond pad opening." ;
ioacx6xxcsxe02_mt	**Description** "IOACX6XXCSXE02_MT is a[n] IOACX6XXCSXE02 is a non-inverting, CMOS-level composite IO with an 2X drive, tri-state output buffer piece with active low enable, controlled slew rate output, and an input buffer piece. Contains a 76ux76u bond pad opening." ;

ioacx6xxcsxe04_mt	**Description** "IOACX6XXCSXE04_MT is a[n] IOACX6XXCSXE04 is a non-inverting, CMOS-level composite IO with an 4X drive, tri-state output buffer piece with active low enable, controlled slew rate output, and an input buffer piece. Contains a 76ux76u bond pad opening." ;
ioacx6xxcsxe08_mt	**Description** "IOACX6XXCSXE08_MT is a[n] IOACX6XXCSXE08 is a non-inverting, CMOS-level composite IO with an 8X drive, tri-state output buffer piece with active low enable, controlled slew rate output, and an input buffer piece. Contains a 76ux76u bond pad opening." ;
ioacxtxxcste08_mt	**Description** "IOACXTXXCSTE08_MT is a[n] IOACXTXXCSTE08 is a 5V-tolerant, non-inverting, CMOS-level composite IO with a 8X drive, tri-state output buffer piece that has a active low enable and controlled slew rate output, and an input buffer piece. Contains a 76ux76u bond pad opening." ;
ioavx6c3vxxe02_mt	**Description** "IOAVX6C3VXXE02_MT is a[n] IOAVX6C3VXXE02 is a non-inverting, LVTTL-level composite IO with a 2X drive, tri-state output buffer piece with a active low enable and controlled slew rate output, a programmable pull-up/pull-down/bus-hold piece, and input buffer piece. Contains a 76ux76u bond pad opening." ;
iosna4_mt	**Description** "IOSNA4_MT is a[n] IOSNA4 is a non-buffered, resistive analog interface input piece. Contains a 76ux76u bond pad opening." ;
obac3csxe02_mt	**Description** "OBAC3CSXE02_MT is a[n] OBAC3CSXE02 is a 2X drive, non-inverting, CMOS-level, tri-state composite output buffer with a programmable pull-up/pull-down/bus-hold piece, active low enable and controlled slew rate output. Contains a 76ux76u bond pad opening." ;
obac3csxe04_mt	**Description** "OBAC3CSXE04_MT is a[n] OBAC3CSXE04 is a 4X drive, non-inverting, CMOS-level, tri-state composite output buffer with a programmable pull-up/pull-down/bus-hold piece, active low enable and controlled slew rate output. Contains a 76ux76u bond pad opening." ;
obac3csxe08_mt	**Description** "OBAC3CSXE08_MT is a[n] OBAC3CSXE08 is a 8X drive, non-inverting, CMOS-level, tri-state composite output buffer with a programmable pull-up/pull-down/bus-hold piece, active low enable and controlled slew rate output. Contains a 76ux76u bond pad opening." ;
obac3cxxe08_mt	**Description** "OBAC3CXXE08_MT is a[n] OBAC3CXXE08 is an 8X drive, non-inverting, CMOS-level, tri-state composite output buffer with a programmable pull-up/pull-down/bus-hold piece and active low enable. Contains a 76ux76u bond pad opening." ;
obaptcxte08_mt	**Description** "OBAPTCXTE08_MT is a[n] OBAPTCXTE08 is an 8X drive, 5V-tolerant, non-inverting, CMOS-level, tri-state composite output buffer with a programmable pull-up/pull-down/bus-hold piece and a active low enable. Contains a 76ux76u bond pad opening." ;
obaxxcste02_mt	**Description** "OBAXXCSTE02_MT is a[n] OBAXXCSTE02 is an 2X drive, 5V-tolerant, non-inverting, CMOS-level, tri-state composite output buffer with active low enable and controlled slew rate output. Contains a 76ux76u bond pad opening." ;
obaxxcsxe02_mt	**Description** "OBAXXCSXE02_MT is a[n] OBAXXCSXE02 is a 2X drive, non-inverting, CMOS-level, tri-state composite output buffer with active low enable and controlled slew rate output. Contains a 76ux76u bond pad opening." ;
obaxxcsxe04_mt	

	Description "OBAXXCSXE04_MT is a[n] OBAXXCSXE04 is a 4X drive, non-inverting, CMOS-level, tri-state composite output buffer with active low enable and controlled slew rate output. Contains a 76ux76u bond pad opening." ;
obaxxcsxe08_mt	**Description** "OBAXXCSXE08_MT is a[n] OBAXXCSXE08 is a 8X drive, non-inverting, CMOS-level, tri-state composite output buffer with active low enable and controlled slew rate output. Contains a 76ux76u bond pad opening." ;
obaxxcxte02_mt	**Description** "OBAXXCXTE02_MT is a[n] OBAXXCXTE02 is an 2X drive, 5V-tolerant, non-inverting, CMOS-level, tri-state composite output buffer with active low enable. Contains a 76ux76u bond pad opening." ;
obaxxvxxe02_mt	**Description** "OBAXXVXXE02_MT is a[n] OBAXXVXXE02 is an 2X drive, non-inverting, LVTTL-level, composite output buffer. Contains a 76ux76u bond pad opening." ;
obaxxvxxe08_mt	**Description** "OBAXXVXXE08_MT is a[n] OBAXXVXXE08 is an 8X drive, non-inverting, LVTTL-level, composite output buffer. Contains a 76ux76u bond pad opening." ;
zgppxbg_mt	**Description** "ZGPPXBG_MT is a[n] ZGPPXBG is a[n] VSS ground pad driving core ground and OGND bus with grounded gate NMOS protection. All supplies should be 3.6V or less. Contains a 76ux76u bond pad opening." ;
zgppxbp_mt	**Description** "ZGPPXBP_MT is a[n] ZGPPXBP is a[n] VDD power pad driving core power and OPWR bus with grounded gate NMOS protection. All supplies should be 3.6V or less. Contains a 76ux76u bond pad opening." ;
zgppxcg_mt	**Description** "ZGPPXCG_MT is a[n] ZGPPXCG is a[n] VSS ground pad driving core ground with anti-parallel diodes from core ground to OGND bus. All supplies should be 3.6V or less. Contains a 76ux76u bond pad opening." ;
zgppxcp_mt	**Description** "ZGPPXCP_MT is a[n] ZGPPXCP is a[n] VDD power pad driving core power with grounded gate NMOS protection on CPWR. All supplies should be 3.6V or less. Contains a 76ux76u bond pad opening." ;
zgppxpg_mt	**Description** "ZGPPXPG_MT is a[n] ZGPPXPG is a[n] VSS ground pad driving OGND with grounded gate NMOS protection. All supplies should be 3.6V or less. Contains a 76ux76u bond pad opening." ;
zgppxpp_mt	**Description** "ZGPPXPP_MT is a[n] ZGPPXPP is a[n] VDD power pad driving OPWR with grounded gate NMOS protection. All supplies should be 3.6V or less. Contains a 76ux76u bond pad opening." ;
zgppxsb_mt	**Description** "ZGPPXSB_MT is a[n] ZGPPXSB is a[n] SUB ground pad with grounded gate NMOS protection from SUB to OGND. Difference between SUB and OGND should be 3.6V or less. Contains a 76ux76u bond pad opening." ;

clamp_inline_bus_cut_mt

Description

"CLAMP_INLINE_BUS_CUT_MT is a[n] CLAMP_INLINE_BUS_CUT is a[n] RC Clamp with bus cut on OPWR bus" ;

Logic Symbol

AREA : 19414.5 sqr microns

Power Characteristics:

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	2.48873e-05	uW

Power Characteristics:

Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	0.000252121	uW

Power Characteristics:

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	0.0725256	uW

clamp_inline_mt

Description
"CLAMP_INLINE_MT is a[n] CLAMP_INLINE is a[n] RC Clamp." ;

Logic Symbol

AREA : 9707.25 sqr microns

Power Characteristics:
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	1.24436e-05	uW

Power Characteristics:
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	0.000126061	uW

Power Characteristics:
Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	0.0362628	uW

clamp_inline_sb_mt

Description

"CLAMP_INLINE_SB_MT is a[n] CLAMP_INLINE_SB is a[n] RC Clamp that clamps OGND to SUB" ;

Logic Symbol

AREA : 9707.25 sqr microns

Power Characteristics:

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	2.64244e-08	uW

Power Characteristics:

Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	8.32333e-08	uW

Power Characteristics:

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	0.00554012	uW

corns_clamp_bus_cut_mt

Description
"CORNS_CLAMP_BUS_CUT_MT is a[n] CORNS_CLAMP_BUS_CUT is a corner cell with a[n] RC Clamp and includes bus cut on OPWR bus" ;

Logic Symbol

AREA : 104006.25 sqr microns

Power Characteristics:
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	7.10553e-05	uW

Power Characteristics:
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	0.000752156	uW

Power Characteristics:
Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	0.244157	uW

corns_clamp_mt

Description
"CORNS_CLAMP_MT is a[n] CORNS_CLAMP is a corner cell with a[n] RC Clamp." ;

Logic Symbol

AREA : 104006.25 sqr microns

Power Characteristics:
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	7.10616e-05	uW

Power Characteristics:
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	0.000752159	uW

Power Characteristics:
Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

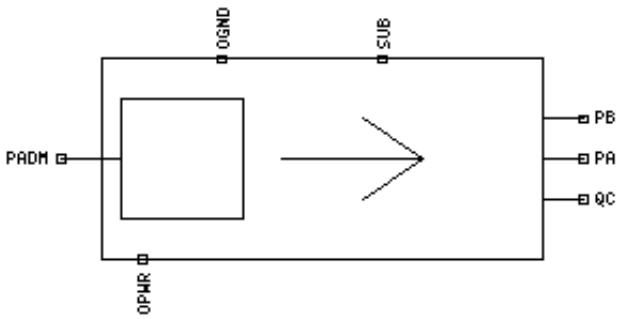
Name	Value	Units
Cell Leakage Power	0.244157	uW

ibacs6c3_mt

Description

"IBACS6C3_MT is a[n] IBACS6C3 is a non-inverting, CMOS-level Schmitt trigger composite input buffer with voltage hysteresis and a programmable pull-up/pull-down/bus-hold piece. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
PA	0.0382323 (pF)
PB	0.0387371 (pF)
PADM	6.78127 (pF)

AREA : 27735.0 sqr microns

Truth Table

PA input	PADM input	PB input	QC output
?	L	?	L
?	H	?	H

IL = Illegal Z = High Impedence ? = Dont Care NC = No Change

Pull Cell Truth Table :

PA	PB	Function
0	0	Pull Down
0	1	Tristate
1	0	Bus Keeper
1	1	Pull Up

Power Characteristics:

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	525.718	uW

Power Characteristics:
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	282.664	uW

Power Characteristics:
Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	128.821	uW

Delay Characteristics: Time Units 1ns
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.147080**	**0.649310**	**1.60840**	**3.10260**	**5.19920**	**7.95800**
PADM to QC	TPLH	0.400000	0.542000	0.846000	1.23600	1.72400	2.32600	3.05300
PADM to QC	TPHL	0.378000	0.549000	0.902000	1.40100	2.07400	2.94700	4.04200

Delay Characteristics: Time Units 1ns
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.147080**	**0.649310**	**1.60840**	**3.10260**	**5.19920**	**7.95800**
PADM to QC	TPLH	0.587000	0.769000	1.24300	1.87200	2.69300	3.72900	5.00400
PADM to QC	TPHL	0.573000	0.789000	1.30000	1.99600	2.91900	4.10200	5.57300

Delay Characteristics: Time Units 1ns
Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.147080**	**0.649310**	**1.60840**	**3.10260**	**5.19920**	**7.95800**
PADM to QC	TPLH	1.18500	1.37400	2.13900	3.27200	4.75400	6.63000	8.94000
PADM to QC	TPHL	1.16800	1.39400	2.21400	3.37700	4.89300	6.81400	9.18000

Test Data

Parameter	Description	Minimum	Maximum	Units
Vih	High Level Input Voltage	(0.8*Vdd)	-	V
Vil	High Level Input Voltage	-	(0.2*Vdd)	V
Vhys	Schmitt Threshold	(0.21*Vdd)	Vdd	V
ipu	Pull up current	-161.0	-40.0	uA
ipd	Pull down current	32.0	192.0	uA
ibkpu	Buskeeper pull-up current	-110.0	-28.0	uA
vtestbkpu	Test voltage for keeping the bus keeper pin high	(0.7*Vdd)	-	V
ibkpd	Buskeeper pull-down current	21.0	139.0	uA

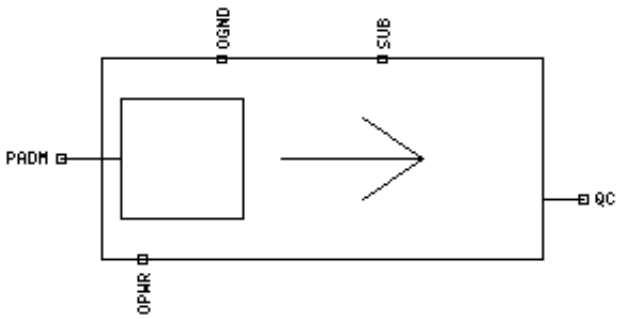
vtestbkpd	Test voltage for keeping the bus keeper pin lob	-	(0.3*Vdd)	V
Iil	Low Level Input Current	-1.0	1.0	uA
Iih	High Level Input Current	-1.0	1.0	uA
Vdiode_vdd	Diode voltage range to Vdd	0.20	1.10	V
Vi_max	Maximum Voltage	-0.5	(1.10 * Vdd)	V
I_max	Maximum sink/source current	-100	100	mA
Vdiode_vss	Diode voltage to Vss	-1.10	-0.20	V

ibacs6xx_mt

Description

"IBACS6XX_MT is a[n] IBACS6XX is a non-inverting, CMOS-level Schmitt trigger composite input buffer with voltage hysteresis. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
PADM	4.74013 (pF)

AREA : 27735.0 sqr microns

Truth Table

PADM input	QC output
L	L
H	H

IL = Illegal Z = High Impedence ? = Dont Care NC = No Change

Power Characteristics:

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	6.01731e-05	uW

Power Characteristics:

Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units

Cell Leakage Power	3.09407e-05	uW

Power Characteristics:

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	0.0537457	uW

Delay Characteristics: Time Units 1ns

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.147090**	**0.649360**	**1.60850**	**3.10280**	**5.19950**	**7.95850**
PADM to QC	TPLH	0.401000	0.542000	0.846000	1.23600	1.72500	2.32700	3.05400
PADM to QC	TPHL	0.379000	0.549000	0.903000	1.40200	2.07500	2.94800	4.04300

Delay Characteristics: Time Units 1ns

Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.147090**	**0.649360**	**1.60850**	**3.10280**	**5.19950**	**7.95850**
PADM to QC	TPLH	0.588000	0.770000	1.24300	1.87200	2.69300	3.73000	5.00500
PADM to QC	TPHL	0.574000	0.790000	1.30000	1.99700	2.92000	4.10300	5.57400

Delay Characteristics: Time Units 1ns

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.147090**	**0.649360**	**1.60850**	**3.10280**	**5.19950**	**7.95850**
PADM to QC	TPLH	1.18700	1.37500	2.13900	3.27300	4.75500	6.63100	8.94100
PADM to QC	TPHL	1.16900	1.39500	2.21500	3.37700	4.89400	6.81400	9.18100

Test Data

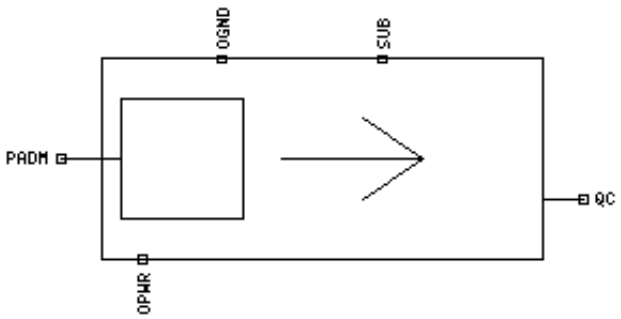
Parameter	Description	Minimum	Maximum	Units
Vih	High Level Input Voltage	(0.8*Vdd)	-	V
Vil	High Level Input Voltage	-	(0.2*Vdd)	V
Vhys	Schmitt Threshold	(0.21*Vdd)	Vdd	V
Iil	Low Level Input Current	-1.0	1.0	uA
Iih	High Level Input Current	-1.0	1.0	uA
Vdiode_vdd	Diode voltage range to Vdd	0.20	1.10	V
Vi_max	Maximum Voltage	-0.5	(1.10 * Vdd)	V
I_max	Maximum sink/source current	-100	100	mA
Vdiode_vss	Diode voltage to Vss	-1.10	-0.20	V

ibacstxx_mt

Description

"IBACSTXX_MT is a[n] IBACSTXX is a non-inverting, 5v tolerant, CMOS-level Schmitt trigger composite input buffer with voltage hysteresis. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
PADM	5.40101 (pF)

AREA : 27735.0 sqr microns

Truth Table

PADM input	QC output
L	L
H	H

IL = Illegal Z = High Impedence ? = Dont Care NC = No Change

Power Characteristics:

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	8.50131e-05	uW

Power Characteristics:

Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units

Cell Leakage Power	4.01092e-05	uW

Power Characteristics:

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	0.0510846	uW

Delay Characteristics: Time Units 1ns

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.143930**	**0.635100**	**1.57310**	**3.03440**	**5.08480**	**7.78280**
PADM to QC	TPLH	0.695000	0.745000	1.02500	1.50700	2.16500	3.01300	4.06700
PADM to QC	TPHL	0.582000	0.719000	1.19800	1.99000	3.11200	4.60100	6.49600

Delay Characteristics: Time Units 1ns

Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.143930**	**0.635100**	**1.57310**	**3.03440**	**5.08480**	**7.78280**
PADM to QC	TPLH	1.32700	1.30600	1.52800	2.03200	2.73100	3.61000	4.68100
PADM to QC	TPHL	0.941000	1.06600	1.55800	2.36200	3.49900	4.99100	6.86700

Delay Characteristics: Time Units 1ns

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.143930**	**0.635100**	**1.57310**	**3.03440**	**5.08480**	**7.78280**
PADM to QC	TPLH	3.40100	3.27500	3.35800	3.90100	4.89300	6.24800	7.92400
PADM to QC	TPHL	1.95000	2.10700	2.72100	3.76700	5.18900	7.04000	9.35000

Test Data

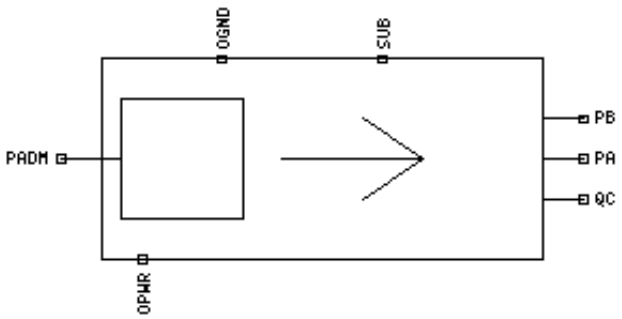
Parameter	Description	Minimum	Maximum	Units
Vih	High Level Input Voltage	(0.8*Vdd)	-	V
Vil	High Level Input Voltage	-	(0.2*Vdd)	V
Vhys	Schmitt Threshold	(0.189*Vdd)	Vdd	V
Iil	Low Level Input Current	-1.0	1.0	uA
Iih	High Level Input Current	-1.0	1.0	uA
Vi_max	Maximum Voltage	-0.5	5.0	V
I_max	Maximum sink/source current	-100	100	mA
Vdiode_vss	Diode voltage to Vss	-1.10	-0.20	V

ibacx6c3_mt

Description

"IBACX6C3_MT is a[n] IBACX6C3 is a non-inverting, CMOS-level composite input buffer with a programmable pull-up/pull-down/bus-hold piece. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
PA	0.0382265 (pF)
PB	0.0387319 (pF)
PADM	6.77141 (pF)

AREA : 27735.0 sqr microns

Truth Table

PA input	PADM input	PB input	QC output
?	L	?	L
?	H	?	H

IL = Illegal Z = High Impedence ? = Dont Care NC = No Change

Pull Cell Truth Table :

PA	PB	Function
0	0	Pull Down
0	1	Tristate
1	0	Bus Keeper
1	1	Pull Up

Power Characteristics:

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	525.718	uW

Power Characteristics:
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	282.664	uW

Power Characteristics:
Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	128.821	uW

Delay Characteristics: Time Units 1ns
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.143910**	**0.635010**	**1.57290**	**3.03400**	**5.08410**	**7.78170**
PADM to QC	TPLH	0.267000	0.398000	0.643000	0.997000	1.48000	2.11100	2.90700
PADM to QC	TPHL	0.282000	0.420000	0.687000	1.06700	1.58300	2.25200	3.09500

Delay Characteristics: Time Units 1ns
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.143910**	**0.635010**	**1.57290**	**3.03400**	**5.08410**	**7.78170**
PADM to QC	TPLH	0.378000	0.531000	0.829000	1.22100	1.73800	2.39500	3.20700
PADM to QC	TPHL	0.415000	0.610000	1.03800	1.67400	2.56100	3.73000	5.21000

Delay Characteristics: Time Units 1ns
Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.143910**	**0.635010**	**1.57290**	**3.03400**	**5.08410**	**7.78170**
PADM to QC	TPLH	0.719000	0.947000	1.45200	2.19100	3.19300	4.48700	6.10300
PADM to QC	TPHL	0.795000	1.07600	1.71500	2.69300	4.06200	5.86800	8.15300

Test Data

Parameter	Description	Minimum	Maximum	Units
Vih	High Level Input Voltage	(0.7*Vdd)	-	V
Vil	High Level Input Voltage	-	(0.3*Vdd)	V
ipu	Pull up current	-161.0	-40.0	uA
ipd	Pull down current	32.0	192.0	uA
ibkpu	Buskeeper pull-up current	-110.0	-28.0	uA
vtestbkpu	Test voltage for keeping the bus keeper pin high	(0.7*Vdd)	-	V
ibkpd	Buskeeper pull-down current	21.0	139.0	uA
vtestbkpd	Test voltage for keeping the bus keeper pin lob	-	(0.3*Vdd)	V

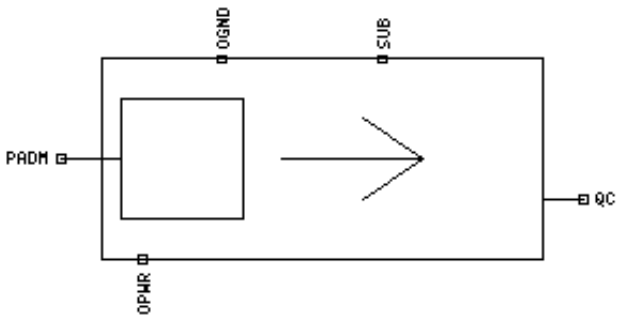
Iil	Low Level Input Current	-1.0	1.0	uA
Iih	High Level Input Current	-1.0	1.0	uA
Vdiode_vdd	Diode voltage range to Vdd	0.20	1.10	V
Vi_max	Maximum Voltage	-0.5	(1.10 * Vdd)	V
I_max	Maximum sink/source current	-100	100	mA
Vdiode_vss	Diode voltage to Vss	-1.10	-0.20	V

ibacx6xx_mt

Description

"IBACX6XX_MT is a[n] IBACX6XX is a non-inverting, CMOS-level composite input buffer. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
PADM	4.7303 (pF)

AREA : 27735.0 sqr microns

Truth Table

PADM input	QC output
L	L
H	H

IL = Illegal Z = High Impedence ? = Dont Care NC = No Change

Power Characteristics:

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	4.90903e-05	uW

Power Characteristics:

Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units

Cell Leakage Power	2.77048e-05	uW

Power Characteristics:

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	0.0537799	uW

Delay Characteristics: Time Units 1ns

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.143910**	**0.635010**	**1.57290**	**3.03400**	**5.08410**	**7.78170**
PADM to QC	TPLH	0.268000	0.398000	0.644000	0.998000	1.48000	2.11100	2.90700
PADM to QC	TPHL	0.282000	0.421000	0.687000	1.06800	1.58400	2.25300	3.09500

Delay Characteristics: Time Units 1ns

Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.143910**	**0.635010**	**1.57290**	**3.03400**	**5.08410**	**7.78170**
PADM to QC	TPLH	0.378000	0.532000	0.829000	1.22200	1.73800	2.39500	3.20800
PADM to QC	TPHL	0.415000	0.611000	1.03900	1.67500	2.56200	3.73000	5.21100

Delay Characteristics: Time Units 1ns

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.143910**	**0.635010**	**1.57290**	**3.03400**	**5.08410**	**7.78170**
PADM to QC	TPLH	0.720000	0.948000	1.45300	2.19200	3.19300	4.48800	6.10400
PADM to QC	TPHL	0.795000	1.07700	1.71500	2.69300	4.06300	5.86800	8.15300

Test Data

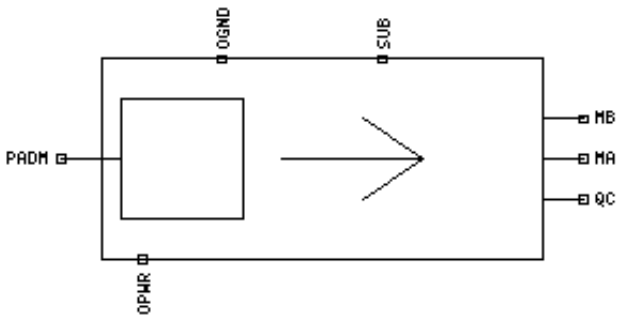
Parameter	Description	Minimum	Maximum	Units
Vih	High Level Input Voltage	(0.7*Vdd)	-	V
Vil	High Level Input Voltage	-	(0.3*Vdd)	V
Iil	Low Level Input Current	-1.0	1.0	uA
Iih	High Level Input Current	-1.0	1.0	uA
Vdiode_vdd	Diode voltage range to Vdd	0.20	1.10	V
Vi_max	Maximum Voltage	-0.5	(1.10 * Vdd)	V
I_max	Maximum sink/source current	-100	100	mA
Vdiode_vss	Diode voltage to Vss	-1.10	-0.20	V

ibacxtpt_mt

Description

"IBACXTPT_MT is a[n] IBACXTPT is a 5V-tolerant, non-inverting, CMOS-level composite input buffer with a programmable pull-up/pull-down/bus-hold piece. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
PADM	7.276 (pF)
MA	0.0293763 (pF)
MB	0.0397068 (pF)

AREA : 27735.0 sqr microns

Truth Table

MA input	MB input	PADM input	QC output
?	?	L	L
?	?	H	H

IL = Illegal Z = High Impedence ? = Dont Care NC = No Change

Pull Cell Truth Table :

MA	MB	Function
0	0	Pull Down
0	1	Tristate
1	0	Tristate
1	1	Pull Up

Power Characteristics:

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	508.752	uW

Power Characteristics:
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	270.507	uW

Power Characteristics:
Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	116.107	uW

Delay Characteristics: Time Units 1ns
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.147050**	**0.649200**	**1.60810**	**3.10210**	**5.19820**	**7.95650**
PADM to QC	TPLH	0.366000	0.486000	0.768000	1.18800	1.76500	2.52100	3.47500
PADM to QC	TPHL	0.340000	0.489000	0.772000	1.18800	1.74800	2.47200	3.37800

Delay Characteristics: Time Units 1ns
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.147050**	**0.649200**	**1.60810**	**3.10210**	**5.19820**	**7.95650**
PADM to QC	TPLH	0.591000	0.682000	0.993000	1.44400	2.04300	2.81000	3.75800
PADM to QC	TPHL	0.504000	0.717000	1.16100	1.84300	2.79500	4.04700	5.62600

Delay Characteristics: Time Units 1ns
Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.147050**	**0.649200**	**1.60810**	**3.10210**	**5.19820**	**7.95650**
PADM to QC	TPLH	1.37500	1.40300	1.79100	2.52900	3.57100	4.92300	6.60800
PADM to QC	TPHL	0.946000	1.25400	1.94700	2.99000	4.46100	6.40500	8.85900

Test Data

Parameter	Description	Minimum	Maximum	Units
Vih	High Level Input Voltage	(0.7*Vdd)	-	V
Vil	High Level Input Voltage	-	(0.3*Vdd)	V
ipu	Pull up current	-155.0	-36.0	uA
ipd	Pull down current	28.0	191.0	uA
Iil	Low Level Input Current	-1.0	1.0	uA
Iih	High Level Input Current	-1.0	1.0	uA
Vi_max	Maximum Voltage	-0.5	5.0	V
I_max	Maximum sink/source current	-100	100	mA

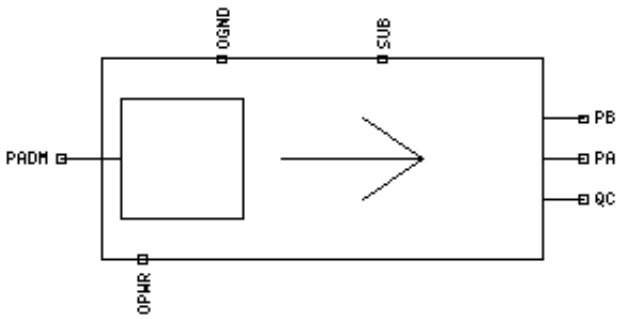
Vdiode_vss	Diode voltage to Vss	-1.10	-0.20	V

ibavs6c3_mt

Description

"IBAVS6C3_MT is a[n] IBAVS6C3 is a non-inverting, LVTTL-level Schmitt trigger composite input buffer with voltage hysteresis and a programmable pull-up/pull-down/bus-hold piece. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
PA	0.0382265 (pF)
PB	0.0387319 (pF)
PADM	6.78102 (pF)

AREA : 27735.0 sqr microns

Truth Table

PA input	PADM input	PB input	QC output
?	L	?	L
?	H	?	H

IL = Illegal Z = High Impedence ? = Dont Care NC = No Change

Pull Cell Truth Table :

PA	PB	Function
0	0	Pull Down
0	1	Tristate
1	0	Bus Keeper
1	1	Pull Up

Power Characteristics:

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	525.718	uW

Power Characteristics:
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	282.664	uW

Power Characteristics:
Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	128.821	uW

Delay Characteristics: Time Units 1ns
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.143890**	**0.634930**	**1.57260**	**3.03360**	**5.08340**	**7.78070**
PADM to QC	TPLH	0.327000	0.488000	0.770000	1.12600	1.56800	2.11000	2.76500
PADM to QC	TPHL	0.352000	0.508000	0.863000	1.40000	2.15100	3.14300	4.40200

Delay Characteristics: Time Units 1ns
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.143890**	**0.634930**	**1.57260**	**3.03360**	**5.08340**	**7.78070**
PADM to QC	TPLH	0.466000	0.688000	1.14200	1.75100	2.55000	3.56100	4.80700
PADM to QC	TPHL	0.534000	0.731000	1.19300	1.84500	2.73300	3.88600	5.33400

Delay Characteristics: Time Units 1ns
Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.143890**	**0.634930**	**1.57260**	**3.03360**	**5.08340**	**7.78070**
PADM to QC	TPLH	0.890000	1.19100	1.97400	3.10800	4.63800	6.60600	9.05700
PADM to QC	TPHL	1.10200	1.30500	2.05600	3.09500	4.46000	6.19900	8.35400

Test Data

Parameter	Description	Minimum	Maximum	Units
Vih	High Level Input Voltage	2.1v	-	V
Vil	High Level Input Voltage	-	0.7v	V
Vhys	Schmitt Threshold	0.4v	Vdd	V
ipu	Pull up current	-161.0	-40.0	uA
ipd	Pull down current	32.0	192.0	uA
ibkpu	Buskeeper pull-up current	-110.0	-28.0	uA
vtestbkpu	Test voltage for keeping the bus keeper pin high	(0.7*Vdd)	-	V
ibkpd	Buskeeper pull-down current	21.0	139.0	uA

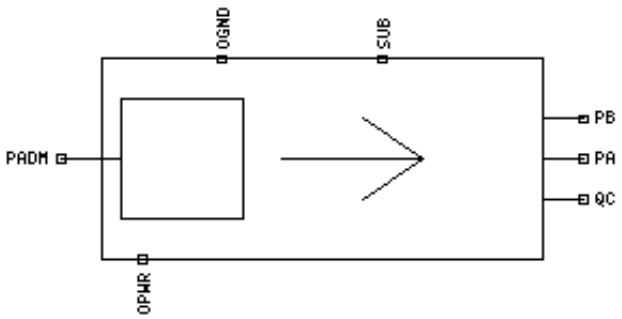
vtestbkpd	Test voltage for keeping the bus keeper pin lob	-	(0.3*Vdd)	V
Iil	Low Level Input Current	-1.0	1.0	uA
Iih	High Level Input Current	-1.0	1.0	uA
Vdiode_vdd	Diode voltage range to Vdd	0.20	1.10	V
Vi_max	Maximum Voltage	-0.5	(1.10 * Vdd)	V
I_max	Maximum sink/source current	-100	100	mA
Vdiode_vss	Diode voltage to Vss	-1.10	-0.20	V

ibavx6c3_mt

Description

"IBAVX6C3_MT is a[n] IBAVX6C3 is a non-inverting, LVTTL-level composite input buffer with a programmable pull-up/pull-down/bus-hold piece. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
PA	0.0382265 (pF)
PB	0.0387319 (pF)
PADM	6.77135 (pF)

AREA : 27735.0 sqr microns

Truth Table

PA input	PADM input	PB input	QC output
?	L	?	L
?	H	?	H

IL = Illegal Z = High Impedence ? = Dont Care NC = No Change

Pull Cell Truth Table :

PA	PB	Function
0	0	Pull Down
0	1	Tristate
1	0	Bus Keeper
1	1	Pull Up

Power Characteristics:

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	525.718	uW

Power Characteristics:
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	282.664	uW

Power Characteristics:
Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	128.821	uW

Delay Characteristics: Time Units 1ns
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.143910**	**0.635010**	**1.57290**	**3.03400**	**5.08410**	**7.78170**
PADM to QC	TPLH	0.264000	0.390000	0.626000	0.970000	1.44200	2.06000	2.84300
PADM to QC	TPHL	0.255000	0.393000	0.679000	1.10800	1.70700	2.50000	3.51100

Delay Characteristics: Time Units 1ns
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.143910**	**0.635010**	**1.57290**	**3.03400**	**5.08410**	**7.78170**
PADM to QC	TPLH	0.377000	0.531000	0.839000	1.26100	1.83000	2.57000	3.49600
PADM to QC	TPHL	0.370000	0.553000	0.968000	1.59800	2.48900	3.67300	5.18000

Delay Characteristics: Time Units 1ns
Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.143910**	**0.635010**	**1.57290**	**3.03400**	**5.08410**	**7.78170**
PADM to QC	TPLH	0.713000	0.964000	1.49600	2.29200	3.39500	4.84100	6.66400
PADM to QC	TPHL	0.711000	0.961000	1.55200	2.47400	3.77600	5.50200	7.69200

Test Data

Parameter	Description	Minimum	Maximum	Units
Vih	High Level Input Voltage	2.0v	-	V
Vil	High Level Input Voltage	-	0.8v	V
ipu	Pull up current	-161.0	-40.0	uA
ipd	Pull down current	32.0	192.0	uA
ibkpu	Buskeeper pull-up current	-110.0	-28.0	uA
vtestbkpu	Test voltage for keeping the bus keeper pin high	(0.7*Vdd)	-	V
ibkpd	Buskeeper pull-down current	21.0	139.0	uA
vtestbkpd	Test voltage for keeping the bus keeper pin lob	-	(0.3*Vdd)	V

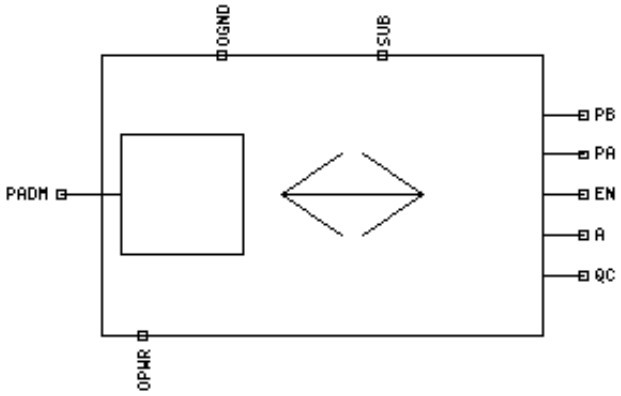
Iil	Low Level Input Current	-1.0	1.0	uA
Iih	High Level Input Current	-1.0	1.0	uA
Vdiode_vdd	Diode voltage range to Vdd	0.20	1.10	V
Vi_max	Maximum Voltage	-0.5	(1.10 * Vdd)	V
I_max	Maximum sink/source current	-100	100	mA
Vdiode_vss	Diode voltage to Vss	-1.10	-0.20	V

ioacs6c3csxe02_mt

Description

"IOACS6C3CSXE02_MT is a[n] IOACS6C3CSXE02 is a non-inverting, CMOS-level, composite IO with a 2X drive, tri-state output buffer piece with active low enable and controlled slew rate output, a programmable pull-up/pull-down/bus-hold piece, and a Schmitt trigger input buffer piece with voltage hysteresis. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
PA	0.0382265 (pF)
A	0.0311864 (pF)
PB	0.0388944 (pF)
PADM	6.78035 (pF)
EN	0.0343174 (pF)

AREA : 27735.0 sqr microns

Truth Table

A input	EN input	PA input	PB input	PADM inout	QC output
L	L	?	?	L	L
L	H	?	?	Z	?
H	L	?	?	H	H
H	H	?	?	Z	?

IL = Illegal Z = High Impedence ? = Dont Care NC = No Change

Pull Cell Truth Table :

PA	PB	Function
0	0	Pull Down
0	1	Tristate

1	0	Bus Keeper
1	1	Pull Up

Power Characteristics:

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	607.437	uW

Power Characteristics:

Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	282.664	uW

Power Characteristics:

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	128.821	uW

Delay Characteristics: Time Units 1ns

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.147070**	**0.649290**	**1.60830**	**3.10250**	**5.19900**	**7.95770**
PADM to QC	TPLH	0.400000	0.542000	0.846000	1.23600	1.72500	2.32600	3.05300
PADM to QC	TPHL	0.378000	0.549000	0.902000	1.40200	2.07400	2.94700	4.04200

Delay Characteristics: Time Units 1ns

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		9.28035	**12.3833**	**23.2753**	**44.0753**	**76.4813**	**121.950**	**181.780**
A to PADM	TPLH	2.01300	2.53800	4.27000	7.43800	12.2870	19.0390	27.8860
A to PADM	TPHL	1.70900	2.11200	3.36900	5.58700	8.94900	13.6080	19.6990
EN to PADM three_state_disable	TLZ	0.249000						
EN to PADM three_state_disable	THZ	0.278000						
EN to PADM three_state_enable	TZH	2.68400	3.01000	4.22400	7.04900	11.5230	17.7560	25.9300
EN to PADM three_state_enable	TZL	2.42000	2.63100	3.42800	5.39100	8.57800	12.9960	18.7720

Delay Characteristics: Time Units 1ns

Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.147070**	**0.649290**	**1.60830**	**3.10250**	**5.19900**	**7.95770**
PADM to QC	TPLH	0.587000	0.769000	1.24300	1.87200	2.69300	3.72900	5.00400
PADM to QC	TPHL	0.574000	0.789000	1.30000	1.99600	2.91900	4.10200	5.57300

Delay Characteristics: Time Units 1ns

Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		8.45690	**11.5599**	**22.4519**	**43.2519**	**75.6579**	**121.127**	**180.957**
A to PADM	TPLH	3.35600	4.12300	6.65600	11.3180	18.4840	28.4740	41.5730
A to PADM	TPHL	2.78400	3.32700	5.02300	8.00400	12.5280	18.8000	26.9990
EN to PADM three_state_disable	TLZ	0.352000						
EN to PADM three_state_disable	THZ	0.449000						
EN to PADM three_state_enable	TZH	3.61200	4.27100	6.57400	11.0230	17.8820	27.4600	40.0300
EN to PADM three_state_enable	TZL	3.04400	3.47900	4.96100	7.82700	12.1920	18.2480	26.1710

Delay Characteristics: Time Units 1ns

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.147070**	**0.649290**	**1.60830**	**3.10250**	**5.19900**	**7.95770**
PADM to QC	TPLH	1.18600	1.37400	2.13900	3.27300	4.75400	6.63000	8.94000
PADM to QC	TPHL	1.16800	1.39400	2.21400	3.37700	4.89300	6.81400	9.18000

Delay Characteristics: Time Units 1ns

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		7.92548	**11.0285**	**21.9205**	**42.7205**	**75.1265**	**120.595**	**180.425**
A to PADM	TPLH	6.80600	8.06900	12.3190	20.2200	32.4160	49.4450	71.7820
A to PADM	TPHL	5.78900	6.68100	9.46300	14.3090	21.6550	31.8710	45.2450
EN to PADM three_state_disable	TLZ	0.648000						
EN to PADM three_state_disable	THZ	0.866000						
EN to PADM three_state_enable	TZH	6.96800	8.20000	12.3070	19.9530	31.7860	48.3320	70.0600
EN to PADM three_state_enable	TZL	5.81800	6.71000	9.40500	14.1250	21.3150	31.3190	44.4200

Test Data

Parameter	Description	Minimum	Maximum	Units
Vih	High Level Input Voltage	(0.8*Vdd)	-	V
Vil	High Level Input Voltage	-	(0.2*Vdd)	V
Vhys	Schmitt Threshold	(0.21*Vdd)	Vdd	V
ipu	Pull up current	-161.0	-40.0	uA
ipd	Pull down current	32.0	192.0	uA
ibkpu	Buskeeper pull-up current	-110.0	-28.0	uA
vtestbkpu	Test voltage for keeping the bus keeper pin high	(0.7*Vdd)	-	V
ibkpd	Buskeeper pull-down current	21.0	139.0	uA
vtestbkpd	Test voltage for keeping the bus keeper pin lob	-	(0.3*Vdd)	V

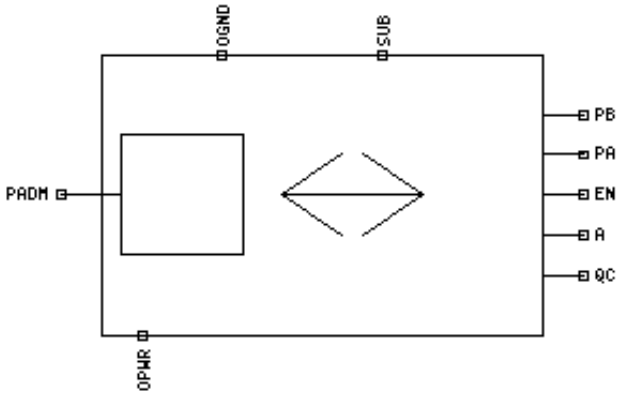
Iil	Low Level Input Current	-10.0	10.0	uA
Iih	High Level Input Current	-10.0	10.0	uA
Vdiode_vdd	Diode voltage range to Vdd	0.20	1.10	V
Vi_max	Maximum Voltage	-0.5	(1.10 * Vdd)	V
I_max	Maximum sink/source current	-100	100	mA
Vdiode_vss	Diode voltage to Vss	-1.10	-0.20	V
Voh	High Level Output Voltage	2.4	Vdd	V
Vol	Low Level Output Voltage	0.0	0.4	V
Iol	Low Level Output Current	2.0	-	mA
Ioh	High Level Output Current	-	-1.7	mA

ioacs6c3csxe04_mt

Description

"IOACS6C3CSXE04_MT is a[n] IOACS6C3CSXE04 is a non-inverting, CMOS-level, composite IO with a 4X drive, tri-state output buffer piece with active low enable and controlled slew rate output, a programmable pull-up/pull-down/bus-hold piece, and a Schmitt trigger input buffer piece with voltage hysteresis. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
PA	0.0382265 (pF)
A	0.0311864 (pF)
PB	0.0388941 (pF)
PADM	6.67952 (pF)
EN	0.0343174 (pF)

AREA : 27735.0 sqr microns

Truth Table

A input	EN input	PA input	PB input	PADM inout	QC output
L	L	?	?	L	L
L	H	?	?	Z	?
H	L	?	?	H	H
H	H	?	?	Z	?

IL = Illegal Z = High Impedence ? = Dont Care NC = No Change

Pull Cell Truth Table :

PA	PB	Function
0	0	Pull Down
0	1	Tristate

1	0	Bus Keeper
1	1	Pull Up

Power Characteristics:

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	607.444	uW

Power Characteristics:

Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	282.664	uW

Power Characteristics:

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	128.821	uW

Delay Characteristics: Time Units 1ns

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.147080**	**0.649310**	**1.60840**	**3.10260**	**5.19920**	**7.95800**
PADM to QC	TPLH	0.400000	0.542000	0.846000	1.23600	1.72500	2.32600	3.05300
PADM to QC	TPHL	0.378000	0.549000	0.902000	1.40200	2.07400	2.94700	4.04300

Delay Characteristics: Time Units 1ns

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		9.17952	**12.2825**	**23.1745**	**43.9745**	**76.3805**	**121.850**	**181.680**
A to PADM	TPLH	1.93300	2.29300	3.34500	5.13900	7.84000	11.5790	16.4620
A to PADM	TPHL	1.74700	2.09600	3.10600	4.75100	7.16200	10.4740	14.7890
EN to PADM three_state_disable	TLZ	0.277000						
EN to PADM three_state_disable	THZ	0.321000						
EN to PADM three_state_enable	TZH	2.34100	2.52500	3.22400	4.72400	7.02700	10.2150	14.3820
EN to PADM three_state_enable	TZL	2.30600	2.46900	3.10600	4.57200	6.82400	9.92000	13.9550

Delay Characteristics: Time Units 1ns

Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.147080**	**0.649310**	**1.60840**	**3.10260**	**5.19920**	**7.95800**
PADM to QC	TPLH	0.587000	0.769000	1.24300	1.87200	2.69300	3.72900	5.00400
PADM to QC	TPHL	0.574000	0.789000	1.30000	1.99600	2.91900	4.10200	5.57300

Delay Characteristics: Time Units 1ns

Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		8.35266	**11.4557**	**22.3477**	**43.1477**	**75.5537**	**121.023**	**180.853**
A to PADM	TPLH	3.18400	3.70500	5.23800	7.82100	11.6910	17.0520	24.0570
A to PADM	TPHL	2.89700	3.37100	4.75300	6.98400	10.2230	14.6630	20.4450
EN to PADM three_state_disable	TLZ	0.395000						
EN to PADM three_state_disable	THZ	0.514000						
EN to PADM three_state_enable	TZH	3.32700	3.77500	5.13600	7.49100	11.0270	15.9330	22.3530
EN to PADM three_state_enable	TZL	3.04700	3.44200	4.68400	6.82300	9.92300	14.1700	19.7060

Delay Characteristics: Time Units 1ns

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.147080**	**0.649310**	**1.60840**	**3.10260**	**5.19920**	**7.95800**
PADM to QC	TPLH	1.18600	1.37400	2.13900	3.27300	4.75400	6.63000	8.94000
PADM to QC	TPHL	1.16800	1.39400	2.21400	3.37700	4.89300	6.81400	9.18100

Delay Characteristics: Time Units 1ns

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		7.81766	**10.9207**	**21.8127**	**42.6127**	**75.0187**	**120.488**	**180.318**
A to PADM	TPLH	6.50500	7.38300	10.0060	14.3670	20.8350	29.7820	41.4770
A to PADM	TPHL	6.13700	6.93200	9.24800	12.9230	18.1760	25.3390	34.6680
EN to PADM three_state_disable	TLZ	0.714000						
EN to PADM three_state_disable	THZ	0.990000						
EN to PADM three_state_enable	TZH	6.66000	7.50300	9.97200	14.0520	20.1180	28.5260	39.5370
EN to PADM three_state_enable	TZL	6.14700	6.94800	9.18900	12.7560	17.8780	24.8610	33.9590

Test Data

Parameter	Description	Minimum	Maximum	Units
Vih	High Level Input Voltage	(0.8*Vdd)	-	V
Vil	High Level Input Voltage	-	(0.2*Vdd)	V
Vhys	Schmitt Threshold	(0.21*Vdd)	Vdd	V
ipu	Pull up current	-161.0	-40.0	uA
ipd	Pull down current	32.0	192.0	uA
ibkpu	Buskeeper pull-up current	-110.0	-28.0	uA
vtestbkpu	Test voltage for keeping the bus keeper pin high	(0.7*Vdd)	-	V
ibkpd	Buskeeper pull-down current	21.0	139.0	uA
vtestbkpd	Test voltage for keeping the bus keeper pin lob	-	(0.3*Vdd)	V

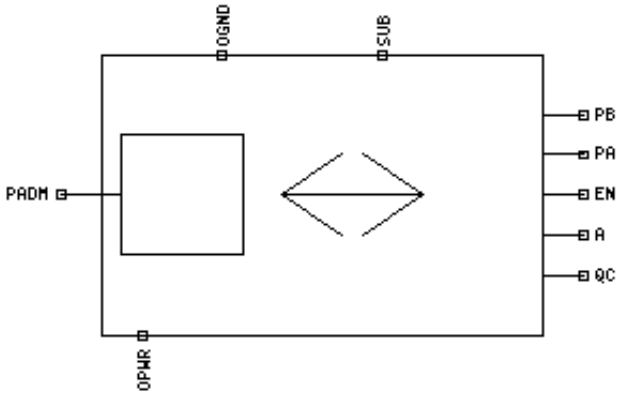
Iil	Low Level Input Current	-10.0	10.0	uA
Iih	High Level Input Current	-10.0	10.0	uA
Vdiode_vdd	Diode voltage range to Vdd	0.20	1.10	V
Vi_max	Maximum Voltage	-0.5	(1.10 * Vdd)	V
I_max	Maximum sink/source current	-100	100	mA
Vdiode_vss	Diode voltage to Vss	-1.10	-0.20	V
Voh	High Level Output Voltage	2.4	Vdd	V
Vol	Low Level Output Voltage	0.0	0.4	V
Iol	Low Level Output Current	3.12	-	mA
Ioh	High Level Output Current	-	-3.39	mA

ioacs6c3csxe08_mt

Description

"IOACS6C3CSXE08_MT is a[n] IOACS6C3CSXE08 is a non-inverting, CMOS-level, composite IO with a 8X drive, tri-state output buffer piece with active low enable and controlled slew rate output, a programmable pull-up/pull-down/bus-hold piece, and a Schmitt trigger input buffer piece with voltage hysteresis. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
PA	0.0382265 (pF)
A	0.0311864 (pF)
PB	0.0388941 (pF)
PADM	6.67968 (pF)
EN	0.0343174 (pF)

AREA : 27735.0 sqr microns

Truth Table

A input	EN input	PA input	PB input	PADM inout	QC output
L	L	?	?	L	L
L	H	?	?	Z	?
H	L	?	?	H	H
H	H	?	?	Z	?

IL = Illegal Z = High Impedence ? = Dont Care NC = No Change

Pull Cell Truth Table :

PA	PB	Function
0	0	Pull Down
0	1	Tristate

1	0	Bus Keeper
1	1	Pull Up

Power Characteristics:

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	607.448	uW

Power Characteristics:

Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	282.664	uW

Power Characteristics:

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	128.821	uW

Delay Characteristics: Time Units 1ns

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.147070**	**0.649290**	**1.60830**	**3.10250**	**5.19900**	**7.95770**
PADM to QC	TPLH	0.400000	0.542000	0.846000	1.23600	1.72500	2.32600	3.05300
PADM to QC	TPHL	0.378000	0.549000	0.902000	1.40200	2.07400	2.94700	4.04200

Delay Characteristics: Time Units 1ns

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		9.17968	**12.2827**	**23.1747**	**43.9747**	**76.3807**	**121.850**	**181.680**
A to PADM	TPLH	2.17700	2.51000	3.37500	4.62700	6.32100	8.57200	11.4770
A to PADM	TPHL	2.19200	2.52100	3.39600	4.62100	6.18100	8.13300	10.5580
EN to PADM three_state_disable	TLZ	0.375000						
EN to PADM three_state_disable	THZ	0.402000						
EN to PADM three_state_enable	TZH	2.41500	2.61500	3.22900	4.20700	5.49900	7.19100	9.36900
EN to PADM three_state_enable	TZL	2.43500	2.64100	3.32900	4.45300	5.87000	7.62500	9.79600

Delay Characteristics: Time Units 1ns

Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.147070**	**0.649290**	**1.60830**	**3.10250**	**5.19900**	**7.95770**
PADM to QC	TPLH	0.587000	0.769000	1.24300	1.87200	2.69300	3.72900	5.00400
PADM to QC	TPHL	0.574000	0.789000	1.30000	1.99600	2.91900	4.10200	5.57300

Delay Characteristics: Time Units 1ns

Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		8.35283	**11.4558**	**22.3478**	**43.1478**	**75.5538**	**121.023**	**180.853**
A to PADM	TPLH	3.54600	4.01000	5.24000	7.01500	9.37800	12.4760	16.4490
A to PADM	TPHL	3.74100	4.19800	5.42200	7.13100	9.27600	11.9230	15.1750
EN to PADM three_state_disable	TLZ	0.513000						
EN to PADM three_state_disable	THZ	0.643000						
EN to PADM three_state_enable	TZH	3.63500	4.04800	5.13400	6.67700	8.70000	11.3330	14.7080
EN to PADM three_state_enable	TZL	3.75700	4.18800	5.34900	6.98100	9.00400	11.4800	14.5090

Delay Characteristics: Time Units 1ns

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.147070**	**0.649290**	**1.60830**	**3.10250**	**5.19900**	**7.95770**
PADM to QC	TPLH	1.18600	1.37400	2.13900	3.27300	4.75400	6.63000	8.94000
PADM to QC	TPHL	1.16800	1.39400	2.21400	3.37700	4.89300	6.81400	9.18000

Delay Characteristics: Time Units 1ns

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		7.81781	**10.9208**	**21.8128**	**42.6128**	**75.0188**	**120.488**	**180.318**
A to PADM	TPLH	7.15600	7.93300	10.0640	13.1250	17.1070	22.2040	28.6500
A to PADM	TPHL	8.08700	8.89400	11.0490	14.0050	17.6210	21.9750	27.2180
EN to PADM three_state_disable	TLZ	0.916000						
EN to PADM three_state_disable	THZ	1.23100						
EN to PADM three_state_enable	TZH	7.30500	8.04800	10.0210	12.7980	16.3690	20.9140	26.6580
EN to PADM three_state_enable	TZL	8.07500	8.89100	10.9820	13.8460	17.3530	21.5570	26.6010

Test Data

Parameter	Description	Minimum	Maximum	Units
Vih	High Level Input Voltage	(0.8*Vdd)	-	V
Vil	High Level Input Voltage	-	(0.2*Vdd)	V
Vhys	Schmitt Threshold	(0.21*Vdd)	Vdd	V
ipu	Pull up current	-161.0	-40.0	uA
ipd	Pull down current	32.0	192.0	uA
ibkpu	Buskeeper pull-up current	-110.0	-28.0	uA
vtestbkpu	Test voltage for keeping the bus keeper pin high	(0.7*Vdd)	-	V
ibkpd	Buskeeper pull-down current	21.0	139.0	uA
vtestbkpd	Test voltage for keeping the bus keeper pin lob	-	(0.3*Vdd)	V

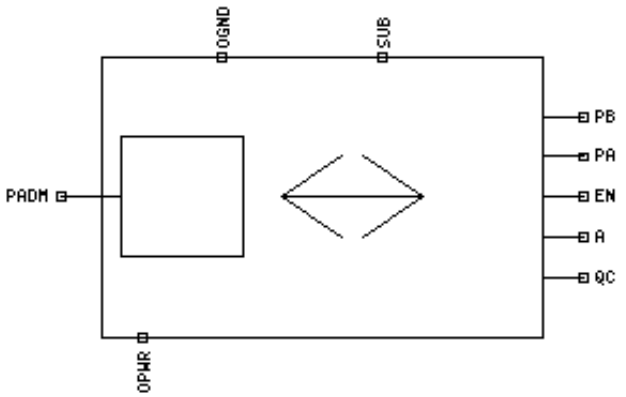
Iil	Low Level Input Current	-10.0	10.0	uA
Iih	High Level Input Current	-10.0	10.0	uA
Vdiode_vdd	Diode voltage range to Vdd	0.20	1.10	V
Vi_max	Maximum Voltage	-0.5	(1.10 * Vdd)	V
I_max	Maximum sink/source current	-100	100	mA
Vdiode_vss	Diode voltage to Vss	-1.10	-0.20	V
Voh	High Level Output Voltage	2.4	Vdd	V
Vol	Low Level Output Voltage	0.0	0.4	V
Iol	Low Level Output Current	6.25	-	mA
Ioh	High Level Output Current	-	-6.79	mA

ioacs6c3cxxe02_mt

Description

"IOACS6C3CXXE02_MT is a[n] IOACS6C3CXXE02 is a non-inverting, CMOS-level composite IO with a 2X drive, tri-state output buffer piece with active low enable, a programmable pull-up/pull-down/bus-hold piece, and a Schmitt trigger input buffer piece with voltage hysteresis. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
PA	0.0382265 (pF)
A	0.0311861 (pF)
PB	0.0388944 (pF)
PADM	6.78038 (pF)
EN	0.0343174 (pF)

AREA : 27735.0 sqr microns

Truth Table

A input	EN input	PA input	PB input	PADM inout	QC output
L	L	?	?	L	L
L	H	?	?	Z	?
H	L	?	?	H	H
H	H	?	?	Z	?

IL = Illegal Z = High Impedence ? = Dont Care NC = No Change

Pull Cell Truth Table :

PA	PB	Function
0	0	Pull Down
0	1	Tristate
1	0	Bus Keeper

1	1	Pull Up

Power Characteristics:
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	607.437	uW

Power Characteristics:
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	282.664	uW

Power Characteristics:
Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	128.821	uW

Delay Characteristics: Time Units 1ns
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.147070**	**0.649290**	**1.60830**	**3.10250**	**5.19900**	**7.95770**
PADM to QC	TPLH	0.400000	0.542000	0.846000	1.23600	1.72500	2.32600	3.05300
PADM to QC	TPHL	0.378000	0.549000	0.902000	1.40200	2.07400	2.94700	4.04200

Delay Characteristics: Time Units 1ns
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		9.28038	**12.3833**	**23.2754**	**44.0754**	**76.4814**	**121.950**	**181.780**
A to PADM	TPLH	1.12400	1.64500	3.38000	6.55000	11.4000	18.1510	26.9940
A to PADM	TPHL	0.850000	1.20900	2.42100	4.62600	7.98300	12.6380	18.7210
EN to PADM three_state_disable	TLZ	0.281000						
EN to PADM three_state_disable	THZ	0.293000						
EN to PADM three_state_enable	TZH	2.64500	2.95000	3.97100	6.15200	10.6260	16.8610	25.0360
EN to PADM three_state_enable	TZL	2.34400	2.51200	3.07800	4.43800	7.62000	12.0310	17.7960

Delay Characteristics: Time Units 1ns
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.147070**	**0.649290**	**1.60830**	**3.10250**	**5.19900**	**7.95770**
PADM to QC	TPLH	0.587000	0.769000	1.24300	1.87200	2.69300	3.72900	5.00400
PADM to QC	TPHL	0.574000	0.789000	1.30000	1.99600	2.91900	4.10200	5.57300

Delay Characteristics: Time Units 1ns
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		8.45690	11.5598	22.4519	43.2519	75.6579	121.127	180.957
A to PADM	TPLH	1.83800	2.59500	5.12500	9.78900	16.9560	26.9500	40.0520
A to PADM	TPHL	1.28400	1.75100	3.35700	6.31300	10.8280	17.0930	25.2880
EN to PADM three_state_disable	TLZ	0.398000						
EN to PADM three_state_disable	THZ	0.471000						
EN to PADM three_state_enable	TZH	3.20900	3.74700	5.54800	9.48000	16.3400	25.9180	38.4900
EN to PADM three_state_enable	TZL	2.58800	2.87000	3.81800	6.14000	10.5000	16.5530	24.4700

Delay Characteristics: Time Units 1ns

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	0.147070	0.649290	1.60830	3.10250	5.19900	7.95770
PADM to QC	TPLH	1.18600	1.37400	2.13900	3.27300	4.75400	6.63000	8.94000
PADM to QC	TPHL	1.16800	1.39400	2.21400	3.37700	4.89300	6.81400	9.18000

Delay Characteristics: Time Units 1ns

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		7.92551	11.0284	21.9205	42.7205	75.1265	120.596	180.426
A to PADM	TPLH	3.56100	4.76400	8.96600	16.8620	29.0620	46.0950	68.4370
A to PADM	TPHL	2.49000	3.20900	5.74400	10.4990	17.8240	28.0270	41.3880
EN to PADM three_state_disable	TLZ	0.737000						
EN to PADM three_state_disable	THZ	0.907000						
EN to PADM three_state_enable	TZH	4.51000	5.49300	8.96000	16.5740	28.4040	44.9490	66.6770
EN to PADM three_state_enable	TZL	3.28600	3.82700	5.76500	10.3100	17.4830	27.4810	40.5780

Test Data

Parameter	Description	Minimum	Maximum	Units
Vih	High Level Input Voltage	(0.8*Vdd)	-	V
Vil	High Level Input Voltage	-	(0.2*Vdd)	V
Vhys	Schmitt Threshold	(0.21*Vdd)	Vdd	V
ipu	Pull up current	-161.0	-40.0	uA
ipd	Pull down current	32.0	192.0	uA
ibkpu	Buskeeper pull-up current	-110.0	-28.0	uA
vtestbkpu	Test voltage for keeping the bus keeper pin high	(0.7*Vdd)	-	V
ibkpd	Buskeeper pull-down current	21.0	139.0	uA
vtestbkpd	Test voltage for keeping the bus keeper pin lob	-	(0.3*Vdd)	V
Iil	Low Level Input Current	-10.0	10.0	uA

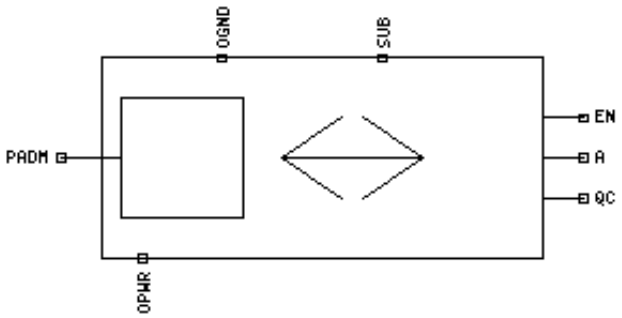
Iih	High Level Input Current	-10.0	10.0	uA
Vdiode_vdd	Diode voltage range to Vdd	0.20	1.10	V
Vi_max	Maximum Voltage	-0.5	(1.10 * Vdd)	V
I_max	Maximum sink/source current	-100	100	mA
Vdiode_vss	Diode voltage to Vss	-1.10	-0.20	V
Voh	High Level Output Voltage	2.4	Vdd	V
Vol	Low Level Output Voltage	0.0	0.4	V
Iol	Low Level Output Current	2.0	-	mA
Ioh	High Level Output Current	-	-1.7	mA

ioacs6xxcsxe02_mt

Description

"IOACS6XXCSXE02_MT is a[n] IOACS6XXCSXE02 is a non-inverting, CMOS-level composite IO with a 2X drive, tri-state output buffer piece with active low enable, controlled slew rate output, and a Schmitt trigger input buffer piece with voltage hysteresis. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
A	0.0310205 (pF)
PADM	4.73909 (pF)
EN	0.0343174 (pF)

AREA : 27735.0 sqr microns

Truth Table

A input	EN input	PADM inout	QC output
L	L	L	L
L	H	Z	?
H	L	H	H
H	H	Z	?

IL = Illegal Z = High Impedence ? = Dont Care NC = No Change

Power Characteristics:

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	0.000101787	uW

Power Characteristics:
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	0.000212006	uW

Power Characteristics:
Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	0.089468	uW

Delay Characteristics: Time Units 1ns
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.146840**	**0.648220**	**1.60570**	**3.09740**	**5.19040**	**7.94450**
PADM to QC	TPLH	0.401000	0.542000	0.846000	1.23600	1.72400	2.32600	3.05200
PADM to QC	TPHL	0.379000	0.550000	0.903000	1.40100	2.07400	2.94600	4.03900

Delay Characteristics: Time Units 1ns
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		7.23909	**10.3420**	**21.2341**	**42.0341**	**74.4401**	**119.909**	**179.739**
A to PADM	TPLH	1.99000	2.51600	4.24700	7.41400	12.2640	19.0140	27.8630
A to PADM	TPHL	1.69500	2.09800	3.35400	5.57300	8.93400	13.5940	19.6840
EN to PADM three_state_disable	TLZ	0.249000						
EN to PADM three_state_disable	THZ	0.278000						
EN to PADM three_state_enable	TZH	2.65500	2.97700	4.17900	6.98500	11.4250	17.6150	25.7290
EN to PADM three_state_enable	TZL	2.41300	2.62600	3.43400	5.42200	8.64800	13.1230	18.9700

Delay Characteristics: Time Units 1ns
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.146840**	**0.648220**	**1.60570**	**3.09740**	**5.19040**	**7.94450**
PADM to QC	TPLH	0.588000	0.770000	1.24300	1.87200	2.69200	3.72800	5.00100
PADM to QC	TPHL	0.575000	0.790000	1.30000	1.99600	2.91800	4.09900	5.56900

Delay Characteristics: Time Units 1ns
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		7.25821	**10.3611**	**21.2532**	**42.0532**	**74.4592**	**119.928**	**179.758**
A to PADM	TPLH	3.32300	4.09100	6.62100	11.2820	18.4480	28.4370	41.5370
A to PADM	TPHL	2.76400	3.30700	5.00400	7.98600	12.5090	18.7820	26.9790
	TLZ	0.352000						

EN to PADM three_state_disable								
EN to PADM three_state_disable	THZ	0.449000						
EN to PADM three_state_enable	TZH	3.56700	4.22200	6.51000	10.9340	17.7510	27.2730	39.7670
EN to PADM three_state_enable	TZL	3.03500	3.47300	4.96800	7.85900	12.2600	18.3710	26.3620

Delay Characteristics: Time Units 1ns

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	0.146840	0.648220	1.60570	3.09740	5.19040	7.94450
PADM to QC	TPLH	1.18700	1.37500	2.13900	3.27200	4.75300	6.62700	8.93500
PADM to QC	TPHL	1.16900	1.39500	2.21400	3.37600	4.89000	6.80900	9.17200

Delay Characteristics: Time Units 1ns

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		7.29966	10.4026	21.2947	42.0947	74.5007	119.970	179.800
A to PADM	TPLH	6.73600	8.00300	12.2530	20.1540	32.3510	49.3790	71.7170
A to PADM	TPHL	5.74600	6.64100	9.42800	14.2760	21.6210	31.8380	45.2110
EN to PADM three_state_disable	TLZ	0.648000						
EN to PADM three_state_disable	THZ	0.866000						
EN to PADM three_state_enable	TZH	6.87900	8.10800	12.2000	19.8130	31.5910	48.0610	69.6860
EN to PADM three_state_enable	TZL	5.80300	6.70100	9.41400	14.1640	21.3960	31.4620	44.6420

Test Data

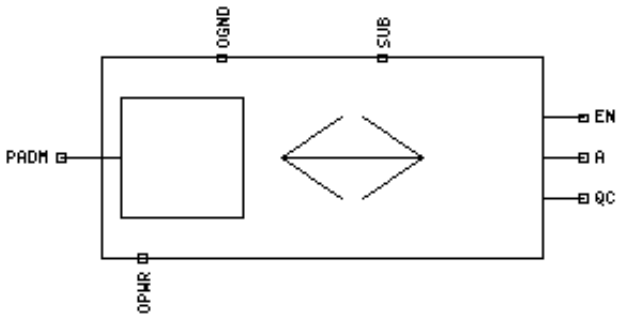
Parameter	Description	Minimum	Maximum	Units
Vih	High Level Input Voltage	(0.8*Vdd)	-	V
Vil	High Level Input Voltage	-	(0.2*Vdd)	V
Vhys	Schmitt Threshold	(0.21*Vdd)	Vdd	V
Iil	Low Level Input Current	-10.0	10.0	uA
Iih	High Level Input Current	-10.0	10.0	uA
Vdiode_vdd	Diode voltage range to Vdd	0.20	1.10	V
Vi_max	Maximum Voltage	-0.5	(1.10 * Vdd)	V
I_max	Maximum sink/source current	-100	100	mA
Vdiode_vss	Diode voltage to Vss	-1.10	-0.20	V
Voh	High Level Output Voltage	2.4	Vdd	V
Vol	Low Level Output Voltage	0.0	0.4	V
Iol	Low Level Output Current	2.0	-	mA
Ioh	High Level Output Current	-	-1.7	mA

ioacs6xxcsxe04_mt

Description

"IOACS6XXCSXE04_MT is a[n] IOACS6XXCSXE04 is a non-inverting, CMOS-level composite IO with a 4X drive, tri-state output buffer piece with active low enable, controlled slew rate output, and a Schmitt trigger input buffer piece with voltage hysteresis. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
A	0.0310208 (pF)
PADM	4.63826 (pF)
EN	0.0343174 (pF)

AREA : 27735.0 sqr microns

Truth Table

A input	EN input	PADM inout	QC output
L	L	L	L
L	H	Z	?
H	L	H	H
H	H	Z	?

IL = Illegal Z = High Impedence ? = Dont Care NC = No Change

Power Characteristics:

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	0.000101602	uW

Power Characteristics:
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	0.000206843	uW

Power Characteristics:
Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	0.0889358	uW

Delay Characteristics: Time Units 1ns
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.146840**	**0.648220**	**1.60570**	**3.09740**	**5.19040**	**7.94450**
PADM to QC	TPLH	0.401000	0.542000	0.846000	1.23600	1.72400	2.32600	3.05200
PADM to QC	TPHL	0.379000	0.550000	0.903000	1.40100	2.07400	2.94600	4.03900

Delay Characteristics: Time Units 1ns
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		7.13826	**10.2412**	**21.1333**	**41.9333**	**74.3393**	**119.808**	**179.638**
A to PADM	TPLH	1.91900	2.28100	3.33300	5.12700	7.82900	11.5670	16.4510
A to PADM	TPHL	1.73400	2.08400	3.09600	4.74200	7.15200	10.4630	14.7790
EN to PADM three_state_disable	TLZ	0.277000						
EN to PADM three_state_disable	THZ	0.321000						
EN to PADM three_state_enable	TZH	2.32700	2.50900	3.20600	4.70200	6.99600	10.1730	14.3250
EN to PADM three_state_enable	TZL	2.30000	2.46400	3.10800	4.58900	6.86200	9.98800	14.0620

Delay Characteristics: Time Units 1ns
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.146840**	**0.648220**	**1.60570**	**3.09740**	**5.19040**	**7.94450**
PADM to QC	TPLH	0.588000	0.770000	1.24300	1.87200	2.69200	3.72800	5.00100
PADM to QC	TPHL	0.575000	0.790000	1.30000	1.99600	2.91800	4.09900	5.56900

Delay Characteristics: Time Units 1ns
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		7.15397	**10.2569**	**21.1490**	**41.9490**	**74.3550**	**119.824**	**179.654**
A to PADM	TPLH	3.16200	3.68700	5.22000	7.80300	11.6740	17.0330	24.0390
A to PADM	TPHL	2.87900	3.35500	4.74000	6.97100	10.2100	14.6490	20.4310
	TLZ	0.395000						

EN to PADM three_state_disable								
EN to PADM three_state_disable	THZ	0.514000						
EN to PADM three_state_enable	TZH	3.30100	3.74900	5.11000	7.45900	10.9840	15.8760	22.2770
EN to PADM three_state_enable	TZL	3.04000	3.43800	4.68800	6.84100	9.96000	14.2350	19.8080

Delay Characteristics: Time Units 1ns

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	0.146840	0.648220	1.60570	3.09740	5.19040	7.94450
PADM to QC	TPLH	1.18700	1.37500	2.13900	3.27200	4.75300	6.62700	8.93500
PADM to QC	TPHL	1.16900	1.39500	2.21400	3.37600	4.89000	6.80900	9.17200

Delay Characteristics: Time Units 1ns

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		7.19181	10.2947	21.1868	41.9868	74.3928	119.862	179.692
A to PADM	TPLH	6.45700	7.34000	9.97000	14.3320	20.8020	29.7480	41.4440
A to PADM	TPHL	6.09800	6.89800	9.22100	12.9000	18.1530	25.3150	34.6440
EN to PADM three_state_disable	TLZ	0.714000						
EN to PADM three_state_disable	THZ	0.990000						
EN to PADM three_state_enable	TZH	6.60100	7.44900	9.92100	13.9980	20.0500	28.4390	39.4250
EN to PADM three_state_enable	TZL	6.13400	6.94200	9.19600	12.7790	17.9220	24.9360	34.0750

Test Data

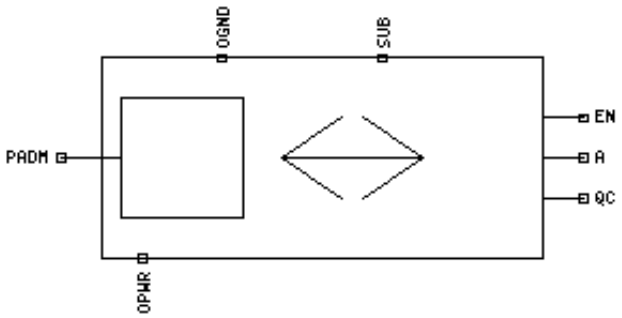
Parameter	Description	Minimum	Maximum	Units
Vih	High Level Input Voltage	(0.8*Vdd)	-	V
Vil	High Level Input Voltage	-	(0.2*Vdd)	V
Vhys	Schmitt Threshold	(0.21*Vdd)	Vdd	V
Iil	Low Level Input Current	-10.0	10.0	uA
Iih	High Level Input Current	-10.0	10.0	uA
Vdiode_vdd	Diode voltage range to Vdd	0.20	1.10	V
Vi_max	Maximum Voltage	-0.5	(1.10 * Vdd)	V
I_max	Maximum sink/source current	-100	100	mA
Vdiode_vss	Diode voltage to Vss	-1.10	-0.20	V
Voh	High Level Output Voltage	2.4	Vdd	V
Vol	Low Level Output Voltage	0.0	0.4	V
Iol	Low Level Output Current	3.12	-	mA
Ioh	High Level Output Current	-	-3.39	mA

ioacs6xxcsxe08_mt

Description

"IOACS6XXCSXE08_MT is a[n] IOACS6XXCSXE08 is a non-inverting, CMOS-level composite IO with a 8X drive, tri-state output buffer piece with active low enable, controlled slew rate output, and a Schmitt trigger input buffer piece with voltage hysteresis. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
A	0.0310205 (pF)
PADM	4.63841 (pF)
EN	0.0343174 (pF)

AREA : 27735.0 sqr microns

Truth Table

A input	EN input	PADM inout	QC output
L	L	L	L
L	H	Z	?
H	L	H	H
H	H	Z	?

IL = Illegal Z = High Impedence ? = Dont Care NC = No Change

Power Characteristics:

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	0.00010159	uW

Power Characteristics:
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	0.000206835	uW

Power Characteristics:
Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	0.0889358	uW

Delay Characteristics: Time Units 1ns
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.146840**	**0.648220**	**1.60570**	**3.09740**	**5.19040**	**7.94450**
PADM to QC	TPLH	0.401000	0.542000	0.846000	1.23600	1.72400	2.32600	3.05200
PADM to QC	TPHL	0.379000	0.550000	0.903000	1.40100	2.07400	2.94600	4.03900

Delay Characteristics: Time Units 1ns
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		7.13841	**10.2414**	**21.1334**	**41.9334**	**74.3394**	**119.808**	**179.638**
A to PADM	TPLH	2.16400	2.50000	3.36700	4.62000	6.31600	8.56600	11.4710
A to PADM	TPHL	2.17900	2.51100	3.38800	4.61600	6.17600	8.12800	10.5520
EN to PADM three_state_disable	TLZ	0.375000						
EN to PADM three_state_disable	THZ	0.402000						
EN to PADM three_state_enable	TZH	2.40200	2.60100	3.21700	4.19800	5.48700	7.17700	9.35200
EN to PADM three_state_enable	TZL	2.43000	2.63800	3.33200	4.46400	5.88800	7.65400	9.83800

Delay Characteristics: Time Units 1ns
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.146840**	**0.648220**	**1.60570**	**3.09740**	**5.19040**	**7.94450**
PADM to QC	TPLH	0.588000	0.770000	1.24300	1.87200	2.69200	3.72800	5.00100
PADM to QC	TPHL	0.575000	0.790000	1.30000	1.99600	2.91800	4.09900	5.56900

Delay Characteristics: Time Units 1ns
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		7.15414	**10.2571**	**21.1491**	**41.9491**	**74.3551**	**119.824**	**179.654**
A to PADM	TPLH	3.52600	3.99500	5.22800	7.00400	9.36900	12.4660	16.4400
A to PADM	TPHL	3.72300	4.18300	5.41100	7.12300	9.26900	11.9160	15.1680
	TLZ	0.513000						

EN to PADM three_state_disable								
EN to PADM three_state_disable	THZ	0.643000						
EN to PADM three_state_enable	TZH	3.61000	4.02600	5.11700	6.66200	8.68300	11.3130	14.6830
EN to PADM three_state_enable	TZL	3.75300	4.18700	5.35500	6.99400	9.02300	11.5080	14.5490

Delay Characteristics: Time Units 1ns

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	0.146840	0.648220	1.60570	3.09740	5.19040	7.94450
PADM to QC	TPLH	1.18700	1.37500	2.13900	3.27200	4.75300	6.62700	8.93500
PADM to QC	TPHL	1.16900	1.39500	2.21400	3.37600	4.89000	6.80900	9.17200

Delay Characteristics: Time Units 1ns

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		7.19196	10.2950	21.1870	41.9870	74.3930	119.862	179.692
A to PADM	TPLH	7.11300	7.89800	10.0380	13.1040	17.0890	22.1860	28.6330
A to PADM	TPHL	8.04600	8.86000	11.0260	13.9880	17.6060	21.9620	27.2050
EN to PADM three_state_disable	TLZ	0.916000						
EN to PADM three_state_disable	THZ	1.23100						
EN to PADM three_state_enable	TZH	7.25200	8.00200	9.98500	12.7680	16.3380	20.8800	26.6180
EN to PADM three_state_enable	TZL	8.07100	8.89100	10.9920	13.8650	17.3790	21.5920	26.6490

Test Data

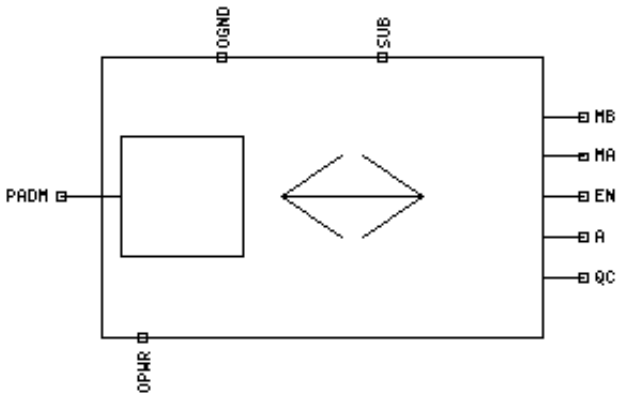
Parameter	Description	Minimum	Maximum	Units
Vih	High Level Input Voltage	(0.8*Vdd)	-	V
Vil	High Level Input Voltage	-	(0.2*Vdd)	V
Vhys	Schmitt Threshold	(0.21*Vdd)	Vdd	V
Iil	Low Level Input Current	-10.0	10.0	uA
Iih	High Level Input Current	-10.0	10.0	uA
Vdiode_vdd	Diode voltage range to Vdd	0.20	1.10	V
Vi_max	Maximum Voltage	-0.5	(1.10 * Vdd)	V
I_max	Maximum sink/source current	-100	100	mA
Vdiode_vss	Diode voltage to Vss	-1.10	-0.20	V
Voh	High Level Output Voltage	2.4	Vdd	V
Vol	Low Level Output Voltage	0.0	0.4	V
Iol	Low Level Output Current	6.25	-	mA
Ioh	High Level Output Current	-	-6.79	mA

ioacstptcxte02_mt

Description

"IOACSTPTCXTE02_MT is a[n] IOACSTPTCXTE02 is a non-inverting, 5v tolerant, CMOS-level Schmitt trigger composite IO with a 2X drive, tri-state output buffer piece with a active low enable and controlled slew rate output, a programmable pull-up/pull-down piece, and input buffer piece. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
A	0.0316489 (pF)
MA	0.0299008 (pF)
PADM	7.32752 (pF)
MB	0.0409256 (pF)
EN	0.0620083 (pF)

AREA : 27735.0 sqr microns

Truth Table

A input	EN input	MA input	MB input	PADM inout	QC output
L	L	?	?	L	L
L	H	?	?	Z	?
H	L	?	?	H	H
H	H	?	?	Z	?

IL = Illegal Z = High Impedence ? = Dont Care NC = No Change

Pull Cell Truth Table :

MA	MB	Function
0	0	Pull Down
0	1	Tristate
1	0	Tristate

1	1	Pull Up

Power Characteristics:
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	601.898	uW

Power Characteristics:
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	270.507	uW

Power Characteristics:
Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	116.107	uW

Delay Characteristics: Time Units 1ns
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.143910**	**0.635030**	**1.57290**	**3.03400**	**5.08420**	**7.78200**
PADM to QC	TPLH	0.695000	0.745000	1.02400	1.50700	2.16400	3.01200	4.06700
PADM to QC	TPHL	0.581000	0.718000	1.19700	1.98900	3.11200	4.60100	6.49600

Delay Characteristics: Time Units 1ns
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		9.82752	**12.9305**	**23.8225**	**44.6225**	**77.0285**	**122.498**	**182.328**
A to PADM	TPLH	1.31500	1.84700	3.60000	6.79400	11.6730	18.4620	27.3580
A to PADM	TPHL	0.904000	1.27400	2.51900	4.77900	8.21500	12.9780	19.2060
EN to PADM three_state_disable	TLZ	0.333000						
EN to PADM three_state_disable	THZ	0.426000						
EN to PADM three_state_enable	TZH	2.78400	3.09800	4.13600	6.54400	11.0920	17.4100	25.6810
EN to PADM three_state_enable	TZL	2.39300	2.57300	3.17400	4.57900	7.82100	12.3120	18.1800

Delay Characteristics: Time Units 1ns
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.143910**	**0.635030**	**1.57290**	**3.03400**	**5.08420**	**7.78200**
PADM to QC	TPLH	1.32600	1.30600	1.52800	2.03200	2.73000	3.60900	4.68000
PADM to QC	TPHL	0.940000	1.06500	1.55800	2.36200	3.49900	4.99000	6.86700

Delay Characteristics: Time Units 1ns
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		8.97774	**12.0807**	**22.9727**	**43.7727**	**76.1787**	**121.648**	**181.478**
A to PADM	TPLH	2.13900	2.90700	5.46600	10.1720	17.3910	27.4480	40.6330
A to PADM	TPHL	1.40400	1.91900	3.67700	6.91400	11.8640	18.7400	27.7370
EN to PADM three_state_disable	TLZ	0.471000						
EN to PADM three_state_disable	THZ	0.686000						
EN to PADM three_state_enable	TZH	3.41900	3.96600	5.79200	10.0540	17.0200	26.7180	39.4240
EN to PADM three_state_enable	TZL	2.70600	3.03500	4.13700	6.72800	11.5140	18.1560	26.8470

Delay Characteristics: Time Units 1ns

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.143910**	**0.635030**	**1.57290**	**3.03400**	**5.08420**	**7.78200**
PADM to QC	TPLH	3.40100	3.27500	3.35800	3.90100	4.89200	6.24700	7.92300
PADM to QC	TPHL	1.95000	2.10600	2.72100	3.76700	5.18900	7.03900	9.34900

Delay Characteristics: Time Units 1ns

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		8.45713	**11.5601**	**22.4521**	**43.2521**	**75.6581**	**121.127**	**180.957**
A to PADM	TPLH	4.14000	5.37600	9.65700	17.6400	29.9280	47.0610	69.5280
A to PADM	TPHL	2.86600	3.75200	6.87000	12.7190	21.7280	34.2870	50.7440
EN to PADM three_state_disable	TLZ	0.878000						
EN to PADM three_state_disable	THZ	1.36600						
EN to PADM three_state_enable	TZH	4.88100	5.90900	9.88000	17.6760	29.6710	46.3990	68.3330
EN to PADM three_state_enable	TZL	3.65800	4.36700	6.86900	12.4960	21.3400	33.6710	49.8300

Test Data

Parameter	Description	Minimum	Maximum	Units
Vih	High Level Input Voltage	(0.8*Vdd)	-	V
Vil	High Level Input Voltage	-	(0.2*Vdd)	V
Vhys	Schmitt Threshold	(0.189*Vdd)	Vdd	V
ipu	Pull up current	-155.0	-36.0	uA
ipd	Pull down current	28.0	191.0	uA
Iil	Low Level Input Current	-10.0	10.0	uA
Iih	High Level Input Current	-10.0	10.0	uA
Vi_max	Maximum Voltage	-0.5	5.0	V
I_max	Maximum sink/source current	-100	100	mA
Vdiode_vss	Diode voltage to Vss	-1.10	-0.20	V

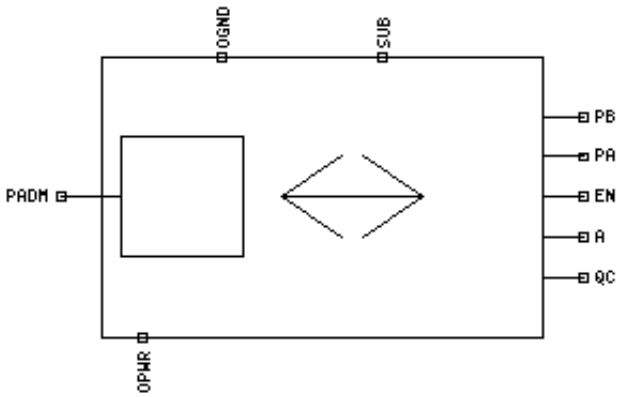
Voh	High Level Output Voltage	2.4	Vdd	V
Vol	Low Level Output Voltage	0.0	0.4	V
Iol	Low Level Output Current	1.62	-	mA
Ioh	High Level Output Current	-	-1.69	mA

ioacx6c3csxe02_mt

Description

"IOACX6C3CSXE02_MT is a[n] IOACX6C3CSXE02 is a non-inverting, CMOS-level composite IO with at 2X drive, tri-state output buffer piece with a active low enable and controlled slew rate output, a programmable pull-up/pull-down/bus-hold piece, and input buffer piece. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
PA	0.0382265 (pF)
A	0.0311864 (pF)
PB	0.0388944 (pF)
PADM	6.77049 (pF)
EN	0.0343174 (pF)

AREA : 27735.0 sqr microns

Truth Table

A input	EN input	PA input	PB input	PADM inout	QC output
L	L	?	?	L	L
L	H	?	?	Z	?
H	L	?	?	H	H
H	H	?	?	Z	?

IL = Illegal Z = High Impedence ? = Dont Care NC = No Change

Pull Cell Truth Table :

PA	PB	Function
0	0	Pull Down
0	1	Tristate
1	0	Bus Keeper

1	1	Pull Up

Power Characteristics:
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	607.437	uW

Power Characteristics:
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	282.664	uW

Power Characteristics:
Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	128.821	uW

Delay Characteristics: Time Units 1ns
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.143910**	**0.635010**	**1.57290**	**3.03400**	**5.08410**	**7.78170**
PADM to QC	TPLH	0.268000	0.398000	0.643000	0.998000	1.48000	2.11100	2.90700
PADM to QC	TPHL	0.282000	0.420000	0.687000	1.06700	1.58300	2.25300	3.09500

Delay Characteristics: Time Units 1ns
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		9.27049	**12.3735**	**23.2655**	**44.0655**	**76.4715**	**121.940**	**181.770**
A to PADM	TPLH	2.01200	2.53700	4.26900	7.43800	12.2860	19.0380	27.8850
A to PADM	TPHL	1.70900	2.11200	3.36800	5.58600	8.94800	13.6080	19.6990
EN to PADM three_state_disable	TLZ	0.249000						
EN to PADM three_state_disable	THZ	0.278000						
EN to PADM three_state_enable	TZH	2.68300	3.00900	4.22300	7.04800	11.5220	17.7550	25.9290
EN to PADM three_state_enable	TZL	2.41900	2.63100	3.42700	5.39000	8.57700	12.9960	18.7710

Delay Characteristics: Time Units 1ns
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.143910**	**0.635010**	**1.57290**	**3.03400**	**5.08410**	**7.78170**
PADM to QC	TPLH	0.378000	0.531000	0.829000	1.22200	1.73800	2.39500	3.20700
PADM to QC	TPHL	0.415000	0.610000	1.03800	1.67400	2.56100	3.73000	5.21000

Delay Characteristics: Time Units 1ns
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		8.44680	**11.5498**	**22.4418**	**43.2418**	**75.6478**	**121.117**	**180.947**
A to PADM	TPLH	3.35500	4.12200	6.65500	11.3170	18.4820	28.4730	41.5720
A to PADM	TPHL	2.78300	3.32600	5.02200	8.00300	12.5280	18.8000	26.9980
EN to PADM three_state_disable	TLZ	0.352000						
EN to PADM three_state_disable	THZ	0.449000						
EN to PADM three_state_enable	TZH	3.61000	4.27000	6.57300	11.0210	17.8810	27.4590	40.0290
EN to PADM three_state_enable	TZL	3.04300	3.47800	4.96000	7.82700	12.1910	18.2480	26.1710

Delay Characteristics: Time Units 1ns

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.143910**	**0.635010**	**1.57290**	**3.03400**	**5.08410**	**7.78170**
PADM to QC	TPLH	0.719000	0.947000	1.45200	2.19100	3.19300	4.48800	6.10300
PADM to QC	TPHL	0.795000	1.07600	1.71500	2.69300	4.06200	5.86800	8.15300

Delay Characteristics: Time Units 1ns

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		7.91519	**11.0182**	**21.9102**	**42.7102**	**75.1162**	**120.585**	**180.415**
A to PADM	TPLH	6.80300	8.06600	12.3170	20.2170	32.4140	49.4430	71.7800
A to PADM	TPHL	5.78800	6.67900	9.46100	14.3080	21.6530	31.8700	45.2430
EN to PADM three_state_disable	TLZ	0.648000						
EN to PADM three_state_disable	THZ	0.866000						
EN to PADM three_state_enable	TZH	6.96500	8.19700	12.3040	19.9500	31.7830	48.3290	70.0570
EN to PADM three_state_enable	TZL	5.81600	6.70800	9.40400	14.1240	21.3130	31.3180	44.4180

Test Data

Parameter	Description	Minimum	Maximum	Units
Vih	High Level Input Voltage	(0.7*Vdd)	-	V
Vil	High Level Input Voltage	-	(0.3*Vdd)	V
ipu	Pull up current	-161.0	-40.0	uA
ipd	Pull down current	32.0	192.0	uA
ibkpu	Buskeeper pull-up current	-110.0	-28.0	uA
vtestbkpu	Test voltage for keeping the bus keeper pin high	(0.7*Vdd)	-	V
ibkpd	Buskeeper pull-down current	21.0	139.0	uA
vtestbkpd	Test voltage for keeping the bus keeper pin lob	-	(0.3*Vdd)	V
Iil	Low Level Input Current	-10.0	10.0	uA
Iih	High Level Input Current	-10.0	10.0	uA

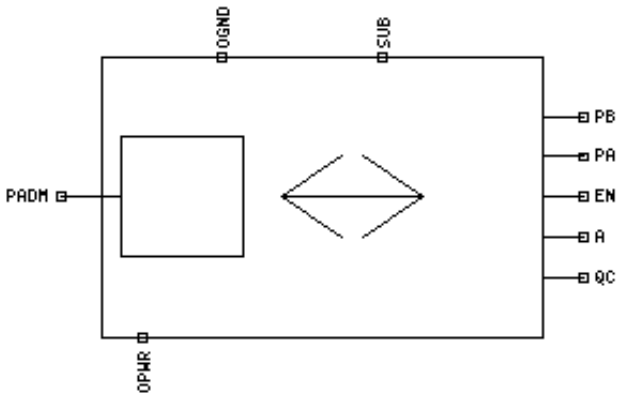
Vdiode_vdd	Diode voltage range to Vdd	0.20	1.10	V
Vi_max	Maximum Voltage	-0.5	(1.10 * Vdd)	V
I_max	Maximum sink/source current	-100	100	mA
Vdiode_vss	Diode voltage to Vss	-1.10	-0.20	V
Voh	High Level Output Voltage	2.4	Vdd	V
Vol	Low Level Output Voltage	0.0	0.4	V
Iol	Low Level Output Current	2.0	-	mA
Ioh	High Level Output Current	-	-1.7	mA

ioacx6c3csxe04_mt

Description

"IOACX6C3CSXE04_MT is a[n] IOACX6C3CSXE04 is a non-inverting, CMOS-level composite IO with a 4X drive, tri-state output buffer piece with a active low enable and controlled slew rate output, a programmable pull-up/pull-down/bus-hold piece, and input buffer piece. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
PA	0.0382265 (pF)
A	0.0311864 (pF)
PB	0.0388941 (pF)
PADM	6.66967 (pF)
EN	0.0343174 (pF)

AREA : 27735.0 sqr microns

Truth Table

A input	EN input	PA input	PB input	PADM inout	QC output
L	L	?	?	L	L
L	H	?	?	Z	?
H	L	?	?	H	H
H	H	?	?	Z	?

IL = Illegal Z = High Impedence ? = Dont Care NC = No Change

Pull Cell Truth Table :

PA	PB	Function
0	0	Pull Down
0	1	Tristate
1	0	Bus Keeper

1	1	Pull Up

Power Characteristics:
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	607.444	uW

Power Characteristics:
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	282.664	uW

Power Characteristics:
Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	128.821	uW

Delay Characteristics: Time Units 1ns
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.143910**	**0.635010**	**1.57290**	**3.03400**	**5.08410**	**7.78170**
PADM to QC	TPLH	0.268000	0.398000	0.643000	0.998000	1.48000	2.11100	2.90700
PADM to QC	TPHL	0.282000	0.420000	0.687000	1.06700	1.58300	2.25200	3.09500

Delay Characteristics: Time Units 1ns
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		9.16967	**12.2726**	**23.1647**	**43.9647**	**76.3707**	**121.840**	**181.670**
A to PADM	TPLH	1.93300	2.29300	3.34400	5.13900	7.84000	11.5790	16.4620
A to PADM	TPHL	1.74600	2.09500	3.10600	4.75100	7.16200	10.4730	14.7890
EN to PADM three_state_disable	TLZ	0.277000						
EN to PADM three_state_disable	THZ	0.321000						
EN to PADM three_state_enable	TZH	2.34000	2.52400	3.22300	4.72300	7.02600	10.2140	14.3810
EN to PADM three_state_enable	TZL	2.30500	2.46800	3.10500	4.57200	6.82400	9.92000	13.9540

Delay Characteristics: Time Units 1ns
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.143910**	**0.635010**	**1.57290**	**3.03400**	**5.08410**	**7.78170**
PADM to QC	TPLH	0.378000	0.531000	0.829000	1.22200	1.73800	2.39500	3.20700
PADM to QC	TPHL	0.415000	0.610000	1.03800	1.67400	2.56100	3.73000	5.21000

Delay Characteristics: Time Units 1ns
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		8.34256	11.4455	22.3376	43.1376	75.5436	121.013	180.843
A to PADM	TPLH	3.18200	3.70400	5.23700	7.82000	11.6900	17.0520	24.0560
A to PADM	TPHL	2.89600	3.37100	4.75300	6.98300	10.2230	14.6620	20.4440
EN to PADM three_state_disable	TLZ	0.395000						
EN to PADM three_state_disable	THZ	0.514000						
EN to PADM three_state_enable	TZH	3.32600	3.77400	5.13600	7.49000	11.0260	15.9320	22.3520
EN to PADM three_state_enable	TZL	3.04600	3.44200	4.68400	6.82200	9.92200	14.1700	19.7060

Delay Characteristics: Time Units 1ns

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	0.143910	0.635010	1.57290	3.03400	5.08410	7.78170
PADM to QC	TPLH	0.719000	0.947000	1.45200	2.19100	3.19300	4.48800	6.10300
PADM to QC	TPHL	0.795000	1.07600	1.71500	2.69300	4.06200	5.86800	8.15300

Delay Characteristics: Time Units 1ns

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		7.80733	10.9102	21.8023	42.6023	75.0083	120.477	180.307
A to PADM	TPLH	6.50300	7.38100	10.0050	14.3650	20.8340	29.7810	41.4760
A to PADM	TPHL	6.13500	6.93100	9.24700	12.9220	18.1750	25.3380	34.6670
EN to PADM three_state_disable	TLZ	0.714000						
EN to PADM three_state_disable	THZ	0.990000						
EN to PADM three_state_enable	TZH	6.65800	7.50200	9.97100	14.0510	20.1170	28.5250	39.5350
EN to PADM three_state_enable	TZL	6.14500	6.94700	9.18800	12.7550	17.8770	24.8600	33.9580

Test Data

Parameter	Description	Minimum	Maximum	Units
Vih	High Level Input Voltage	(0.7*Vdd)	-	V
Vil	High Level Input Voltage	-	(0.3*Vdd)	V
ipu	Pull up current	-161.0	-40.0	uA
ipd	Pull down current	32.0	192.0	uA
ibkpu	Buskeeper pull-up current	-110.0	-28.0	uA
vtestbkpu	Test voltage for keeping the bus keeper pin high	(0.7*Vdd)	-	V
ibkpd	Buskeeper pull-down current	21.0	139.0	uA
vtestbkpd	Test voltage for keeping the bus keeper pin lob	-	(0.3*Vdd)	V
Iil	Low Level Input Current	-10.0	10.0	uA
Iih	High Level Input Current	-10.0	10.0	uA

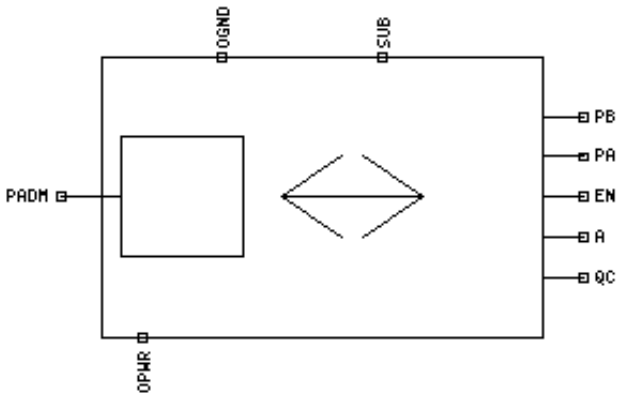
Vdiode_vdd	Diode voltage range to Vdd	0.20	1.10	V
Vi_max	Maximum Voltage	-0.5	(1.10 * Vdd)	V
I_max	Maximum sink/source current	-100	100	mA
Vdiode_vss	Diode voltage to Vss	-1.10	-0.20	V
Voh	High Level Output Voltage	2.4	Vdd	V
Vol	Low Level Output Voltage	0.0	0.4	V
Iol	Low Level Output Current	3.12	-	mA
Ioh	High Level Output Current	-	-3.39	mA

ioacx6c3csxe08_mt

Description

"IOACX6C3CSXE08_MT is a[n] IOACX6C3CSXE08 is a non-inverting, CMOS-level composite IO with a 8X drive, tri-state output buffer piece with a active low enable and controlled slew rate output, a programmable pull-up/pull-down/bus-hold piece, and input buffer piece. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
PA	0.0382265 (pF)
A	0.0311864 (pF)
PB	0.0388941 (pF)
PADM	6.66982 (pF)
EN	0.0343174 (pF)

AREA : 27735.0 sqr microns

Truth Table

A input	EN input	PA input	PB input	PADM inout	QC output
L	L	?	?	L	L
L	H	?	?	Z	?
H	L	?	?	H	H
H	H	?	?	Z	?

IL = Illegal Z = High Impedence ? = Dont Care NC = No Change

Pull Cell Truth Table :

PA	PB	Function
0	0	Pull Down
0	1	Tristate
1	0	Bus Keeper

1	1	Pull Up

Power Characteristics:
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	607.448	uW

Power Characteristics:
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	282.664	uW

Power Characteristics:
Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	128.821	uW

Delay Characteristics: Time Units 1ns
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.143910**	**0.635010**	**1.57290**	**3.03400**	**5.08410**	**7.78170**
PADM to QC	TPLH	0.268000	0.398000	0.643000	0.998000	1.48000	2.11100	2.90700
PADM to QC	TPHL	0.282000	0.420000	0.687000	1.06700	1.58300	2.25200	3.09500

Delay Characteristics: Time Units 1ns
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		9.16982	**12.2727**	**23.1648**	**43.9648**	**76.3708**	**121.840**	**181.670**
A to PADM	TPLH	2.17700	2.51000	3.37500	4.62600	6.32100	8.57200	11.4760
A to PADM	TPHL	2.19100	2.52100	3.39500	4.62100	6.18100	8.13300	10.5570
EN to PADM three_state_disable	TLZ	0.375000						
EN to PADM three_state_disable	THZ	0.402000						
EN to PADM three_state_enable	TZH	2.41500	2.61400	3.22800	4.20700	5.49900	7.19100	9.36900
EN to PADM three_state_enable	TZL	2.43500	2.64100	3.32900	4.45300	5.87000	7.62500	9.79500

Delay Characteristics: Time Units 1ns
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.143910**	**0.635010**	**1.57290**	**3.03400**	**5.08410**	**7.78170**
PADM to QC	TPLH	0.378000	0.531000	0.829000	1.22200	1.73800	2.39500	3.20700
PADM to QC	TPHL	0.415000	0.610000	1.03800	1.67400	2.56100	3.73000	5.21000

Delay Characteristics: Time Units 1ns
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		8.34273	**11.4456**	**22.3377**	**43.1377**	**75.5437**	**121.013**	**180.843**
A to PADM	TPLH	3.54500	4.00900	5.23900	7.01400	9.37800	12.4760	16.4490
A to PADM	TPHL	3.74000	4.19800	5.42200	7.13100	9.27600	11.9230	15.1740
EN to PADM three_state_disable	TLZ	0.513000						
EN to PADM three_state_disable	THZ	0.643000						
EN to PADM three_state_enable	TZH	3.63400	4.04700	5.13400	6.67700	8.70000	11.3330	14.7070
EN to PADM three_state_enable	TZL	3.75600	4.18700	5.34900	6.98100	9.00400	11.4800	14.5090

Delay Characteristics: Time Units 1ns

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.143910**	**0.635010**	**1.57290**	**3.03400**	**5.08410**	**7.78170**
PADM to QC	TPLH	0.719000	0.947000	1.45200	2.19100	3.19300	4.48800	6.10300
PADM to QC	TPHL	0.795000	1.07600	1.71500	2.69300	4.06200	5.86800	8.15300

Delay Characteristics: Time Units 1ns

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		7.80748	**10.9104**	**21.8025**	**42.6025**	**75.0085**	**120.477**	**180.307**
A to PADM	TPLH	7.15400	7.93200	10.0630	13.1240	17.1060	22.2040	28.6490
A to PADM	TPHL	8.08500	8.89300	11.0480	14.0040	17.6200	21.9750	27.2170
EN to PADM three_state_disable	TLZ	0.916000						
EN to PADM three_state_disable	THZ	1.23100						
EN to PADM three_state_enable	TZH	7.30300	8.04600	10.0200	12.7970	16.3680	20.9130	26.6570
EN to PADM three_state_enable	TZL	8.07300	8.88900	10.9810	13.8450	17.3520	21.5560	26.6010

Test Data

Parameter	Description	Minimum	Maximum	Units
Vih	High Level Input Voltage	(0.7*Vdd)	-	V
Vil	High Level Input Voltage	-	(0.3*Vdd)	V
ipu	Pull up current	-161.0	-40.0	uA
ipd	Pull down current	32.0	192.0	uA
ibkpu	Buskeeper pull-up current	-110.0	-28.0	uA
vtestbkpu	Test voltage for keeping the bus keeper pin high	(0.7*Vdd)	-	V
ibkpd	Buskeeper pull-down current	21.0	139.0	uA
vtestbkpd	Test voltage for keeping the bus keeper pin lob	-	(0.3*Vdd)	V
Iil	Low Level Input Current	-10.0	10.0	uA
Iih	High Level Input Current	-10.0	10.0	uA

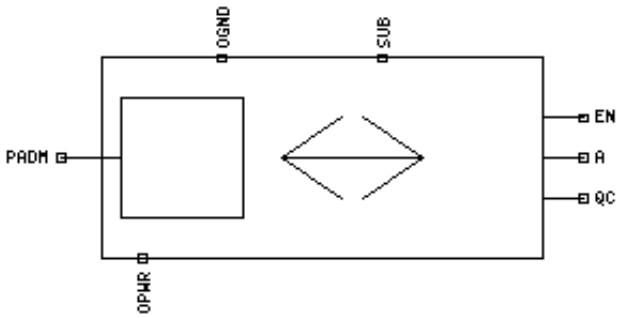
Vdiode_vdd	Diode voltage range to Vdd	0.20	1.10	V
Vi_max	Maximum Voltage	-0.5	(1.10 * Vdd)	V
I_max	Maximum sink/source current	-100	100	mA
Vdiode_vss	Diode voltage to Vss	-1.10	-0.20	V
Voh	High Level Output Voltage	2.4	Vdd	V
Vol	Low Level Output Voltage	0.0	0.4	V
Iol	Low Level Output Current	6.25	-	mA
Ioh	High Level Output Current	-	-6.79	mA

ioacx6xxcsxe02_mt

Description

"IOACX6XXCSXE02_MT is a[n] IOACX6XXCSXE02 is a non-inverting, CMOS-level composite IO with an 2X drive, tri-state output buffer piece with active low enable, controlled slew rate output, and an input buffer piece. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
A	0.0310386 (pF)
PADM	4.72984 (pF)
EN	0.0343361 (pF)

AREA : 27735.0 sqr microns

Truth Table

A input	EN input	PADM inout	QC output
L	L	L	L
L	H	Z	?
H	L	H	H
H	H	Z	?

IL = Illegal Z = High Impedence ? = Dont Care NC = No Change

Power Characteristics:

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	0.000109801	uW

Power Characteristics:
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	0.000215424	uW

Power Characteristics:
Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	0.0894757	uW

Delay Characteristics: Time Units 1ns
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.143910**	**0.635010**	**1.57290**	**3.03400**	**5.08410**	**7.78170**
PADM to QC	TPLH	0.269000	0.399000	0.645000	0.999000	1.48100	2.11200	2.90800
PADM to QC	TPHL	0.283000	0.422000	0.688000	1.06900	1.58400	2.25400	3.09600

Delay Characteristics: Time Units 1ns
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		7.22984	**10.3328**	**21.2248**	**42.0248**	**74.4308**	**119.900**	**179.730**
A to PADM	TPLH	1.99000	2.51600	4.24600	7.41400	12.2640	19.0140	27.8630
A to PADM	TPHL	1.69500	2.09800	3.35500	5.57300	8.93400	13.5950	19.6850
EN to PADM three_state_disable	TLZ	0.247000						
EN to PADM three_state_disable	THZ	0.276000						
EN to PADM three_state_enable	TZH	2.65300	2.97600	4.17900	6.98500	11.4250	17.6150	25.7290
EN to PADM three_state_enable	TZL	2.41300	2.62700	3.43400	5.42200	8.64800	13.1230	18.9710

Delay Characteristics: Time Units 1ns
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.143910**	**0.635010**	**1.57290**	**3.03400**	**5.08410**	**7.78170**
PADM to QC	TPLH	0.379000	0.532000	0.830000	1.22300	1.73900	2.39700	3.20900
PADM to QC	TPHL	0.416000	0.612000	1.04000	1.67600	2.56300	3.73200	5.21200

Delay Characteristics: Time Units 1ns
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		7.24838	**10.3514**	**21.2434**	**42.0434**	**74.4494**	**119.918**	**179.748**
A to PADM	TPLH	3.32200	4.09000	6.62100	11.2810	18.4470	28.4370	41.5360
A to PADM	TPHL	2.76400	3.30700	5.00400	7.98600	12.5090	18.7820	26.9800
	TLZ	0.351000						

EN to PADM three_state_disable								
EN to PADM three_state_disable	THZ	0.440000						
EN to PADM three_state_enable	TZH	3.56700	4.22100	6.51000	10.9330	17.7510	27.2730	39.7670
EN to PADM three_state_enable	TZL	3.03500	3.47300	4.96800	7.85900	12.2610	18.3710	26.3620

Delay Characteristics: Time Units 1ns

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.143910**	**0.635010**	**1.57290**	**3.03400**	**5.08410**	**7.78170**
PADM to QC	TPLH	0.721000	0.949000	1.45400	2.19300	3.19500	4.49000	6.10600
PADM to QC	TPHL	0.796000	1.07800	1.71600	2.69500	4.06400	5.87000	8.15500

Delay Characteristics: Time Units 1ns

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		7.28967	**10.3927**	**21.2847**	**42.0847**	**74.4907**	**119.960**	**179.790**
A to PADM	TPLH	6.73400	8.00200	12.2520	20.1530	32.3500	49.3780	71.7160
A to PADM	TPHL	5.74600	6.64200	9.42900	14.2770	21.6220	31.8400	45.2120
EN to PADM three_state_disable	TLZ	0.641000						
EN to PADM three_state_disable	THZ	0.854000						
EN to PADM three_state_enable	TZH	6.87800	8.10800	12.2000	19.8120	31.5900	48.0600	69.6860
EN to PADM three_state_enable	TZL	5.80300	6.70200	9.41500	14.1650	21.3970	31.4640	44.6440

Test Data

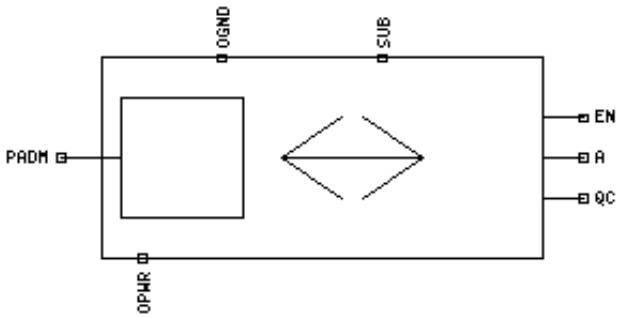
Parameter	Description	Minimum	Maximum	Units
Vih	High Level Input Voltage	(0.7*Vdd)	-	V
Vil	High Level Input Voltage	-	(0.3*Vdd)	V
Iil	Low Level Input Current	-10.0	10.0	uA
Iih	High Level Input Current	-10.0	10.0	uA
Vdiode_vdd	Diode voltage range to Vdd	0.20	1.10	V
Vi_max	Maximum Voltage	-0.5	(1.10 * Vdd)	V
I_max	Maximum sink/source current	-100	100	mA
Vdiode_vss	Diode voltage to Vss	-1.10	-0.20	V
Voh	High Level Output Voltage	2.4	Vdd	V
Vol	Low Level Output Voltage	0.0	0.4	V
Iol	Low Level Output Current	2.0	-	mA
Ioh	High Level Output Current	-	-1.7	mA

ioacx6xxcsxe04_mt

Description

"IOACX6XXCSXE04_MT is a[n] IOACX6XXCSXE04 is a non-inverting, CMOS-level composite IO with an 4X drive, tri-state output buffer piece with active low enable, controlled slew rate output, and an input buffer piece. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
A	0.0310208 (pF)
PADM	4.6284 (pF)
EN	0.0343174 (pF)

AREA : 27735.0 sqr microns

Truth Table

A input	EN input	PADM inout	QC output
L	L	L	L
L	H	Z	?
H	L	H	H
H	H	Z	?

IL = Illegal Z = High Impedence ? = Dont Care NC = No Change

Power Characteristics:

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	0.000101264	uW

Power Characteristics:
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	0.000203306	uW

Power Characteristics:
Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	0.0889381	uW

Delay Characteristics: Time Units 1ns
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.143890**	**0.634950**	**1.57270**	**3.03360**	**5.08350**	**7.78090**
PADM to QC	TPLH	0.268000	0.398000	0.644000	0.998000	1.48000	2.11100	2.90700
PADM to QC	TPHL	0.283000	0.421000	0.687000	1.06800	1.58400	2.25300	3.09500

Delay Characteristics: Time Units 1ns
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		7.12840	**10.2314**	**21.1234**	**41.9234**	**74.3294**	**119.798**	**179.628**
A to PADM	TPLH	1.91800	2.28100	3.33200	5.12700	7.82900	11.5660	16.4500
A to PADM	TPHL	1.73300	2.08300	3.09600	4.74200	7.15200	10.4630	14.7780
EN to PADM three_state_disable	TLZ	0.277000						
EN to PADM three_state_disable	THZ	0.321000						
EN to PADM three_state_enable	TZH	2.32600	2.50800	3.20500	4.70200	6.99600	10.1720	14.3250
EN to PADM three_state_enable	TZL	2.29800	2.46300	3.10800	4.58900	6.86200	9.98800	14.0620

Delay Characteristics: Time Units 1ns
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.143890**	**0.634950**	**1.57270**	**3.03360**	**5.08350**	**7.78090**
PADM to QC	TPLH	0.378000	0.532000	0.829000	1.22200	1.73800	2.39500	3.20800
PADM to QC	TPHL	0.415000	0.611000	1.03900	1.67500	2.56200	3.73000	5.21000

Delay Characteristics: Time Units 1ns
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		7.14391	**10.2469**	**21.1389**	**41.9389**	**74.3449**	**119.814**	**179.644**
A to PADM	TPLH	3.16100	3.68600	5.21900	7.80200	11.6730	17.0330	24.0380
A to PADM	TPHL	2.87800	3.35400	4.73900	6.97100	10.2090	14.6490	20.4300
	TLZ	0.395000						

EN to PADM three_state_disable								
EN to PADM three_state_disable	THZ	0.514000						
EN to PADM three_state_enable	TZH	3.29900	3.74800	5.10900	7.45900	10.9830	15.8750	22.2770
EN to PADM three_state_enable	TZL	3.03800	3.43700	4.68800	6.84100	9.95900	14.2340	19.8070

Delay Characteristics: Time Units 1ns

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	0.143890	0.634950	1.57270	3.03360	5.08350	7.78090
PADM to QC	TPLH	0.720000	0.948000	1.45300	2.19200	3.19300	4.48800	6.10300
PADM to QC	TPHL	0.796000	1.07700	1.71500	2.69300	4.06300	5.86800	8.15300

Delay Characteristics: Time Units 1ns

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		7.18159	10.2846	21.1766	41.9766	74.3826	119.852	179.682
A to PADM	TPLH	6.45500	7.33900	9.96800	14.3310	20.8010	29.7460	41.4420
A to PADM	TPHL	6.09600	6.89700	9.22000	12.8990	18.1520	25.3140	34.6440
EN to PADM three_state_disable	TLZ	0.714000						
EN to PADM three_state_disable	THZ	0.990000						
EN to PADM three_state_enable	TZH	6.59800	7.44700	9.92000	13.9960	20.0490	28.4380	39.4230
EN to PADM three_state_enable	TZL	6.13200	6.94000	9.19400	12.7780	17.9210	24.9350	34.0740

Test Data

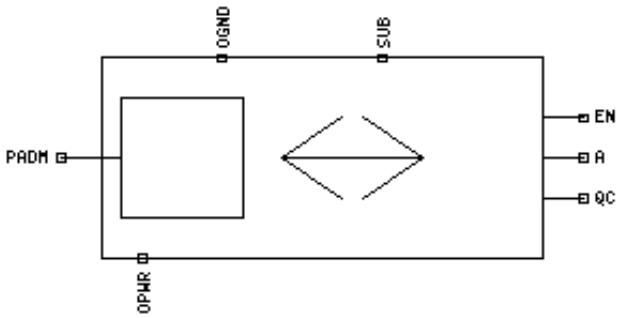
Parameter	Description	Minimum	Maximum	Units
Vih	High Level Input Voltage	(0.7*Vdd)	-	V
Vil	High Level Input Voltage	-	(0.3*Vdd)	V
Iil	Low Level Input Current	-10.0	10.0	uA
Iih	High Level Input Current	-10.0	10.0	uA
Vdiode_vdd	Diode voltage range to Vdd	0.20	1.10	V
Vi_max	Maximum Voltage	-0.5	(1.10 * Vdd)	V
I_max	Maximum sink/source current	-100	100	mA
Vdiode_vss	Diode voltage to Vss	-1.10	-0.20	V
Voh	High Level Output Voltage	2.4	Vdd	V
Vol	Low Level Output Voltage	0.0	0.4	V
Iol	Low Level Output Current	3.12	-	mA
Ioh	High Level Output Current	-	-3.39	mA

ioacx6xxcsxe08_mt

Description

"IOACX6XXCSXE08_MT is a[n] IOACX6XXCSXE08 is a non-inverting, CMOS-level composite IO with an 8X drive, tri-state output buffer piece with active low enable, controlled slew rate output, and an input buffer piece. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
A	0.0310205 (pF)
PADM	4.62856 (pF)
EN	0.0343174 (pF)

AREA : 27735.0 sqr microns

Truth Table

A input	EN input	PADM inout	QC output
L	L	L	L
L	H	Z	?
H	L	H	H
H	H	Z	?

IL = Illegal Z = High Impedence ? = Dont Care NC = No Change

Power Characteristics:

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	0.000101252	uW

Power Characteristics:
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	0.000203301	uW

Power Characteristics:
Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	0.0889378	uW

Delay Characteristics: Time Units 1ns
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.143910**	**0.635010**	**1.57290**	**3.03400**	**5.08410**	**7.78170**
PADM to QC	TPLH	0.268000	0.398000	0.644000	0.998000	1.48000	2.11100	2.90700
PADM to QC	TPHL	0.283000	0.421000	0.687000	1.06800	1.58400	2.25300	3.09500

Delay Characteristics: Time Units 1ns
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		7.12856	**10.2316**	**21.1236**	**41.9236**	**74.3296**	**119.799**	**179.629**
A to PADM	TPLH	2.16300	2.50000	3.36700	4.62000	6.31500	8.56600	11.4710
A to PADM	TPHL	2.17800	2.51000	3.38700	4.61500	6.17500	8.12800	10.5520
EN to PADM three_state_disable	TLZ	0.375000						
EN to PADM three_state_disable	THZ	0.402000						
EN to PADM three_state_enable	TZH	2.40100	2.60100	3.21700	4.19700	5.48700	7.17700	9.35100
EN to PADM three_state_enable	TZL	2.42900	2.63700	3.33200	4.46400	5.88800	7.65400	9.83700

Delay Characteristics: Time Units 1ns
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.143910**	**0.635010**	**1.57290**	**3.03400**	**5.08410**	**7.78170**
PADM to QC	TPLH	0.378000	0.532000	0.829000	1.22200	1.73800	2.39600	3.20800
PADM to QC	TPHL	0.415000	0.611000	1.03900	1.67500	2.56200	3.73100	5.21100

Delay Characteristics: Time Units 1ns
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		7.14404	**10.2470**	**21.1390**	**41.9390**	**74.3450**	**119.814**	**179.644**
A to PADM	TPLH	3.52500	3.99400	5.22700	7.00400	9.36900	12.4660	16.4400
A to PADM	TPHL	3.72100	4.18200	5.41000	7.12300	9.26800	11.9160	15.1670
	TLZ	0.513000						

EN to PADM three_state_disable								
EN to PADM three_state_disable	THZ	0.643000						
EN to PADM three_state_enable	TZH	3.60800	4.02600	5.11600	6.66200	8.68200	11.3120	14.6820
EN to PADM three_state_enable	TZL	3.75100	4.18600	5.35400	6.99300	9.02300	11.5080	14.5490

Delay Characteristics: Time Units 1ns

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	0.143910	0.635010	1.57290	3.03400	5.08410	7.78170
PADM to QC	TPLH	0.720000	0.948000	1.45300	2.19200	3.19300	4.48800	6.10400
PADM to QC	TPHL	0.796000	1.07700	1.71500	2.69400	4.06300	5.86900	8.15400

Delay Characteristics: Time Units 1ns

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		7.18174	10.2847	21.1767	41.9767	74.3827	119.852	179.682
A to PADM	TPLH	7.11100	7.89700	10.0360	13.1030	17.0880	22.1850	28.6320
A to PADM	TPHL	8.04300	8.85900	11.0250	13.9880	17.6060	21.9620	27.2050
EN to PADM three_state_disable	TLZ	0.916000						
EN to PADM three_state_disable	THZ	1.23100						
EN to PADM three_state_enable	TZH	7.24900	8.00000	9.98400	12.7670	16.3370	20.8790	26.6180
EN to PADM three_state_enable	TZL	8.06800	8.89000	10.9910	13.8640	17.3780	21.5910	26.6480

Test Data

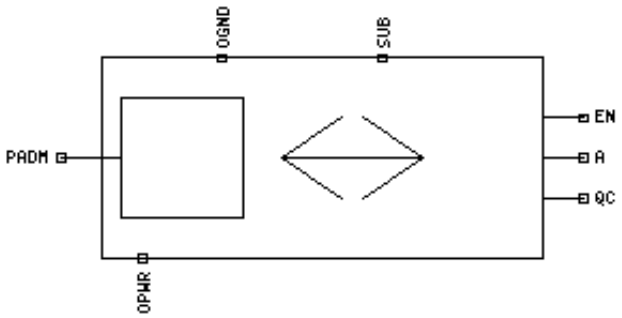
Parameter	Description	Minimum	Maximum	Units
Vih	High Level Input Voltage	(0.7*Vdd)	-	V
Vil	High Level Input Voltage	-	(0.3*Vdd)	V
Iil	Low Level Input Current	-10.0	10.0	uA
Iih	High Level Input Current	-10.0	10.0	uA
Vdiode_vdd	Diode voltage range to Vdd	0.20	1.10	V
Vi_max	Maximum Voltage	-0.5	(1.10 * Vdd)	V
I_max	Maximum sink/source current	-100	100	mA
Vdiode_vss	Diode voltage to Vss	-1.10	-0.20	V
Voh	High Level Output Voltage	2.4	Vdd	V
Vol	Low Level Output Voltage	0.0	0.4	V
Iol	Low Level Output Current	6.25	-	mA
Ioh	High Level Output Current	-	-6.79	mA

ioacxtxxcste08_mt

Description

"IOACXTXXCSTE08_MT is a[n] IOACXTXXCSTE08 is a 5V-tolerant, non-inverting, CMOS-level composite IO with a 8X drive, tri-state output buffer piece that has a active low enable and controlled slew rate output, and an input buffer piece. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
A	0.0314849 (pF)
PADM	5.44426 (pF)
EN	0.0613587 (pF)

AREA : 27735.0 sqr microns

Truth Table

A input	EN input	PADM inout	QC output
L	L	L	L
L	H	Z	?
H	L	H	H
H	H	Z	?

IL = Illegal Z = High Impedence ? = Dont Care NC = No Change

Power Characteristics:

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	0.000142405	uW

Power Characteristics:
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	0.000189555	uW

Power Characteristics:
Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	0.0869607	uW

Delay Characteristics: Time Units 1ns
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.147050**	**0.649180**	**1.60810**	**3.10200**	**5.19810**	**7.95630**
PADM to QC	TPLH	0.367000	0.487000	0.768000	1.18800	1.76600	2.52200	3.47500
PADM to QC	TPHL	0.340000	0.489000	0.773000	1.18800	1.74800	2.47300	3.37800

Delay Characteristics: Time Units 1ns
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		7.94426	**11.0473**	**21.9393**	**42.7393**	**75.1453**	**120.614**	**180.444**
A to PADM	TPLH	2.62000	2.96300	3.87100	5.18000	6.92100	9.20300	12.1260
A to PADM	TPHL	2.52700	2.83800	3.65500	4.75900	6.10200	7.73300	9.71300
EN to PADM three_state_disable	TLZ	0.589000						
EN to PADM three_state_disable	THZ	0.561000						
EN to PADM three_state_enable	TZH	2.81100	3.06800	3.81600	4.90200	6.28100	8.04300	10.2760
EN to PADM three_state_enable	TZL	2.62700	2.86400	3.59300	4.60600	5.81000	7.24800	8.97800

Delay Characteristics: Time Units 1ns
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.147050**	**0.649180**	**1.60810**	**3.10200**	**5.19810**	**7.95630**
PADM to QC	TPLH	0.592000	0.683000	0.994000	1.44400	2.04400	2.81000	3.75800
PADM to QC	TPHL	0.504000	0.717000	1.16100	1.84400	2.79500	4.04700	5.62700

Delay Characteristics: Time Units 1ns
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		7.93926	**11.0423**	**21.9343**	**42.7343**	**75.1403**	**120.609**	**180.439**
A to PADM	TPLH	4.27300	4.75300	6.04800	7.91200	10.3550	13.5090	17.5180
A to PADM	TPHL	4.39100	4.83500	6.00400	7.57400	9.47500	11.7880	14.5950
	TLZ	0.799000						

EN to PADM three_state_disable								
EN to PADM three_state_disable	THZ	0.894000						
EN to PADM three_state_enable	TZH	4.44200	4.87900	6.07500	7.75800	9.91300	12.6550	16.1130
EN to PADM three_state_enable	TZL	4.41400	4.84000	5.95100	7.44600	9.23000	11.3770	13.9700

Delay Characteristics: Time Units 1ns

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.147050**	**0.649180**	**1.60810**	**3.10200**	**5.19810**	**7.95630**
PADM to QC	TPLH	1.37600	1.40300	1.79100	2.53000	3.57100	4.92400	6.60800
PADM to QC	TPHL	0.946000	1.25400	1.94700	2.99100	4.46200	6.40600	8.85900

Delay Characteristics: Time Units 1ns

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		8.01837	**11.1214**	**22.0134**	**42.8134**	**75.2194**	**120.688**	**180.518**
A to PADM	TPLH	8.67600	9.49700	11.7650	15.0130	19.1770	24.4170	30.9580
A to PADM	TPHL	9.59500	10.4190	12.5660	15.4040	18.8370	23.0030	28.0140
EN to PADM three_state_disable	TLZ	1.44700						
EN to PADM three_state_disable	THZ	1.80000						
EN to PADM three_state_enable	TZH	9.04400	9.81700	11.9650	14.9990	18.8250	23.5950	29.5140
EN to PADM three_state_enable	TZL	9.63800	10.4640	12.5390	15.2830	18.6100	22.6320	27.4540

Test Data

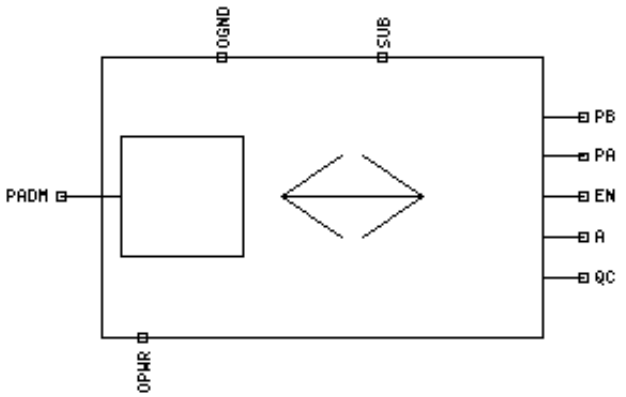
Parameter	Description	Minimum	Maximum	Units
Vih	High Level Input Voltage	(0.7*Vdd)	-	V
Vil	High Level Input Voltage	-	(0.3*Vdd)	V
Iil	Low Level Input Current	-10.0	10.0	uA
Iih	High Level Input Current	-10.0	10.0	uA
Vi_max	Maximum Voltage	-0.5	5.0	V
I_max	Maximum sink/source current	-100	100	mA
Vdiode_vss	Diode voltage to Vss	-1.10	-0.20	V
Voh	High Level Output Voltage	2.4	Vdd	V
Vol	Low Level Output Voltage	0.0	0.4	V
Iol	Low Level Output Current	6.47	-	mA
Ioh	High Level Output Current	-	-6.76	mA

ioavx6c3vxxe02_mt

Description

"IOAVX6C3VXXE02_MT is a[n] IOAVX6C3VXXE02 is a non-inverting, LVTTL-level composite IO with a 2X drive, tri-state output buffer piece with a active low enable and controlled slew rate output, a programmable pull-up/pull-down/bus-hold piece, and input buffer piece. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
PA	0.0382265 (pF)
A	0.0311861 (pF)
PB	0.0388944 (pF)
PADM	6.77046 (pF)
EN	0.0343174 (pF)

AREA : 27735.0 sqr microns

Truth Table

A input	EN input	PA input	PB input	PADM inout	QC output
L	L	?	?	L	L
L	H	?	?	Z	?
H	L	?	?	H	H
H	H	?	?	Z	?

IL = Illegal Z = High Impedence ? = Dont Care NC = No Change

Pull Cell Truth Table :

PA	PB	Function
0	0	Pull Down
0	1	Tristate
1	0	Bus Keeper

1	1	Pull Up

Power Characteristics:
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	607.437	uW

Power Characteristics:
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	282.664	uW

Power Characteristics:
Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	128.821	uW

Delay Characteristics: Time Units 1ns
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.143880**	**0.634900**	**1.57260**	**3.03340**	**5.08320**	**7.78040**
PADM to QC	TPLH	0.264000	0.390000	0.626000	0.970000	1.44200	2.06000	2.84300
PADM to QC	TPHL	0.255000	0.394000	0.680000	1.10800	1.70700	2.50000	3.51100

Delay Characteristics: Time Units 1ns
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		9.27046	**12.3735**	**23.2655**	**44.0655**	**76.4715**	**121.940**	**181.770**
A to PADM	TPLH	1.12300	1.64400	3.37900	6.55000	11.3990	18.1500	26.9930
A to PADM	TPHL	0.850000	1.20900	2.42000	4.62600	7.98300	12.6370	18.7210
EN to PADM three_state_disable	TLZ	0.281000						
EN to PADM three_state_disable	THZ	0.293000						
EN to PADM three_state_enable	TZH	2.64400	2.94900	3.97000	6.15100	10.6260	16.8600	25.0350
EN to PADM three_state_enable	TZL	2.34300	2.51100	3.07700	4.43700	7.62000	12.0300	17.7960

Delay Characteristics: Time Units 1ns
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.143880**	**0.634900**	**1.57260**	**3.03340**	**5.08320**	**7.78040**
PADM to QC	TPLH	0.377000	0.532000	0.840000	1.26100	1.83000	2.57000	3.49600
PADM to QC	TPHL	0.370000	0.553000	0.968000	1.59800	2.48900	3.67300	5.18000

Delay Characteristics: Time Units 1ns
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		8.44667	11.5497	22.4417	43.2417	75.6477	121.117	180.947
A to PADM	TPLH	1.83700	2.59400	5.12300	9.78700	16.9550	26.9490	40.0510
A to PADM	TPHL	1.28300	1.75000	3.35600	6.31200	10.8270	17.0920	25.2870
EN to PADM three_state_disable	TLZ	0.398000						
EN to PADM three_state_disable	THZ	0.471000						
EN to PADM three_state_enable	TZH	3.20800	3.74600	5.54700	9.47900	16.3380	25.9170	38.4880
EN to PADM three_state_enable	TZL	2.58800	2.86900	3.81800	6.13900	10.4990	16.5520	24.4690

Delay Characteristics: Time Units 1ns

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	0.143880	0.634900	1.57260	3.03340	5.08320	7.78040
PADM to QC	TPLH	0.714000	0.964000	1.49600	2.29200	3.39500	4.84000	6.66300
PADM to QC	TPHL	0.711000	0.961000	1.55200	2.47400	3.77600	5.50100	7.69200

Delay Characteristics: Time Units 1ns

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		7.91511	11.0181	21.9101	42.7101	75.1161	120.585	180.415
A to PADM	TPLH	3.55800	4.76100	8.96300	16.8590	29.0590	46.0920	68.4340
A to PADM	TPHL	2.48900	3.20800	5.74300	10.4980	17.8220	28.0260	41.3860
EN to PADM three_state_disable	TLZ	0.737000						
EN to PADM three_state_disable	THZ	0.907000						
EN to PADM three_state_enable	TZH	4.50700	5.49000	8.95700	16.5710	28.4010	44.9470	66.6750
EN to PADM three_state_enable	TZL	3.28400	3.82600	5.76400	10.3090	17.4810	27.4800	40.5760

Test Data

Parameter	Description	Minimum	Maximum	Units
Vih	High Level Input Voltage	2.0v	-	V
Vil	High Level Input Voltage	-	0.8v	V
ipu	Pull up current	-161.0	-40.0	uA
ipd	Pull down current	32.0	192.0	uA
ibkpu	Buskeeper pull-up current	-110.0	-28.0	uA
vtestbkpu	Test voltage for keeping the bus keeper pin high	(0.7*Vdd)	-	V
ibkpd	Buskeeper pull-down current	21.0	139.0	uA
vtestbkpd	Test voltage for keeping the bus keeper pin lob	-	(0.3*Vdd)	V
Iil	Low Level Input Current	-10.0	10.0	uA
Iih	High Level Input Current	-10.0	10.0	uA

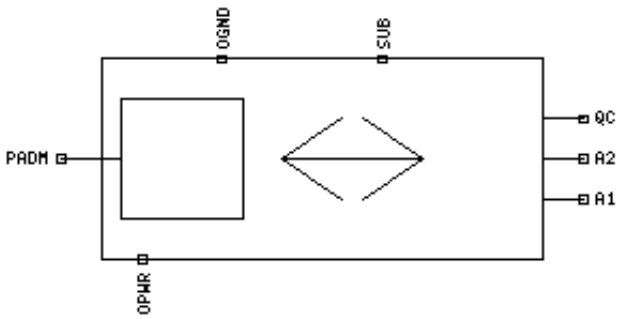
Vdiode_vdd	Diode voltage range to Vdd	0.20	1.10	V
Vi_max	Maximum Voltage	-0.5	(1.10 * Vdd)	V
I_max	Maximum sink/source current	-100	100	mA
Vdiode_vss	Diode voltage to Vss	-1.10	-0.20	V
Voh	High Level Output Voltage	2.4	Vdd	V
Vol	Low Level Output Voltage	0.0	0.4	V
Iol	Low Level Output Current	2.0	-	mA
Ioh	High Level Output Current	-	-1.7	mA

iosna4_mt

Description

"IOSNA4_MT is a[n] IOSNA4 is a non-buffered, resistive analog interface input piece. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
PADM	7.54533 (pF)

AREA : 27735.0 sqr microns

Truth Table

PADM input	A1 output	A2 output	QC output
L	L	?	?
H	H	?	?
L	?	L	?
H	?	H	?
L	?	?	L
H	?	?	H

IL = Illegal Z = High Impedence ? = Dont Care NC = No Change

Power Characteristics:

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	3.00583e-07	uW

Power Characteristics:
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	1.56371e-06	uW

Power Characteristics:
Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	0.0772773	uW

Delay Characteristics: Time Units 1ns
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.0938690**	**0.409330**	**1.01180**	**1.95030**	**3.26720**	**5.00000**
PADM to A1	TPLH	0.0210000	0.00100000	0.00200000	0.00300000	0.00400000	0.00500000	0.00600000
PADM to A1	TPHL	0.0840000	0.221000	0.622000	1.36400	2.51400	4.12700	6.24900
PADM to A2	TPLH	0.0210000	0.00100000	0.00200000	0.00300000	0.00400000	0.00500000	0.00600000
PADM to A2	TPHL	0.0840000	0.221000	0.622000	1.36400	2.51400	4.12700	6.24900
PADM to QC	TPLH	0.00000	0.00100000	0.00200000	0.00300000	0.00400000	0.00500000	0.00600000
PADM to QC	TPHL	0.00800000	0.0350000	0.131000	0.311000	0.593000	0.987000	1.50600

Delay Characteristics: Time Units 1ns
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.0938690**	**0.409330**	**1.01180**	**1.95030**	**3.26720**	**5.00000**
PADM to A1	TPLH	0.0190000	0.00100000	0.00200000	0.00300000	0.00400000	0.00500000	0.00600000
PADM to A1	TPHL	0.0800000	0.221000	0.662000	1.46100	2.69800	4.43100	6.71100
PADM to A2	TPLH	0.0190000	0.00100000	0.00200000	0.00300000	0.00400000	0.00500000	0.00600000
PADM to A2	TPHL	0.0790000	0.221000	0.662000	1.46100	2.69800	4.43100	6.71100
PADM to QC	TPLH	0.00000	0.00100000	0.00200000	0.00300000	0.00400000	0.00500000	0.00600000
PADM to QC	TPHL	0.00800000	0.0350000	0.131000	0.311000	0.593000	0.987000	1.50600

Delay Characteristics: Time Units 1ns
Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		0.00400000	**0.0938690**	**0.409330**	**1.01180**	**1.95030**	**3.26720**	**5.00000**
PADM to A1	TPLH	0.0420000	0.00100000	0.00200000	0.00300000	0.00400000	0.00500000	0.00600000
PADM to A1	TPHL	0.103000	0.246000	0.671000	1.46600	2.70400	4.44000	6.72500
PADM to A2	TPLH	0.0420000	0.00100000	0.00200000	0.00300000	0.00400000	0.00500000	0.00600000
PADM to A2	TPHL	0.103000	0.246000	0.671000	1.46600	2.70400	4.44000	6.72500
PADM to QC	TPLH	0.00000	0.00100000	0.00200000	0.00300000	0.00400000	0.00500000	0.00600000
PADM to QC	TPHL	0.00800000	0.0350000	0.131000	0.311000	0.593000	0.987000	1.50600

Test Data

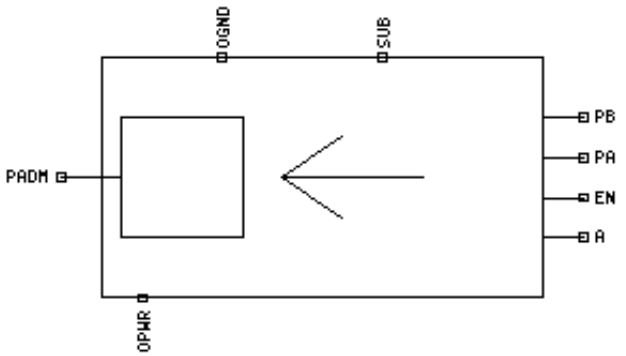
Parameter	Description	Minimum	Maximum	Units
Iil	Low Level Input Current	-1.0	1.0	uA
Iih	High Level Input Current	-1.0	1.0	uA
Vi_max	Maximum Voltage	-0.5	(1.10 * Vdd)	V
I_max	Maximum sink/source current	-100	100	mA
Vdiode_vss	Diode voltage to Vss	-1.10	-0.20	V
Vdiode_vdd	Diode voltage range to Vdd	0.20	1.10	V

obac3csxe02_mt

Description

"OBAC3CSXE02_MT is a[n] OBAC3CSXE02 is a 2X drive, non-inverting, CMOS-level, tri-state composite output buffer with a programmable pull-up/pull-down/bus-hold piece, active low enable and controlled slew rate output. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
PA	0.0381426 (pF)
A	0.0311867 (pF)
PB	0.03888 (pF)
EN	0.0343174 (pF)

AREA : 27735.0 sqr microns

Truth Table

A input	EN input	PA input	PB input	PADM output
L	L	?	?	L
L	H	?	?	Z
H	L	?	?	H
H	H	?	?	Z

IL = Illegal Z = High Impedence ? = Dont Care NC = No Change

Pull Cell Truth Table :

PA	PB	Function
0	0	Pull Down
0	1	Tristate
1	0	Bus Keeper

1	1	Pull Up

Power Characteristics:
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	607.437	uW

Power Characteristics:
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	282.664	uW

Power Characteristics:
Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	128.823	uW

Delay Characteristics: Time Units 1ns
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		7.74637	**10.8494**	**21.7414**	**42.5414**	**74.9474**	**120.416**	**180.246**
A to PADM	TPLH	1.99100	2.51700	4.24800	7.41500	12.2650	19.0150	27.8640
A to PADM	TPHL	1.69600	2.10000	3.35500	5.57400	8.93600	13.5950	19.6850
EN to PADM three_state_disable	TLZ	0.249000						
EN to PADM three_state_disable	THZ	0.278000						
EN to PADM three_state_enable	TZH	2.07700	2.53100	4.11000	7.02700	11.5000	17.7330	25.9060
EN to PADM three_state_enable	TZL	1.78800	2.11000	3.27000	5.37100	8.55700	12.9760	18.7500

Delay Characteristics: Time Units 1ns
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		7.56512	**10.6681**	**21.5601**	**42.3601**	**74.7661**	**120.235**	**180.065**
A to PADM	TPLH	3.32400	4.09200	6.62200	11.2830	18.4490	28.4380	41.5380
A to PADM	TPHL	2.76600	3.31000	5.00500	7.98800	12.5110	18.7830	26.9800
EN to PADM three_state_disable	TLZ	0.352000						
EN to PADM three_state_disable	THZ	0.449000						
EN to PADM three_state_enable	TZH	3.40000	4.13400	6.53800	10.9890	17.8470	27.4250	39.9940
EN to PADM three_state_enable	TZL	2.78000	3.30200	4.92700	7.80500	12.1690	18.2250	26.1470

Delay Characteristics: Time Units 1ns
Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		7.44931	10.5523	21.4443	42.2443	74.6503	120.119	179.949
A to PADM	TPLH	6.73800	8.00500	12.2550	20.1550	32.3520	49.3800	71.7170
A to PADM	TPHL	5.75000	6.64500	9.43100	14.2790	21.6250	31.8410	45.2130
EN to PADM three_state_disable	TLZ	0.648000						
EN to PADM three_state_disable	THZ	0.866000						
EN to PADM three_state_enable	TZH	6.90400	8.13800	12.2420	19.8880	31.7210	48.2670	69.9940
EN to PADM three_state_enable	TZL	5.77100	6.67000	9.36900	14.0910	21.2810	31.2850	44.3850

Test Data

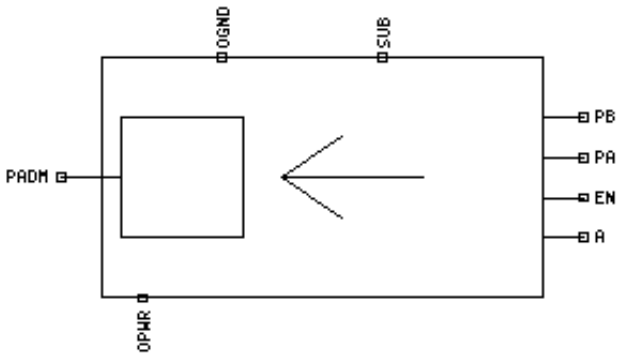
Parameter	Description	Minimum	Maximum	Units
ipu	Pull up current	-161.0	-40.0	uA
ipd	Pull down current	32.0	192.0	uA
ibkpu	Buskeeper pull-up current	-110.0	-28.0	uA
vtestbkpu	Test voltage for keeping the bus keeper pin high	(0.7*Vdd)	-	V
ibkpd	Buskeeper pull-down current	21.0	139.0	uA
vtestbkpd	Test voltage for keeping the bus keeper pin lob	-	(0.3*Vdd)	V
Iil	Low Level Input Current	-10.0	10.0	uA
Iih	High Level Input Current	-10.0	10.0	uA
Vdiode_vdd	Diode voltage range to Vdd	0.20	1.10	V
Vi_max	Maximum Voltage	-0.5	(1.10 * Vdd)	V
I_max	Maximum sink/source current	-100	100	mA
Vdiode_vss	Diode voltage to Vss	-1.10	-0.20	V
Voh	High Level Output Voltage	2.4	Vdd	V
Vol	Low Level Output Voltage	0.0	0.4	V
Iol	Low Level Output Current	2.0	-	mA
Ioh	High Level Output Current	-	-1.7	mA

obac3csxe04_mt

Description

"OBAC3CSXE04_MT is a[n] OBAC3CSXE04 is a 4X drive, non-inverting, CMOS-level, tri-state composite output buffer with a programmable pull-up/pull-down/bus-hold piece, active low enable and controlled slew rate output. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
PA	0.0381429 (pF)
A	0.0311867 (pF)
PB	0.03888 (pF)
EN	0.0343174 (pF)

AREA : 27735.0 sqr microns

Truth Table

A input	EN input	PA input	PB input	PADM output
L	L	?	?	L
L	H	?	?	Z
H	L	?	?	H
H	H	?	?	Z

IL = Illegal Z = High Impedence ? = Dont Care NC = No Change

Pull Cell Truth Table :

PA	PB	Function
0	0	Pull Down
0	1	Tristate
1	0	Bus Keeper

1	1	Pull Up

Power Characteristics:
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	607.444	uW

Power Characteristics:
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	282.664	uW

Power Characteristics:
Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	128.823	uW

Delay Characteristics: Time Units 1ns
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		7.64552	**10.7484**	**21.6405**	**42.4405**	**74.8465**	**120.316**	**180.146**
A to PADM	TPLH	1.91900	2.28200	3.33300	5.12700	7.83000	11.5670	16.4510
A to PADM	TPHL	1.73500	2.08600	3.09700	4.74300	7.15300	10.4650	14.7790
EN to PADM three_state_disable	TLZ	0.277000						
EN to PADM three_state_disable	THZ	0.321000						
EN to PADM three_state_enable	TZH	1.97400	2.28200	3.18300	4.71300	7.01500	10.2040	14.3690
EN to PADM three_state_enable	TZL	1.78300	2.07400	3.01700	4.55800	6.81000	9.90600	13.9400

Delay Characteristics: Time Units 1ns
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		7.46091	**10.5638**	**21.4559**	**42.2559**	**74.6619**	**120.131**	**179.961**
A to PADM	TPLH	3.16200	3.68700	5.22000	7.80300	11.6740	17.0340	24.0390
A to PADM	TPHL	2.88100	3.35800	4.74100	6.97300	10.2110	14.6510	20.4320
EN to PADM three_state_disable	TLZ	0.395000						
EN to PADM three_state_disable	THZ	0.514000						
EN to PADM three_state_enable	TZH	3.23300	3.72200	5.12000	7.47400	11.0080	15.9150	22.3340
EN to PADM three_state_enable	TZL	2.88500	3.34500	4.66500	6.80800	9.90600	14.1550	19.6900

Delay Characteristics: Time Units 1ns
Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		7.34149	10.4444	21.3365	42.1365	74.5425	120.011	179.841
A to PADM	TPLH	6.45800	7.34100	9.97000	14.3320	20.8020	29.7470	41.4430
A to PADM	TPHL	6.10200	6.90200	9.22300	12.9020	18.1550	25.3180	34.6460
EN to PADM three_state_disable	TLZ	0.714000						
EN to PADM three_state_disable	THZ	0.990000						
EN to PADM three_state_enable	TZH	6.61600	7.46400	9.93600	14.0190	20.0840	28.4920	39.5020
EN to PADM three_state_enable	TZL	6.10700	6.91400	9.16100	12.7320	17.8530	24.8380	33.9340

Test Data

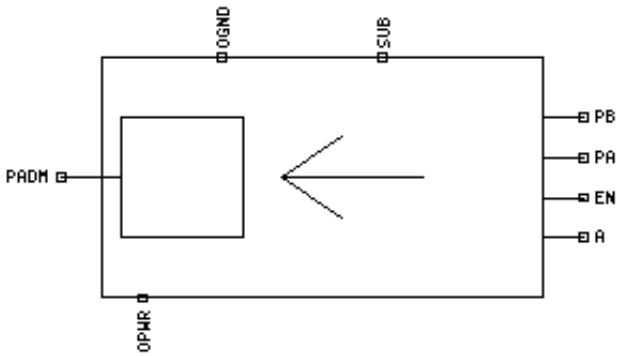
Parameter	Description	Minimum	Maximum	Units
ipu	Pull up current	-161.0	-40.0	uA
ipd	Pull down current	32.0	192.0	uA
ibkpu	Buskeeper pull-up current	-110.0	-28.0	uA
vtestbkpu	Test voltage for keeping the bus keeper pin high	(0.7*Vdd)	-	V
ibkpd	Buskeeper pull-down current	21.0	139.0	uA
vtestbkpd	Test voltage for keeping the bus keeper pin lob	-	(0.3*Vdd)	V
Iil	Low Level Input Current	-10.0	10.0	uA
Iih	High Level Input Current	-10.0	10.0	uA
Vdiode_vdd	Diode voltage range to Vdd	0.20	1.10	V
Vi_max	Maximum Voltage	-0.5	(1.10 * Vdd)	V
I_max	Maximum sink/source current	-100	100	mA
Vdiode_vss	Diode voltage to Vss	-1.10	-0.20	V
Voh	High Level Output Voltage	2.4	Vdd	V
Vol	Low Level Output Voltage	0.0	0.4	V
Iol	Low Level Output Current	3.12	-	mA
Ioh	High Level Output Current	-	-3.39	mA

obac3csxe08_mt

Description

"OBAC3CSXE08_MT is a[n] OBAC3CSXE08 is a 8X drive, non-inverting, CMOS-level, tri-state composite output buffer with a programmable pull-up/pull-down/bus-hold piece, active low enable and controlled slew rate output. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
PA	0.0381429 (pF)
A	0.0311867 (pF)
PB	0.03888 (pF)
EN	0.0343174 (pF)

AREA : 27735.0 sqr microns

Truth Table

A input	EN input	PA input	PB input	PADM output
L	L	?	?	L
L	H	?	?	Z
H	L	?	?	H
H	H	?	?	Z

IL = Illegal Z = High Impedence ? = Dont Care NC = No Change

Pull Cell Truth Table :

PA	PB	Function
0	0	Pull Down
0	1	Tristate
1	0	Bus Keeper

1	1	Pull Up

Power Characteristics:
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	607.448	uW

Power Characteristics:
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	282.664	uW

Power Characteristics:
Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	128.823	uW

Delay Characteristics: Time Units 1ns
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		7.64567	**10.7487**	**21.6407**	**42.4407**	**74.8467**	**120.316**	**180.146**
A to PADM	TPLH	2.16400	2.50000	3.36700	4.62000	6.31600	8.56600	11.4710
A to PADM	TPHL	2.18000	2.51200	3.38800	4.61600	6.17600	8.12900	10.5530
EN to PADM three_state_disable	TLZ	0.375000						
EN to PADM three_state_disable	THZ	0.402000						
EN to PADM three_state_enable	TZH	2.20600	2.49700	3.21500	4.20200	5.49200	7.18600	9.36300
EN to PADM three_state_enable	TZL	2.17900	2.48500	3.31000	4.44500	5.86200	7.61800	9.78800

Delay Characteristics: Time Units 1ns
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		7.46104	**10.5640**	**21.4560**	**42.2560**	**74.6620**	**120.131**	**179.961**
A to PADM	TPLH	3.52600	3.99500	5.22800	7.00400	9.36900	12.4660	16.4400
A to PADM	TPHL	3.72500	4.18500	5.41200	7.12400	9.26900	11.9180	15.1680
EN to PADM three_state_disable	TLZ	0.513000						
EN to PADM three_state_disable	THZ	0.643000						
EN to PADM three_state_enable	TZH	3.59600	4.02700	5.12300	6.66800	8.69000	11.3240	14.6970
EN to PADM three_state_enable	TZL	3.72300	4.16700	5.33600	6.97100	8.99500	11.4720	14.5000

Delay Characteristics: Time Units 1ns
Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		7.34164	10.4446	21.3366	42.1366	74.5426	120.012	179.842
A to PADM	TPLH	7.11300	7.89800	10.0370	13.1030	17.0880	22.1850	28.6320
A to PADM	TPHL	8.04900	8.86400	11.0280	13.9900	17.6070	21.9640	27.2060
EN to PADM three_state_disable	TLZ	0.916000						
EN to PADM three_state_disable	THZ	1.23100						
EN to PADM three_state_enable	TZH	7.26600	8.01500	9.99400	12.7770	16.3490	20.8960	26.6390
EN to PADM three_state_enable	TZL	8.03400	8.85700	10.9570	13.8290	17.3380	21.5440	26.5880

Test Data

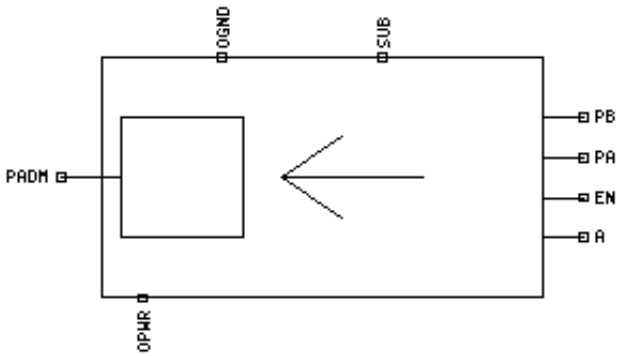
Parameter	Description	Minimum	Maximum	Units
ipu	Pull up current	-161.0	-40.0	uA
ipd	Pull down current	32.0	192.0	uA
ibkpu	Buskeeper pull-up current	-110.0	-28.0	uA
vtestbkpu	Test voltage for keeping the bus keeper pin high	(0.7*Vdd)	-	V
ibkpd	Buskeeper pull-down current	21.0	139.0	uA
vtestbkpd	Test voltage for keeping the bus keeper pin lob	-	(0.3*Vdd)	V
Iil	Low Level Input Current	-10.0	10.0	uA
Iih	High Level Input Current	-10.0	10.0	uA
Vdiode_vdd	Diode voltage range to Vdd	0.20	1.10	V
Vi_max	Maximum Voltage	-0.5	(1.10 * Vdd)	V
I_max	Maximum sink/source current	-100	100	mA
Vdiode_vss	Diode voltage to Vss	-1.10	-0.20	V
Voh	High Level Output Voltage	2.4	Vdd	V
Vol	Low Level Output Voltage	0.0	0.4	V
Iol	Low Level Output Current	6.25	-	mA
Ioh	High Level Output Current	-	-6.79	mA

obac3cxxe08_mt

Description

"OBAC3CXXE08_MT is a[n] OBAC3CXXE08 is an 8X drive, non-inverting, CMOS-level, tri-state composite output buffer with a programmable pull-up/pull-down/bus-hold piece and active low enable. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
PA	0.0381429 (pF)
A	0.0311849 (pF)
PB	0.03888 (pF)
EN	0.0343431 (pF)

AREA : 27735.0 sqr microns

Truth Table

A input	EN input	PA input	PB input	PADM output
L	L	?	?	L
L	H	?	?	Z
H	L	?	?	H
H	H	?	?	Z

IL = Illegal Z = High Impedence ? = Dont Care NC = No Change

Pull Cell Truth Table :

PA	PB	Function
0	0	Pull Down
0	1	Tristate
1	0	Bus Keeper

1	1	Pull Up

Power Characteristics:
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	607.448	uW

Power Characteristics:
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	282.664	uW

Power Characteristics:
Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	128.823	uW

Delay Characteristics: Time Units 1ns
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		7.64567	**10.7487**	**21.6407**	**42.4407**	**74.8467**	**120.316**	**180.146**
A to PADM	TPLH	0.592000	0.779000	1.38100	2.46000	4.08600	6.31900	9.22100
A to PADM	TPHL	0.564000	0.720000	1.23200	2.13100	3.46700	5.29100	7.65100
EN to PADM three_state_disable	TLZ	0.399000						
EN to PADM three_state_disable	THZ	0.418000						
EN to PADM three_state_enable	TZH	1.06600	1.03700	1.21500	2.02800	3.24600	4.92000	7.09500
EN to PADM three_state_enable	TZL	1.05900	1.02800	1.16000	1.96900	3.16100	4.78700	6.88800

Delay Characteristics: Time Units 1ns
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		7.46104	**10.5640**	**21.4560**	**42.2560**	**74.6620**	**120.131**	**179.961**
A to PADM	TPLH	0.923000	1.17500	2.00500	3.48400	5.70200	8.74800	12.7110
A to PADM	TPHL	0.895000	1.09100	1.75200	2.93400	4.69900	7.11300	10.2390
EN to PADM three_state_disable	TLZ	0.560000						
EN to PADM three_state_disable	THZ	0.672000						
EN to PADM three_state_enable	TZH	1.19100	1.26000	1.88700	3.13000	5.00000	7.58000	10.9390
EN to PADM three_state_enable	TZL	1.15300	1.19500	1.68100	2.78600	4.42900	6.67400	9.58000

Delay Characteristics: Time Units 1ns
Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		7.34164	10.4446	21.3366	42.1366	74.5426	120.012	179.842
A to PADM	TPLH	1.84800	2.22800	3.52400	5.86900	9.42100	14.3190	20.6950
A to PADM	TPHL	1.81300	2.10900	3.11900	4.93500	7.67400	11.4450	16.3400
EN to PADM three_state_disable	TLZ	0.997000						
EN to PADM three_state_disable	THZ	1.28400						
EN to PADM three_state_enable	TZH	1.98500	2.33200	3.46600	5.51900	8.64900	12.9880	18.6530
EN to PADM three_state_enable	TZL	1.82200	2.12200	3.06000	4.77600	7.40200	11.0200	15.7190

Test Data

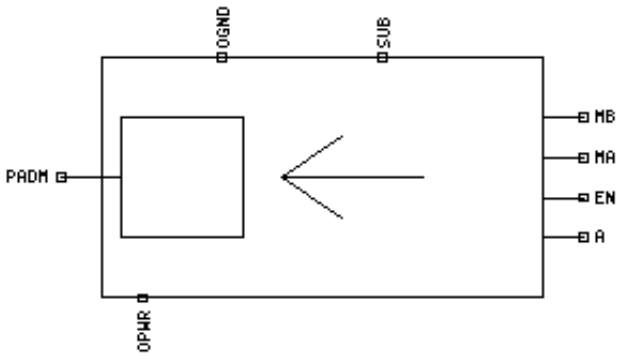
Parameter	Description	Minimum	Maximum	Units
ipu	Pull up current	-161.0	-40.0	uA
ipd	Pull down current	32.0	192.0	uA
ibkpu	Buskeeper pull-up current	-110.0	-28.0	uA
vtestbkpu	Test voltage for keeping the bus keeper pin high	(0.7*Vdd)	-	V
ibkpd	Buskeeper pull-down current	21.0	139.0	uA
vtestbkpd	Test voltage for keeping the bus keeper pin lob	-	(0.3*Vdd)	V
Iil	Low Level Input Current	-10.0	10.0	uA
Iih	High Level Input Current	-10.0	10.0	uA
Vdiode_vdd	Diode voltage range to Vdd	0.20	1.10	V
Vi_max	Maximum Voltage	-0.5	(1.10 * Vdd)	V
I_max	Maximum sink/source current	-100	100	mA
Vdiode_vss	Diode voltage to Vss	-1.10	-0.20	V
Voh	High Level Output Voltage	2.4	Vdd	V
Vol	Low Level Output Voltage	0.0	0.4	V
Iol	Low Level Output Current	6.25	-	mA
Ioh	High Level Output Current	-	-6.79	mA

obaptcxte08_mt

Description

"OBAPTCXTE08_MT is a[n] OBAPTCXTE08 is an 8X drive, 5V-tolerant, non-inverting, CMOS-level, tri-state composite output buffer with a programmable pull-up/pull-down/bus-hold piece and a active low enable. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
A	0.0316517 (pF)
MA	0.0297544 (pF)
MB	0.0409256 (pF)
EN	0.0620153 (pF)

AREA : 27735.0 sqr microns

Truth Table

A input	EN input	MA input	MB input	PADM output
L	L	?	?	L
L	H	?	?	Z
H	L	?	?	H
H	H	?	?	Z

IL = Illegal Z = High Impedence ? = Dont Care NC = No Change

Pull Cell Truth Table :

MA	MB	Function
0	0	Pull Down
0	1	Tristate
1	0	Tristate

1	1	Pull Up

Power Characteristics:
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	601.898	uW

Power Characteristics:
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	270.507	uW

Power Characteristics:
Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	116.109	uW

Delay Characteristics: Time Units 1ns
Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		8.31987	**11.4229**	**22.3149**	**43.1149**	**75.5209**	**120.990**	**180.820**
A to PADM	TPLH	0.748000	0.930000	1.52400	2.60200	4.23300	6.47800	9.39100
A to PADM	TPHL	0.569000	0.701000	1.12300	1.84700	2.91500	4.36500	6.23400
EN to PADM three_state_disable	TLZ	0.614000						
EN to PADM three_state_disable	THZ	0.580000						
EN to PADM three_state_enable	TZH	1.10000	1.08700	1.44100	2.31000	3.58600	5.31500	7.54700
EN to PADM three_state_enable	TZL	1.01100	0.957000	1.04900	1.68700	2.61200	3.86100	5.46600

Delay Characteristics: Time Units 1ns
Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		8.03731	**11.1403**	**22.0323**	**42.8323**	**75.2383**	**120.707**	**180.537**
A to PADM	TPLH	1.14600	1.39900	2.23000	3.71700	5.94900	9.01500	12.9960
A to PADM	TPHL	0.922000	1.09400	1.66400	2.66000	4.14100	6.15900	8.76900
EN to PADM three_state_disable	TLZ	0.849000						
EN to PADM three_state_disable	THZ	0.928000						
EN to PADM three_state_enable	TZH	1.32600	1.48800	2.23500	3.54700	5.49400	8.14800	11.5840
EN to PADM three_state_enable	TZL	1.10600	1.13500	1.58100	2.51100	3.87500	5.72600	8.11500

Delay Characteristics: Time Units 1ns
Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		7.87998	10.9830	21.8750	42.6750	75.0810	120.550	180.380
A to PADM	TPLH	2.30600	2.69300	4.01200	6.38700	9.97700	14.9140	21.3260
A to PADM	TPHL	1.94000	2.22100	3.16200	4.82900	7.33400	10.7820	15.2560
EN to PADM three_state_disable	TLZ	1.53500						
EN to PADM three_state_disable	THZ	1.85500						
EN to PADM three_state_enable	TZH	2.63200	2.98100	4.18700	6.35300	9.60500	14.0710	19.8610
EN to PADM three_state_enable	TZL	1.89200	2.18000	3.06600	4.65200	7.05600	10.3590	14.6410

Test Data

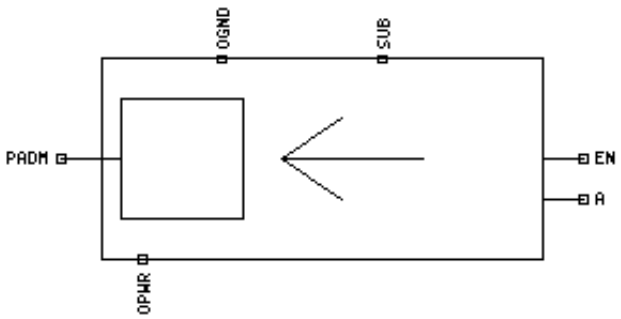
Parameter	Description	Minimum	Maximum	Units
ipu	Pull up current	-155.0	-36.0	uA
ipd	Pull down current	28.0	191.0	uA
Iil	Low Level Input Current	-10.0	10.0	uA
Iih	High Level Input Current	-10.0	10.0	uA
Vi_max	Maximum Voltage	-0.5	5.0	V
I_max	Maximum sink/source current	-100	100	mA
Vdiode_vss	Diode voltage to Vss	-1.10	-0.20	V
Voh	High Level Output Voltage	2.4	Vdd	V
Vol	Low Level Output Voltage	0.0	0.4	V
Iol	Low Level Output Current	6.47	-	mA
Ioh	High Level Output Current	-	-6.76	mA

obaxxcste02_mt

Description

"OBAXXCSTE02_MT is a[n] OBAXXCSTE02 is an 2X drive, 5V-tolerant, non-inverting, CMOS-level, tri-state composite output buffer with active low enable and controlled slew rate output. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
A	0.0314855 (pF)
EN	0.0613419 (pF)

AREA : 27735.0 sqr microns

Truth Table

A input	EN input	PADM output
L	L	L
L	H	Z
H	L	H
H	H	Z

IL = Illegal Z = High Impedence ? = Dont Care NC = No Change

Power Characteristics:

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	0.000109332	uW

Power Characteristics:

Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	0.000150766	uW

Power Characteristics:

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	0.0869726	uW

Delay Characteristics: Time Units 1ns

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		7.65647	**10.7595**	**21.6515**	**42.4515**	**74.8575**	**120.326**	**180.156**
A to PADM	TPLH	2.70800	3.25500	5.01400	8.20300	13.0800	19.8690	28.7660
A to PADM	TPHL	1.68200	2.07500	3.34200	5.60700	9.04500	13.8120	20.0460
EN to PADM three_state_disable	TLZ	0.302000						
EN to PADM three_state_disable	THZ	0.413000						
EN to PADM three_state_enable	TZH	2.80300	3.31200	4.95900	7.92400	12.4390	18.7090	26.9200
EN to PADM three_state_enable	TZL	1.77000	2.09000	3.28300	5.44900	8.73400	13.2870	19.2410

Delay Characteristics: Time Units 1ns

Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		7.66239	**10.7654**	**21.6574**	**42.4574**	**74.8634**	**120.332**	**180.162**
A to PADM	TPLH	4.50800	5.31400	7.90300	12.6070	19.8220	29.8760	43.0560
A to PADM	TPHL	2.76300	3.31700	5.12500	8.37500	13.3270	20.2060	29.2060
EN to PADM three_state_disable	TLZ	0.430000						
EN to PADM three_state_disable	THZ	0.664000						
EN to PADM three_state_enable	TZH	4.67500	5.44100	7.93200	12.4530	19.3790	29.0210	41.6530
EN to PADM three_state_enable	TZL	2.79000	3.32900	5.07500	8.24600	13.0720	19.7750	28.5480

Delay Characteristics: Time Units 1ns

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		7.73491	**10.8379**	**21.7299**	**42.5299**	**74.9359**	**120.405**	**180.235**
A to PADM	TPLH	9.22800	10.6080	15.0510	23.0640	35.3480	52.4780	74.9380
A to PADM	TPHL	5.85100	6.85600	10.1410	16.0450	25.0600	37.6210	54.0840
EN to PADM three_state_disable	TLZ	0.785000						
	THZ	1.32100						

EN to PADM three_state_disable								
EN to PADM three_state_enable	TZH	9.60100	10.9330	15.2530	23.0520	34.9990	51.6570	73.4960
EN to PADM three_state_enable	TZL	5.90700	6.91600	10.1200	15.9230	24.8260	37.2360	53.5010

Test Data

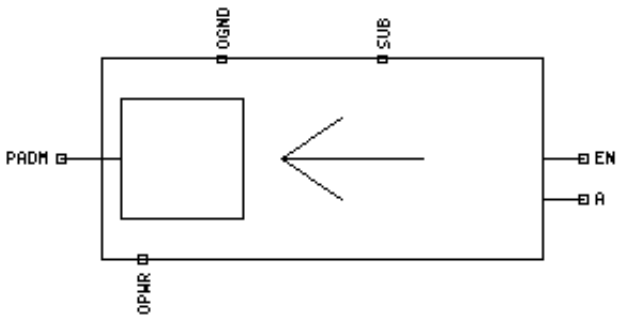
Parameter	Description	Minimum	Maximum	Units
Iil	Low Level Input Current	-10.0	10.0	uA
Iih	High Level Input Current	-10.0	10.0	uA
Vi_max	Maximum Voltage	-0.5	5.0	V
I_max	Maximum sink/source current	-100	100	mA
Vdiode_vss	Diode voltage to Vss	-1.10	-0.20	V
Voh	High Level Output Voltage	2.4	Vdd	V
Vol	Low Level Output Voltage	0.0	0.4	V
Iol	Low Level Output Current	1.62	-	mA
Ioh	High Level Output Current	-	-1.69	mA

obaxxcsxe02_mt

Description

"OBAXXCSXE02_MT is a[n] OBAXXCSXE02 is a 2X drive, non-inverting, CMOS-level, tri-state composite output buffer with active low enable and controlled slew rate output. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
A	0.0310208 (pF)
EN	0.0343174 (pF)

AREA : 27735.0 sqr microns

Truth Table

A input	EN input	PADM output
L	L	L
L	H	Z
H	L	H
H	H	Z

IL = Illegal Z = High Impedence ? = Dont Care NC = No Change

Power Characteristics:

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	7.03425e-05	uW

Power Characteristics:

Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	0.000170794	uW

Power Characteristics:

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	0.0895054	uW

Delay Characteristics: Time Units 1ns

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		7.01377	**10.1168**	**21.0088**	**41.8088**	**74.2148**	**119.684**	**179.514**
A to PADM	TPLH	1.96900	2.49500	4.22500	7.39200	12.2410	18.9910	27.8390
A to PADM	TPHL	1.67900	2.08400	3.34200	5.55900	8.92000	13.5790	19.6700
EN to PADM three_state_disable	TLZ	0.249000						
EN to PADM three_state_disable	THZ	0.278000						
EN to PADM three_state_enable	TZH	2.04600	2.49600	4.06500	6.96100	11.4020	17.5900	25.7060
EN to PADM three_state_enable	TZL	1.78200	2.10900	3.28300	5.40800	8.63400	13.1080	18.9570

Delay Characteristics: Time Units 1ns

Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		7.08515	**10.1882**	**21.0802**	**41.8802**	**74.2862**	**119.755**	**179.585**
A to PADM	TPLH	3.29100	4.05900	6.58700	11.2470	18.4120	28.4010	41.5000
A to PADM	TPHL	2.74400	3.29000	4.98700	7.96800	12.4910	18.7620	26.9610
EN to PADM three_state_disable	TLZ	0.352000						
EN to PADM three_state_disable	THZ	0.449000						
EN to PADM three_state_enable	TZH	3.35300	4.08300	6.47500	10.8970	17.7150	27.2360	39.7310
EN to PADM three_state_enable	TZL	2.77400	3.30100	4.94000	7.84100	12.2420	18.3510	26.3430

Delay Characteristics: Time Units 1ns

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		7.13894	**10.2419**	**21.1339**	**41.9339**	**74.3399**	**119.809**	**179.639**
A to PADM	TPLH	6.66700	7.93700	12.1880	20.0880	32.2850	49.3120	71.6500
A to PADM	TPHL	5.70500	6.60500	9.39600	14.2450	21.5900	31.8060	45.1800
EN to PADM three_state_disable	TLZ	0.648000						
	THZ	0.866000						

EN to PADM three_state_disable								
EN to PADM three_state_enable	TZH	6.81200	8.04500	12.1350	19.7460	31.5240	47.9930	69.6190
EN to PADM three_state_enable	TZL	5.76000	6.66600	9.38300	14.1320	21.3650	31.4310	44.6110

Test Data

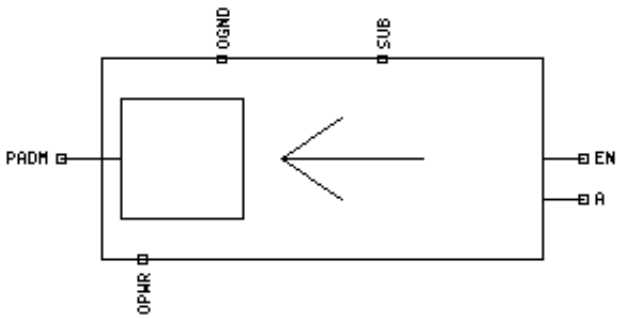
Parameter	Description	Minimum	Maximum	Units
Iil	Low Level Input Current	-10.0	10.0	uA
Iih	High Level Input Current	-10.0	10.0	uA
Vdiode_vdd	Diode voltage range to Vdd	0.20	1.10	V
Vi_max	Maximum Voltage	-0.5	(1.10 * Vdd)	V
I_max	Maximum sink/source current	-100	100	mA
Vdiode_vss	Diode voltage to Vss	-1.10	-0.20	V
Voh	High Level Output Voltage	2.4	Vdd	V
Vol	Low Level Output Voltage	0.0	0.4	V
Iol	Low Level Output Current	2.0	-	mA
Ioh	High Level Output Current	-	-1.7	mA

obaxxcsxe04_mt

Description

"OBAXXCSXE04_MT is a[n] OBAXXCSXE04 is a 4X drive, non-inverting, CMOS-level, tri-state composite output buffer with active low enable and controlled slew rate output. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
A	0.0310208 (pF)
EN	0.0343174 (pF)

AREA : 27735.0 sqr microns

Truth Table

A input	EN input	PADM output
L	L	L
L	H	Z
H	L	H
H	H	Z

IL = Illegal Z = High Impedence ? = Dont Care NC = No Change

Power Characteristics:

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	7.01839e-05	uW

Power Characteristics:

Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	0.000165649	uW

Power Characteristics:

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	0.0889735	uW

Delay Characteristics: Time Units 1ns

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		6.91292	**10.0158**	**20.9079**	**41.7079**	**74.1139**	**119.583**	**179.413**
A to PADM	TPLH	1.90500	2.26900	3.32200	5.11600	7.81800	11.5550	16.4380
A to PADM	TPHL	1.72100	2.07300	3.08700	4.73200	7.14300	10.4540	14.7700
EN to PADM three_state_disable	TLZ	0.277000						
EN to PADM three_state_disable	THZ	0.321000						
EN to PADM three_state_enable	TZH	1.95400	2.26400	3.16600	4.69000	6.98500	10.1610	14.3130
EN to PADM three_state_enable	TZL	1.77800	2.07300	3.02500	4.58000	6.85300	9.97900	14.0530

Delay Characteristics: Time Units 1ns

Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		6.98094	**10.0838**	**20.9759**	**41.7759**	**74.1819**	**119.651**	**179.481**
A to PADM	TPLH	3.14100	3.66800	5.20300	7.78500	11.6550	17.0150	24.0190
A to PADM	TPHL	2.86200	3.34100	4.72700	6.95900	10.1980	14.6370	20.4190
EN to PADM three_state_disable	TLZ	0.395000						
EN to PADM three_state_disable	THZ	0.513000						
EN to PADM three_state_enable	TZH	3.20400	3.69500	5.09400	7.44100	10.9660	15.8570	22.2590
EN to PADM three_state_enable	TZL	2.88000	3.34400	4.67400	6.82900	9.94800	14.2230	19.7960

Delay Characteristics: Time Units 1ns

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		7.03109	**10.1340**	**21.0261**	**41.8261**	**74.2321**	**119.701**	**179.531**
A to PADM	TPLH	6.40800	7.29800	9.93300	14.2980	20.7670	29.7130	41.4080
A to PADM	TPHL	6.06000	6.86700	9.19600	12.8770	18.1320	25.2940	34.6230
EN to PADM three_state_disable	TLZ	0.714000						
	THZ	0.990000						

EN to PADM three_state_disable								
EN to PADM three_state_enable	TZH	6.55400	7.40800	9.88500	13.9620	20.0150	28.4040	39.3900
EN to PADM three_state_enable	TZL	6.09700	6.91100	9.17100	12.7560	17.9010	24.9150	34.0540

Test Data

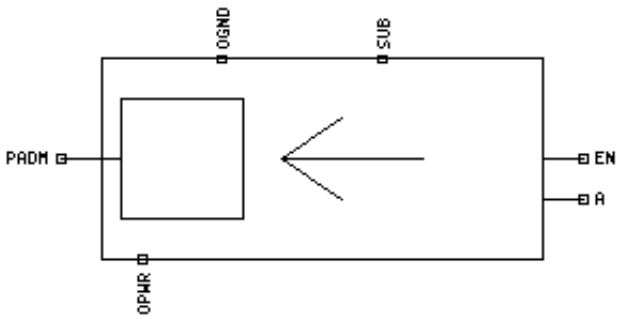
Parameter	Description	Minimum	Maximum	Units
Iil	Low Level Input Current	-10.0	10.0	uA
Iih	High Level Input Current	-10.0	10.0	uA
Vdiode_vdd	Diode voltage range to Vdd	0.20	1.10	V
Vi_max	Maximum Voltage	-0.5	(1.10 * Vdd)	V
I_max	Maximum sink/source current	-100	100	mA
Vdiode_vss	Diode voltage to Vss	-1.10	-0.20	V
Voh	High Level Output Voltage	2.4	Vdd	V
Vol	Low Level Output Voltage	0.0	0.4	V
Iol	Low Level Output Current	3.12	-	mA
Ioh	High Level Output Current	-	-3.39	mA

obaxxcsxe08_mt

Description

"OBAXXCSXE08_MT is a[n] OBAXXCSXE08 is a 8X drive, non-inverting, CMOS-level, tri-state composite output buffer with active low enable and controlled slew rate output. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
A	0.0310208 (pF)
EN	0.0343174 (pF)

AREA : 27735.0 sqr microns

Truth Table

A input	EN input	PADM output
L	L	L
L	H	Z
H	L	H
H	H	Z

IL = Illegal Z = High Impedence ? = Dont Care NC = No Change

Power Characteristics:

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	7.0153e-05	uW

Power Characteristics:

Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	0.000165627	uW

Power Characteristics:

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	0.0889732	uW

Delay Characteristics: Time Units 1ns

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		6.91307	**10.0160**	**20.9081**	**41.7081**	**74.1141**	**119.583**	**179.413**
A to PADM	TPLH	2.15000	2.48900	3.35900	4.61400	6.31000	8.56000	11.4640
A to PADM	TPHL	2.16600	2.50100	3.38100	4.60900	6.17100	8.12400	10.5480
EN to PADM three_state_disable	TLZ	0.375000						
EN to PADM three_state_disable	THZ	0.402000						
EN to PADM three_state_enable	TZH	2.18700	2.48100	3.20400	4.19100	5.48100	7.17100	9.34600
EN to PADM three_state_enable	TZL	2.17600	2.48500	3.31700	4.45800	5.88400	7.64900	9.83300

Delay Characteristics: Time Units 1ns

Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		6.98108	**10.0840**	**20.9761**	**41.7761**	**74.1821**	**119.651**	**179.481**
A to PADM	TPLH	3.50700	3.97900	5.21600	6.99500	9.36000	12.4570	16.4290
A to PADM	TPHL	3.70500	4.16900	5.40100	7.11500	9.26200	11.9100	15.1620
EN to PADM three_state_disable	TLZ	0.513000						
EN to PADM three_state_disable	THZ	0.643000						
EN to PADM three_state_enable	TZH	3.56900	4.00500	5.10600	6.65100	8.67300	11.3030	14.6730
EN to PADM three_state_enable	TZL	3.72200	4.16900	5.34500	6.98500	9.01700	11.5020	14.5430

Delay Characteristics: Time Units 1ns

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		7.03120	**10.1341**	**21.0262**	**41.8262**	**74.2322**	**119.701**	**179.531**
A to PADM	TPLH	7.06900	7.86200	10.0110	13.0820	17.0690	22.1670	28.6130
A to PADM	TPHL	8.00600	8.82800	11.0040	13.9720	17.5930	21.9510	27.1950
EN to PADM three_state_disable	TLZ	0.916000						
	THZ	1.23100						

EN to PADM three_state_disable								
EN to PADM three_state_enable	TZH	7.21100	7.96700	9.95900	12.7450	16.3180	20.8610	26.5990
EN to PADM three_state_enable	TZL	8.03200	8.86100	10.9700	13.8480	17.3660	21.5800	26.6380

Test Data

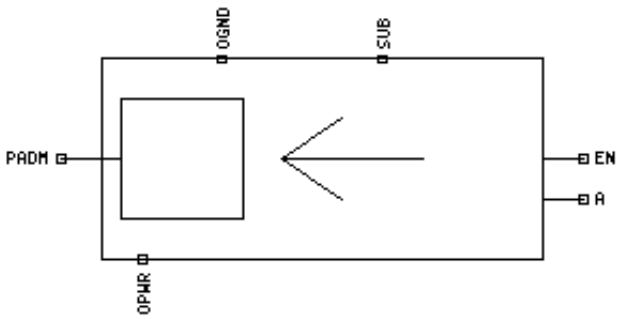
Parameter	Description	Minimum	Maximum	Units
Iil	Low Level Input Current	-10.0	10.0	uA
Iih	High Level Input Current	-10.0	10.0	uA
Vdiode_vdd	Diode voltage range to Vdd	0.20	1.10	V
Vi_max	Maximum Voltage	-0.5	(1.10 * Vdd)	V
I_max	Maximum sink/source current	-100	100	mA
Vdiode_vss	Diode voltage to Vss	-1.10	-0.20	V
Voh	High Level Output Voltage	2.4	Vdd	V
Vol	Low Level Output Voltage	0.0	0.4	V
Iol	Low Level Output Current	6.25	-	mA
Ioh	High Level Output Current	-	-6.79	mA

obaxxcxte02_mt

Description

"OBAXXCXTE02_MT is a[n] OBAXXCXTE02 is an 2X drive, 5V-tolerant, non-inverting, CMOS-level, tri-state composite output buffer with active low enable. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
A	0.0314833 (pF)
EN	0.0613263 (pF)

AREA : 27735.0 sqr microns

Truth Table

A input	EN input	PADM output
L	L	L
L	H	Z
H	L	H
H	H	Z

IL = Illegal Z = High Impedence ? = Dont Care NC = No Change

Power Characteristics:

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	0.000117582	uW

Power Characteristics:

Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	0.000154978	uW

Power Characteristics:

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	0.0870341	uW

Delay Characteristics: Time Units 1ns

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		7.65666	**10.7597**	**21.6517**	**42.4517**	**74.8577**	**120.327**	**180.157**
A to PADM	TPLH	1.26000	1.79100	3.54400	6.73600	11.6140	18.4030	27.2980
A to PADM	TPHL	0.875000	1.24300	2.48600	4.74500	8.18000	12.9430	19.1700
EN to PADM three_state_disable	TLZ	0.333000						
EN to PADM three_state_disable	THZ	0.425000						
EN to PADM three_state_enable	TZH	1.82200	2.13200	3.48100	6.44600	10.9630	17.2390	25.4540
EN to PADM three_state_enable	TZL	1.47400	1.65700	2.42200	4.58500	7.86700	12.4150	18.3580

Delay Characteristics: Time Units 1ns

Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		7.66239	**10.7654**	**21.6574**	**42.4574**	**74.8634**	**120.332**	**180.162**
A to PADM	TPLH	2.05700	2.82200	5.37900	10.0830	17.3000	27.3580	40.5410
A to PADM	TPHL	1.36500	1.87600	3.63100	6.86600	11.8150	18.6900	27.6860
EN to PADM three_state_disable	TLZ	0.471000						
EN to PADM three_state_disable	THZ	0.685000						
EN to PADM three_state_enable	TZH	2.42400	2.98800	5.39800	9.91400	16.8400	26.4830	39.1180
EN to PADM three_state_enable	TZL	1.78000	2.11300	3.56800	6.72800	11.5560	18.2580	27.0270

Delay Characteristics: Time Units 1ns

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		7.73491	**10.8379**	**21.7299**	**42.5299**	**74.9359**	**120.405**	**180.235**
A to PADM	TPLH	3.97800	5.21300	9.49500	17.4770	29.7640	46.8980	69.3630
A to PADM	TPHL	2.78200	3.66500	6.78000	12.6270	21.6360	34.1950	50.6520
EN to PADM three_state_disable	TLZ	0.878000						
	THZ	1.36200						

EN to PADM three_state_disable								
EN to PADM three_state_enable	TZH	4.34100	5.52800	9.68200	17.4440	29.3860	46.0420	67.8810
EN to PADM three_state_enable	TZL	2.81500	3.69100	6.72900	12.4810	21.3820	33.7950	50.0610

Test Data

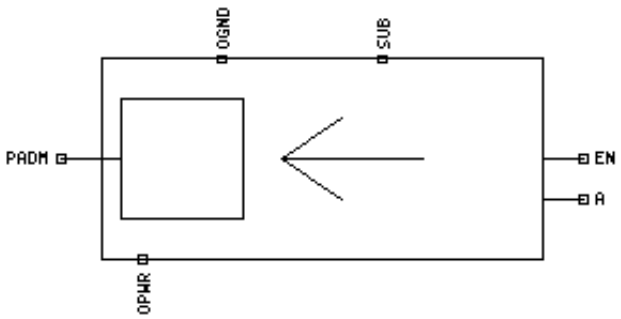
Parameter	Description	Minimum	Maximum	Units
Iil	Low Level Input Current	-10.0	10.0	uA
Iih	High Level Input Current	-10.0	10.0	uA
Vi_max	Maximum Voltage	-0.5	5.0	V
I_max	Maximum sink/source current	-100	100	mA
Vdiode_vss	Diode voltage to Vss	-1.10	-0.20	V
Voh	High Level Output Voltage	2.4	Vdd	V
Vol	Low Level Output Voltage	0.0	0.4	V
Iol	Low Level Output Current	1.62	-	mA
Ioh	High Level Output Current	-	-1.69	mA

obaxxvxxe02_mt

Description

"OBAXXVXXE02_MT is a[n] OBAXXVXXE02 is an 2X drive, non-inverting, LVTTL-level, composite output buffer. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
A	0.0310205 (pF)
EN	0.0343171 (pF)

AREA : 27735.0 sqr microns

Truth Table

A input	EN input	PADM output
L	L	L
L	H	Z
H	L	H
H	H	Z

IL = Illegal Z = High Impedence ? = Dont Care NC = No Change

Power Characteristics:

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	7.85975e-05	uW

Power Characteristics:

Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	0.000175027	uW

Power Characteristics:

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	0.0895612	uW

Delay Characteristics: Time Units 1ns

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		7.01377	**10.1168**	**21.0088**	**41.8088**	**74.2148**	**119.684**	**179.514**
A to PADM	TPLH	1.08300	1.60400	3.33600	6.50500	11.3550	18.1040	26.9480
A to PADM	TPHL	0.827000	1.18500	2.39400	4.59900	7.95500	12.6090	18.6930
EN to PADM three_state_disable	TLZ	0.281000						
EN to PADM three_state_disable	THZ	0.293000						
EN to PADM three_state_enable	TZH	1.70000	2.00100	3.16900	6.06500	10.5070	16.6970	24.8130
EN to PADM three_state_enable	TZL	1.42900	1.59900	2.33100	4.44700	7.66900	12.1350	17.9730

Delay Characteristics: Time Units 1ns

Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		7.08515	**10.1882**	**21.0802**	**41.8802**	**74.2862**	**119.755**	**179.585**
A to PADM	TPLH	1.77800	2.53400	5.05900	9.72000	16.8880	26.8800	39.9820
A to PADM	TPHL	1.25300	1.71900	3.32300	6.27700	10.7900	17.0550	25.2490
EN to PADM three_state_disable	TLZ	0.398000						
EN to PADM three_state_disable	THZ	0.470000						
EN to PADM three_state_enable	TZH	2.24200	2.77500	4.93800	9.35800	16.1760	25.6970	38.1930
EN to PADM three_state_enable	TZL	1.66700	1.95400	3.26300	6.14200	10.5400	16.6450	24.6310

Delay Characteristics: Time Units 1ns

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		7.13894	**10.2419**	**21.1339**	**41.9339**	**74.3399**	**119.809**	**179.639**
A to PADM	TPLH	3.43800	4.64200	8.84200	16.7370	28.9380	45.9700	68.3130
A to PADM	TPHL	2.42800	3.14600	5.68100	10.4350	17.7590	27.9620	41.3230
EN to PADM three_state_disable	TLZ	0.737000						
	THZ	0.907000						

EN to PADM three_state_disable								
EN to PADM three_state_enable	TZH	3.57300	4.74100	8.77600	16.3760	28.1510	44.6190	66.2450
EN to PADM three_state_enable	TZL	2.48400	3.18300	5.64100	10.2980	17.5140	27.5730	40.7500

Test Data

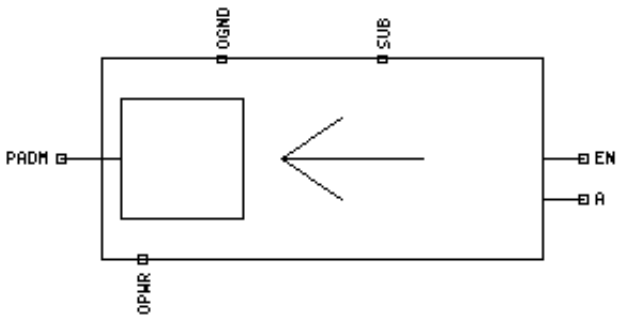
Parameter	Description	Minimum	Maximum	Units
Iil	Low Level Input Current	-10.0	10.0	uA
Iih	High Level Input Current	-10.0	10.0	uA
Vdiode_vdd	Diode voltage range to Vdd	0.20	1.10	V
Vi_max	Maximum Voltage	-0.5	(1.10 * Vdd)	V
I_max	Maximum sink/source current	-100	100	mA
Vdiode_vss	Diode voltage to Vss	-1.10	-0.20	V
Voh	High Level Output Voltage	2.4	Vdd	V
Vol	Low Level Output Voltage	0.0	0.4	V
Iol	Low Level Output Current	2.0	-	mA
Ioh	High Level Output Current	-	-1.7	mA

obaxxvxxe08_mt

Description

"OBAXXVXXE08_MT is a[n] OBAXXVXXE08 is an 8X drive, non-inverting, LVTTL-level, composite output buffer. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
A	0.0310193 (pF)
EN	0.0343431 (pF)

AREA : 27735.0 sqr microns

Truth Table

A input	EN input	PADM output
L	L	L
L	H	Z
H	L	H
H	H	Z

IL = Illegal Z = High Impedence ? = Dont Care NC = No Change

Power Characteristics:

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	7.84276e-05	uW

Power Characteristics:

Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	0.000169881	uW

Power Characteristics:

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	0.0890293	uW

Delay Characteristics: Time Units 1ns

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Delay p1 to p2	Parameter	Load (pF)						
		6.91307	**10.0160**	**20.9081**	**41.7081**	**74.1141**	**119.583**	**179.413**
A to PADM	TPLH	0.589000	0.775000	1.37600	2.45500	4.08100	6.31300	9.21400
A to PADM	TPHL	0.560000	0.716000	1.22800	2.12600	3.46200	5.28600	7.64700
EN to PADM three_state_disable	TLZ	0.399000						
EN to PADM three_state_disable	THZ	0.418000						
EN to PADM three_state_enable	TZH	1.06200	1.03200	1.20900	2.01900	3.23600	4.90700	7.07900
EN to PADM three_state_enable	TZL	1.05500	1.02500	1.15900	1.97100	3.17300	4.80800	6.92400

Delay Characteristics: Time Units 1ns

Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Delay p1 to p2	Parameter	Load (pF)						
		6.98108	**10.0840**	**20.9761**	**41.7761**	**74.1821**	**119.651**	**179.481**
A to PADM	TPLH	0.917000	1.17000	1.99800	3.47700	5.69400	8.74000	12.7010
A to PADM	TPHL	0.889000	1.08500	1.74700	2.92800	4.69300	7.10600	10.2330
EN to PADM three_state_disable	TLZ	0.560000						
EN to PADM three_state_disable	THZ	0.672000						
EN to PADM three_state_enable	TZH	1.18400	1.25200	1.87900	3.11900	4.98700	7.56100	10.9160
EN to PADM three_state_enable	TZL	1.14800	1.19000	1.67900	2.78700	4.43800	6.69100	9.61100

Delay Characteristics: Time Units 1ns

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Delay p1 to p2	Parameter	Load (pF)						
		7.03120	**10.1341**	**21.0262**	**41.8262**	**74.2322**	**119.701**	**179.531**
A to PADM	TPLH	1.83300	2.21300	3.50900	5.85400	9.40600	14.3030	20.6790
A to PADM	TPHL	1.80100	2.09700	3.10800	4.92300	7.66200	11.4330	16.3290
EN to PADM three_state_disable	TLZ	0.997000						
	THZ	1.28400						

EN to PADM three_state_disable								
EN to PADM three_state_enable	TZH	1.96800	2.31500	3.44800	5.49800	8.62500	12.9580	18.6180
EN to PADM three_state_enable	TZL	1.81200	2.11300	3.05400	4.77400	7.40700	11.0350	15.7470

Test Data

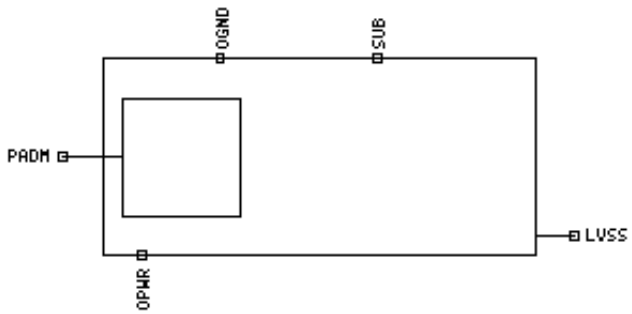
Parameter	Description	Minimum	Maximum	Units
Iil	Low Level Input Current	-10.0	10.0	uA
Iih	High Level Input Current	-10.0	10.0	uA
Vdiode_vdd	Diode voltage range to Vdd	0.20	1.10	V
Vi_max	Maximum Voltage	-0.5	(1.10 * Vdd)	V
I_max	Maximum sink/source current	-100	100	mA
Vdiode_vss	Diode voltage to Vss	-1.10	-0.20	V
Voh	High Level Output Voltage	2.4	Vdd	V
Vol	Low Level Output Voltage	0.0	0.4	V
Iol	Low Level Output Current	6.25	-	mA
Ioh	High Level Output Current	-	-6.79	mA

zgppxbg_mt

Description

"ZGPPXBG_MT is a[n] ZGPPXBG is a[n] VSS ground pad driving core ground and OGND bus with grounded gate NMOS protection. All supplies should be 3.6V or less. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
PADM	0 (pF)

AREA : 27735.0 sqr microns

Power Characteristics:

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	3.52219e-05	uW

Power Characteristics:

Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	0.000375514	uW

Power Characteristics:

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	0.100287	uW

Test Data

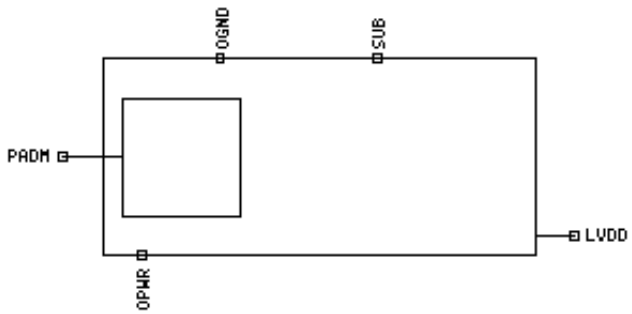
Parameter	Description	Minimum	Maximum	Units
Vi_max	Maximum Voltage	-100	100	V
I_max	Maximum sink/source current	-2	2	A

zgppxbp_mt

Description

"ZGPPXBP_MT is a[n] ZGPPXBP is a[n] VDD power pad driving core power and OPWR bus with grounded gate NMOS protection. All supplies should be 3.6V or less. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
PADM	0 (pF)

AREA : 27735.0 sqr microns

Power Characteristics:

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	2.2996e-05	uW

Power Characteristics:

Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	0.000250437	uW

Power Characteristics:

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	0.0952313	uW

Test Data

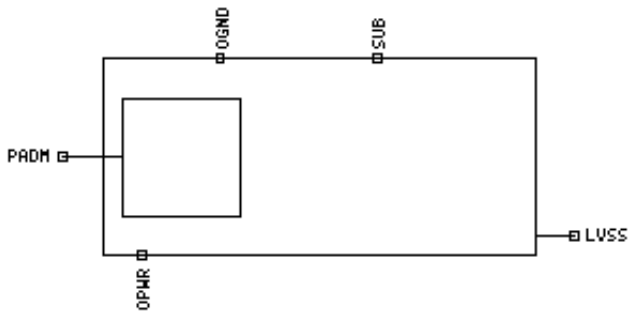
Parameter	Description	Minimum	Maximum	Units
Vi_max	Maximum Voltage	-100	100	V
I_max	Maximum sink/source current	-2	2	A

zgppxcg_mt

Description

"ZGPPXCG_MT is a[n] ZGPPXCG is a[n] VSS ground pad driving core ground with anti-parallel diodes from core ground to OGND bus. All supplies should be 3.6V or less. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
PADM	0 (pF)

AREA : 27735.0 sqr microns

Power Characteristics:

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	1.59118e-07	uW

Power Characteristics:

Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	9.90693e-07	uW

Power Characteristics:

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	0.0833554	uW

Test Data

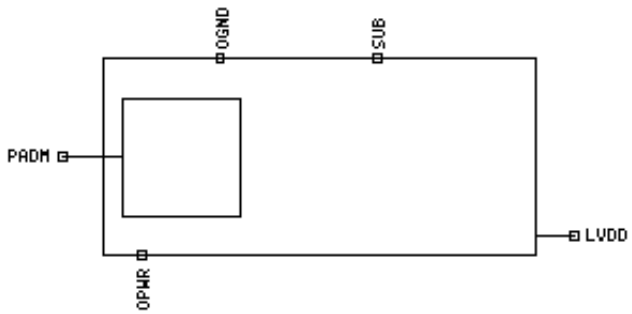
Parameter	Description	Minimum	Maximum	Units
Vi_max	Maximum Voltage	-100	100	V
I_max	Maximum sink/source current	-2	2	A

zgppxcp_mt

Description

"ZGPPXCP_MT is a[n] ZGPPXCP is a[n] VDD power pad driving core power with grounded gate NMOS protection on CPWR. All supplies should be 3.6V or less. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
PADM	0 (pF)

AREA : 27735.0 sqr microns

Power Characteristics:

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	2.66507e-08	uW

Power Characteristics:

Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	2.81918e-07	uW

Power Characteristics:

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	0.0249974	uW

Test Data

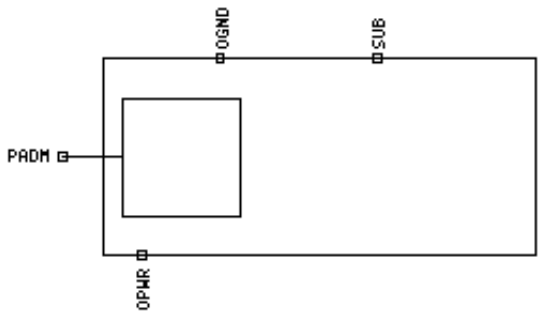
Parameter	Description	Minimum	Maximum	Units
Vi_max	Maximum Voltage	-100	100	V
I_max	Maximum sink/source current	-2	2	A

zgppxpg_mt

Description

"ZGPPXPG_MT is a[n] ZGPPXPG is a[n] VSS ground pad driving OGND with grounded gate NMOS protection. All supplies should be 3.6V or less. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
PADM	0 (pF)

AREA : 27735.0 sqr microns

Power Characteristics:

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	3.52285e-05	uW

Power Characteristics:

Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	0.00037553	uW

Power Characteristics:

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	0.100287	uW

Test Data

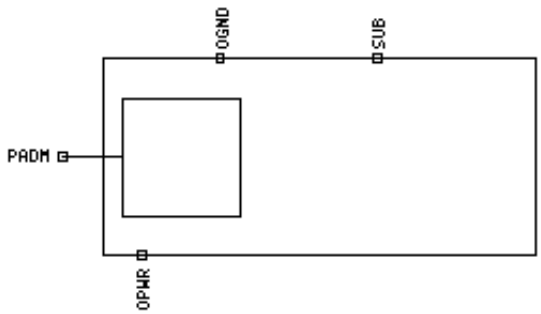
Parameter	Description	Minimum	Maximum	Units
Vi_max	Maximum Voltage	-100	100	V
I_max	Maximum sink/source current	-2	2	A

zgppxpp_mt

Description

"ZGPPXPP_MT is a[n] ZGPPXPP is a[n] VDD power pad driving OPWR with grounded gate NMOS protection. All supplies should be 3.6V or less. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
PADM	0 (pF)

AREA : 27735.0 sqr microns

Power Characteristics:

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	2.30027e-05	uW

Power Characteristics:

Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	0.000250453	uW

Power Characteristics:

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	0.0952313	uW

Test Data

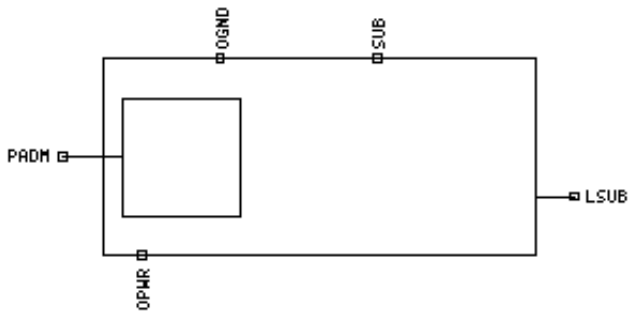
Parameter	Description	Minimum	Maximum	Units
Vi_max	Maximum Voltage	-100	100	V
I_max	Maximum sink/source current	-2	2	A

zgppxsb_mt

Description

"ZGPPXSB_MT is a[n] ZGPPXSB is a[n] SUB ground pad with grounded gate NMOS protection from SUB to OGND. Difference between SUB and OGND should be 3.6V or less. Contains a 76ux76u bond pad opening." ;

Logic Symbol



Pin Loading

Pin name	Pin loading
PADM	0 (pF)

AREA : 27735.0 sqr microns

Power Characteristics:

Conditions : Tj= -40°C, Vdd = 3.63V, Best process

Name	Value	Units
Cell Leakage Power	2.66483e-08	uW

Power Characteristics:

Conditions : Tj= 25°C, Vdd = 3.3V, Typical process

Name	Value	Units
Cell Leakage Power	2.81918e-07	uW

Power Characteristics:

Conditions : Tj= 135°C, Vdd = 2.97V, Worst process

Name	Value	Units
Cell Leakage Power	0.0249974	uW

Test Data

Parameter	Description	Minimum	Maximum	Units
Vi_max	Maximum Voltage	-100	100	V
I_max	Maximum sink/source current	-2	2	A