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1.1 General 3.3V IOLIB specification

1.1.1 DC specifications

Table 1: Absolute Maximum Ratings

Vdd	3.3V Power Supply Voltage	-0.5V to 4V	
	Input or Output Voltage	-0.5V to (Vdd+ 0.5V)	
	Input or Output Voltage	-0.5V to 5.5V	Note 1

Table 2: Recommended DC Operating Conditions

Vdd	Power Supply Voltage	2.7 to 3.6V	Note 1
T_j	Operating Junction temperature	-40^{o}C to 125^{o}C	

Table 3: General Interface Electrical Characteristics

	Parameter	Conditions	Min	Typ	Max	Unit	Note
Iil	Low Level Input Current Without pull-up device	Vi=0V			1	uA	1
Iih	High Level Input Current Without pull-down device	Vi=Vdd			1	uA	1
Ioz	Tri-state Output leakage Without pull up/down device	Vo=0V or Vdd			1	uA	1
IozFT	Five Volt tolerant Tri-state Output leakage Without pull up/down device	Vo=0V or Vdd			1	uA	1
		Vo=5.5V		1	3	uA	
Cin	Input capacitance		See data-sheets				
Cout	Output capacitance		See data-sheets				
Cio	I/O capacitance		See data-sheets				
I latchup	I/O Latch-up Current	V<0V, V>Vdd	200			mA	
Vesd	Electrostatic Protection	Leakage < 1uA	2000			V	2

Table 4: Low Voltage CMOS Interface DC Electrical Characteristics

	Parameter	Conditions	Min	Typ	Max	Unit	Note
Vil	Low level input voltage				0.2*Vdd	V	
Vih	High level input voltage		0.8*Vdd			V	
Vhyst	Schmitt trigger hysteresis		0.8			V	
Vol	Low level output Voltage	Iol=XmA			0.4	V	1, 2
Voh	High level output Voltage	Ioh=-XmA	0.85*Vdd			V	1, 2

Table 5: Low Voltage TTL Interface DC Electrical Characteristics

	Parameter	Conditions	Min	Typ	Max	Unit	Note
Vil	Low level input voltage				0.8	V	1
Vih	High level input voltage		2.0			V	1
Vilhyst	Low level Threshold input falling		0.9		1.35		1
Vihhyst	High level threshold input rising		1.3		1.9		1
Vhyst	Schmitt trigger hysteresis		0.4		0.7	V	1
Vol	Low level output Voltage	Iol=XmA			0.4	V	1, 2,3
Voh	High level output Voltage	Ioh=-XmA	2.4			V	1, 2,3

Table 6: Pullup & pulldown Characteristics

	Parameter	Conditions	Min	Typ	Max	Unit	Note
Ipu	Pullup current	Vi = 0V	-25	-66	-125	uA	1
Ipd	Pulldown current	Vi = Vdd	25	66	125	uA	1
Ipd	Pulldown current	Vi = 5V	25	66	125	uA	2
Rup	Equivalent pull-up resistance	Vi = 0V		50		KOhm	
Rpd	Equivalent pull-down resistance	Vi = Vdd		50		KOhm	
Rpd	Equivalent pull-down resistance	Vi = 5V		76		KOhm	2

^{o}C

^{o}C

1.1.2 Naming convention

❑ Inputs

IBUF	CMOS input buffer.
TLCHT	TTL input buffer.
SCHMIT	Input buffer with hysteresis.
1st suffix	T for TTL levels
	C for CMOS levels
	Not present after IBUF & TLCHT.
2nd suffix	H for High drive input stage.
3rd suffix	U for active pull up
	D for active pull down.
4th suffix	Q for switch on pull-up/down.
5th suffix	_FT for 5V tolerant.

❑ Outputs

B	Push pull output buffer.
BT	Tri-state output buffer.
1st suffix	Drive capability in mA.
2nd suffix	C for CMOS (Absence of “C” = TTL).
3rd suffix	R for slew rate control
	AR for active slew rate control.
4th suffix	OD for open drain.
5th suffix	P for test functions.
6th suffix	_FT for 5V tolerant.

❏ Bidirectional

BD	Bidirectional buffer.
1st suffix	Drive capability in mA.
2nd suffix	H for High drive input stage.
3rd suffix	ZI for Tri-state input stage.
4th suffix	S for Schmitt trigger on input.
5th suffix	T for TTL levels
	C for CMOS levels.
6th suffix	R for slew rate control
	AR for active slew rate control.
7th suffix	OD for open drain output.
8th suffix	U for active pull up.
	D for active pull down.
9th suffix	Q for switch on pull-up/down.
10th suffix	P for test functions.
11th suffix	_FT for 5V tolerant.

1.2 Buffers description (Functionality)

1.2.1 Input stages

❏ Input buffers are available with two possible drives towards the core chip:

- "Normal drive" is equivalent to an X4 drive in the standard digital library. These cells are characterised with internal loads up to 80 Standard Loads, i.e. 0.72pF.
- "High drive" is equivalent to an X16 drive in the standard digital library. They are characterized with loads up to 316 Standard Loads, i.e. 2.84pF. The suffix "H" is used in the cell name when high drive is present.

1.2.2 Five volt Tolerant inputs:

- Five tolerant inputs are input buffers that can receive 5V signals while being supplied under 3.3V:

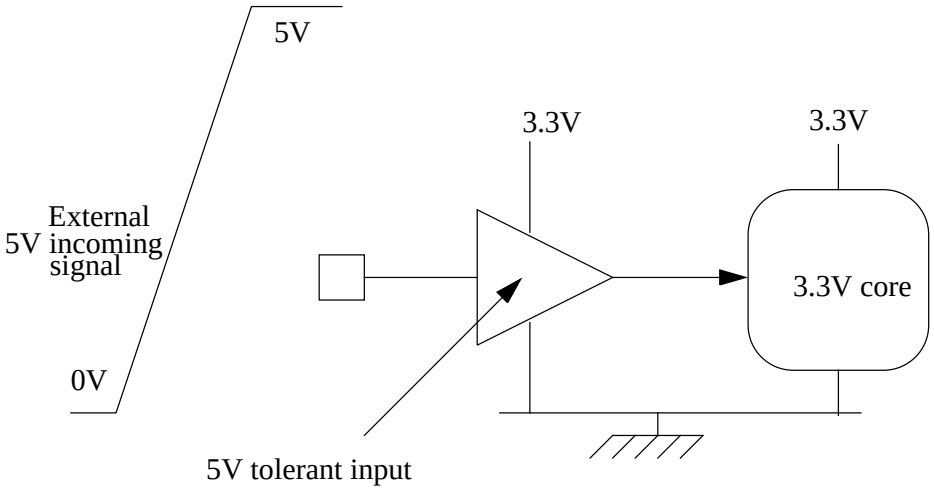

Figure 1: 5V tolerant input principle

- Only TTL buffers (with or without hysteresis) are available with the five volt tolerant option, which means that the minimum supply voltage on-chip is 3.0V.
- Pull down devices are available for 5V tolerant as for normal inputs and sink the same current.

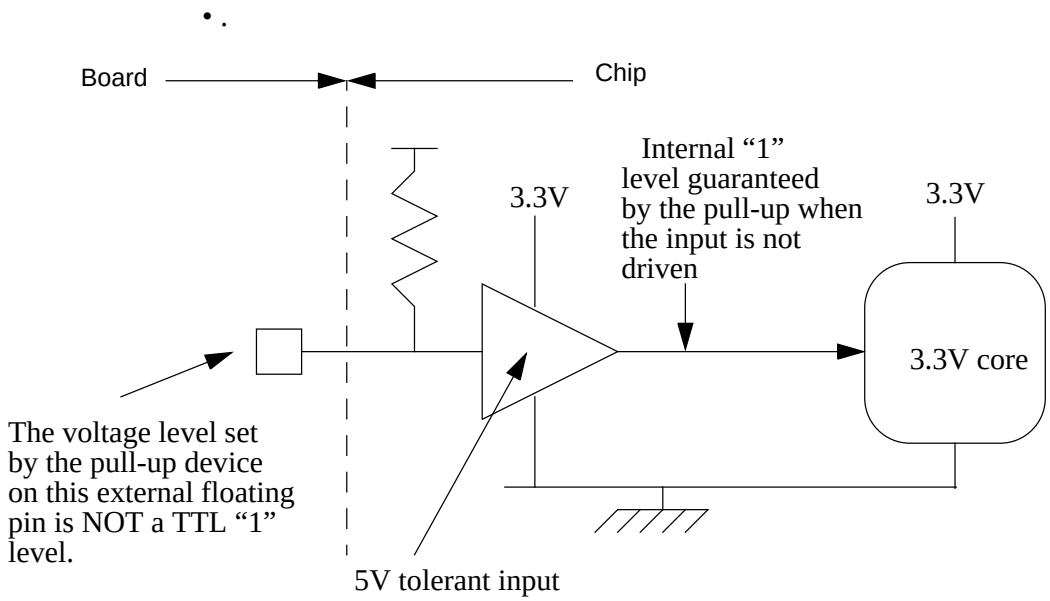

Figure 2: Pull-up device for 5V tolerant inputs

1.2.3 Output buffers: Current drive and slew rate control

❏ Drive choice:

- The rating of output buffers in mA (2, 3, 4, 6, or 8mA) is a DC specification. This is the current a buffer can source/sink within VOH and VOL specifications, in worst case conditions. The maximum output current, during output switching, is much higher. Please refer to table 7.
- The primary goal of the slew rate control circuitry is to reduce the SLOPE of the CURRENT flowing to/from the load. As the timing degradation is usually not very significant, slew rate controlled buffers should be used as much as possible.

Table 7: Typical current characteristics of output buffers. 25ºC, 3.3V, TYP models.

Slew rate control	Current rating	Condition	Typ dI/dT	Typ peak current
YES	2 mA	Cl=35pF	8 mA/nS	24 mA
	3 mA	Cl= 60pF	12 mA/nS	38 mA
	4 mA	Cl=85pF	16 mA/nS	50 mA
	6 mA	Cl=120pF	24 mA/nS	75 mA
	8 mA	Cl=150pF	32 mA/nS	100 mA
NO	2 mA	Cl=35pF	16 mA/nS	27 mA
	3 mA	Cl=60pF	24 mA/nS	42 mA
	4 mA	Cl=85pF	32 mA/nS	55 mA
	6 mA	Cl=120pF	52 mA/nS	83 mA
	8 mA	Cl=150pF	74 mA/nS	110 mA

The dI/dT values are mean values between currents in vdde! and gnde! power lines for one switching buffer.

The peak current values are for currents in gnde!.

- In order to reduce the noise on the supplies, it is important to use the smallest buffers compatible with the application timing requirements (refer to timing values in the datasheets) and always prefer buffer with slew rate control.
- For output stages, the difference between TTL and CMOS is only the thresholds at which the timing delays are measured (vdd/2 for CMOS, 1.4V for TLL). The output transistors are the same in both cases.

1.2.4 Output buffers: test pins

There are two versions of each output buffer and bidirectional: with (“P”

suffix in the cell name) and without test pins.

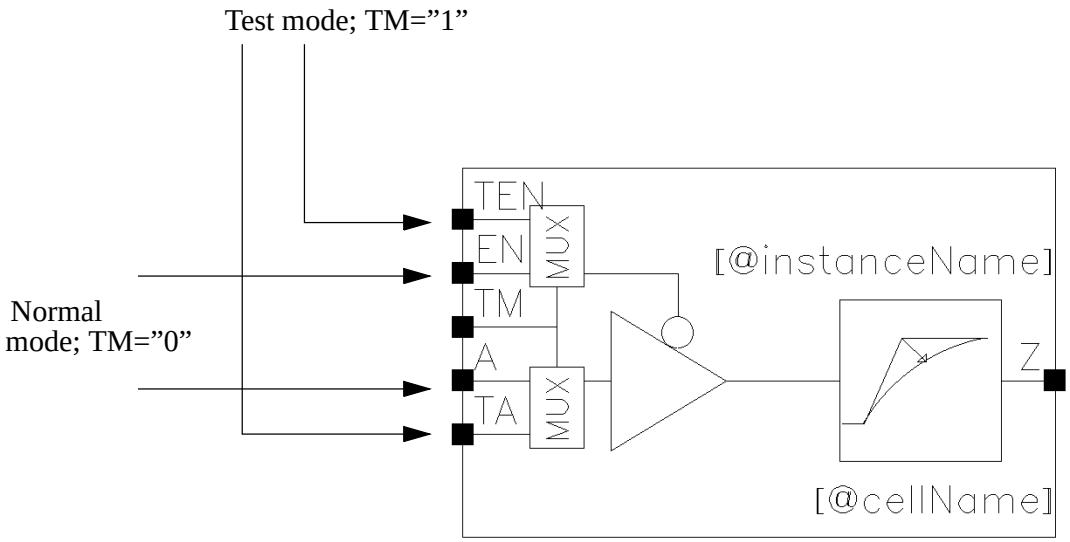

Figure 3: Buffer with test pins

Two muxs are added on the input and tri-state signals providing the following functionality:

Table 8: Modes of operation of an output buffer with test pins

TM	Function
0	Z is driven by A and EN pins. TA and TEN are not used.
1	Z is driven by TA and TEN. A and EN are not used.

These muxs allow to easily put in place a chip test methodology (Boundary scan, IDDQ, etc.) using TA and TEN without any extra delay in the normal operation.

1.2.5 Five volt Tolerant outputs:

- 5V tolerant output buffers are buffers supplied under 3.3V which can drive external loads from 0 to 3.3V but can sustain 5V signals when in tri-state mode:

:

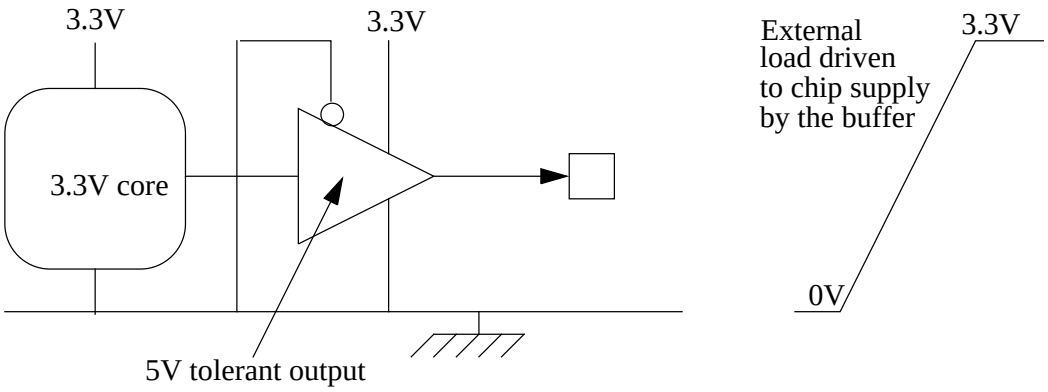

Figure 4: 5V tolerant output buffer in active mode.

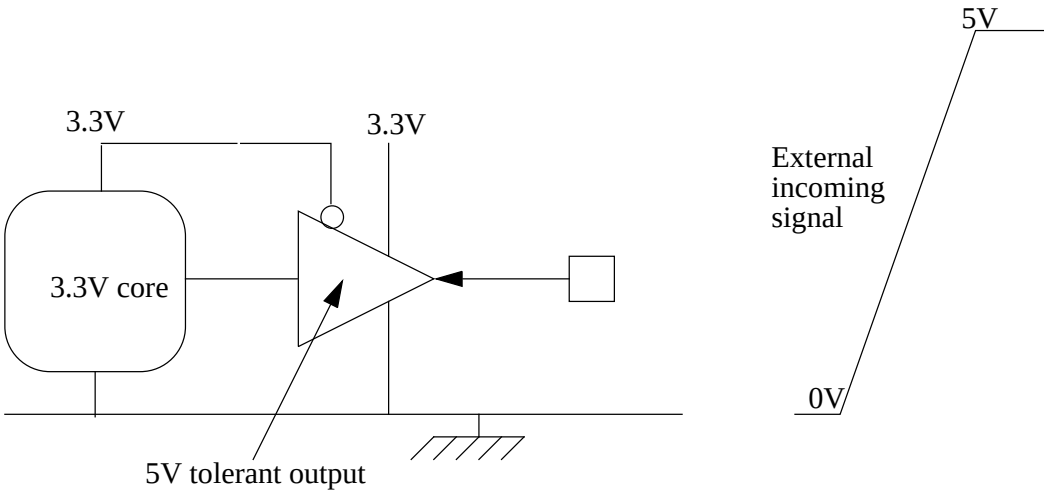

Figure 5: 5V tolerant output buffer in tri-state mode.

- Only TTL buffers are available with the five volt tolerant option, which means that the minimum supply voltage on-chip is 3.0V.
- Only tri-state buffers are available with the five volt tolerant option.

1.2.6 Maximum voltage applicable to 5V tolerant buffers

The 5V tolerant input and output buffers can sustain a absolute maximum external voltage of 5.5V. This condition is safe for latchup, hot carrier injection as well as gate oxide integrity.

However, signals on unterminated bus lines might have overshoot above 5.5V. This situation presents some latchup and hot carrier risks which are currently evaluated. Waiting for more experimental data, we recommend the following:

- **Maximum peak voltage = 6V (Maximum DC voltage = 5.5V).**

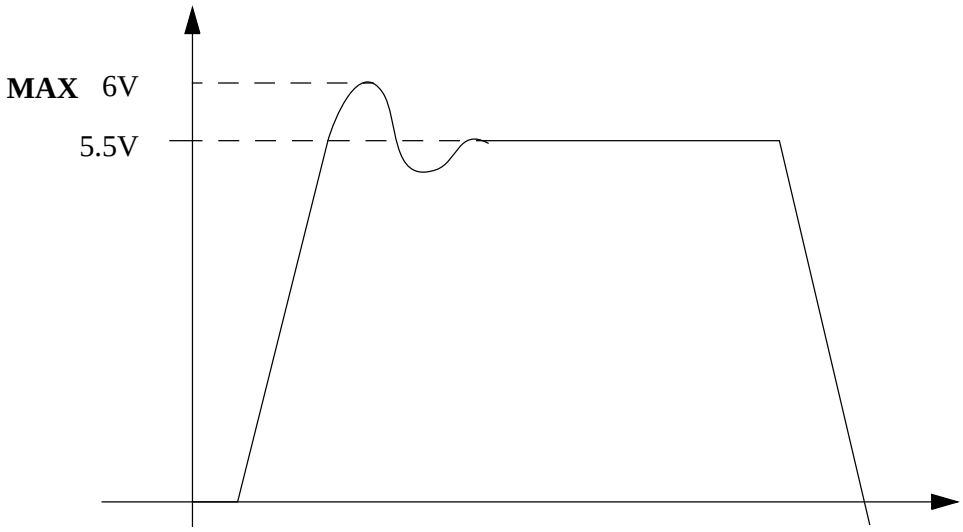

Figure 6: Maximum overshoot applicable to a 5V tolerant buffer

❑ **Case of signal overshoots higher than 6V:**

This clipping can be achieved on-chip thanks to a dedicated 5V rail present in the IOs and a specific vdd pad, VDD5.
Diodes must be used from the signal pad to that rail:

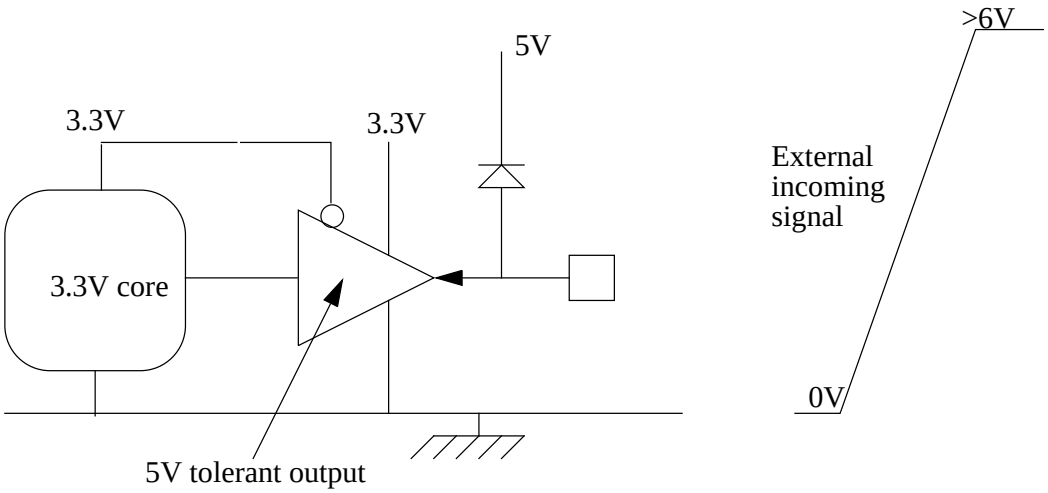

Figure 7: Clipping of >6V signals to the 5V rail

1.2.7 Power supply failure condition

The power supply failure condition is a state where the chip isn't supplied but connected to active signal lines. There are several cases:

- **Active external lines; 3.3V buffers on the non powered chip: NOT ACCEPTABLE**: The chip would be supplied by the signal lines via forward biased diodes to vdd, altering the signals.

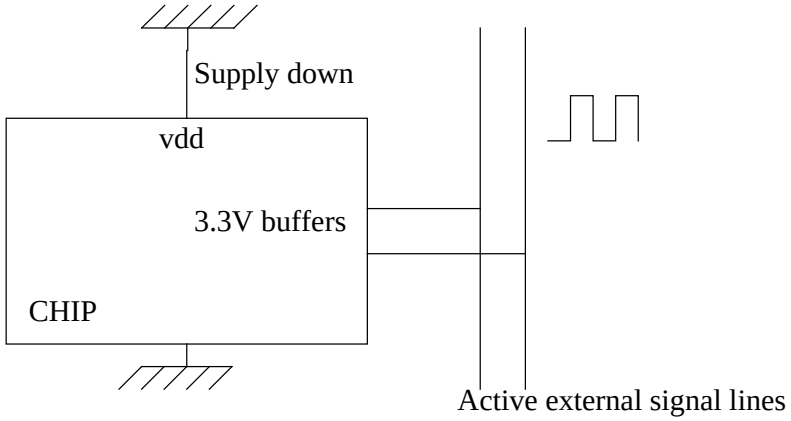

Figure 8: Power down unacceptable with signals on the bus: The external signals are altered.

- **3.3V external lines, 5V tolerant buffers on the non powered chip: ACCEPTABLE**

  The 5V tolerant buffers don't leak (external signals not altered) and there is no reliability problem.

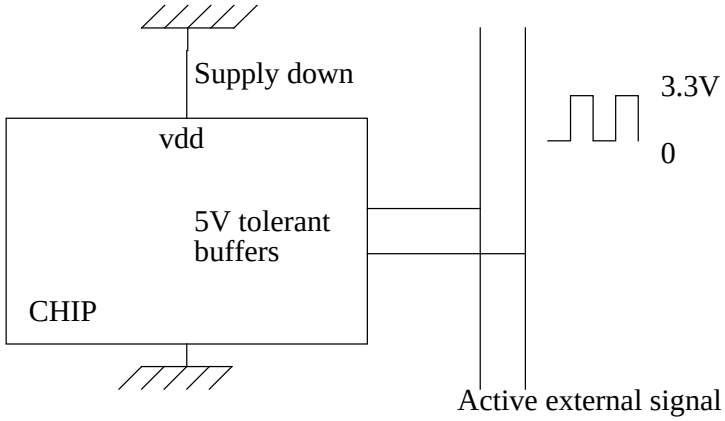

Figure 9: Power down acceptable with 3.3V on the bus. This is a "fail safe" condition.

❑ **5.5V external lines, 5V tolerant buffers on the non powered chip: ACCEPTABLE FOR VERY SHORT TIMES.**

The buffers don't leak (external signals not altered) but there is a fast degradation of the gate oxides in the buffers.

The total maximum time under this stress condition is 2 days.
So to get a 10 year life time, the maximum duty factor is 1/1800, which leads for example to a maximum stress duration of 48 seconds per day.

This limits the possibility of this configuration to short power-up/down sequences, for example.

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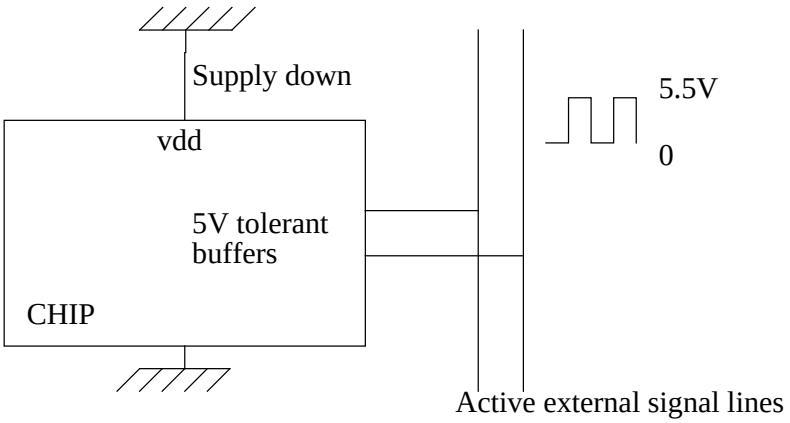


Figure 10: Power down acceptable with 5.5V on the bus only for short times

❑ **>6V external lines, 5V tolerant buffers on the non powered chip: NOT ACCEPTABLE.**

This case is the same as the previous one, but the active signals lines carry peak voltage higher than 6V. The oxide integrity is not guaranteed under such a stress.

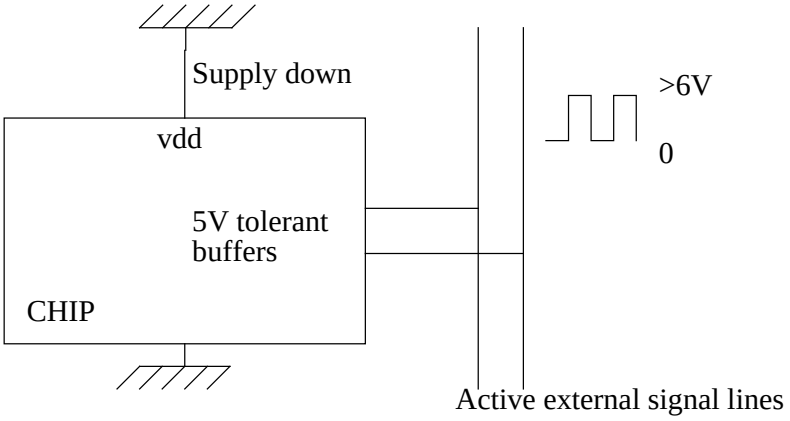


Figure 11: Power down not acceptable with >6V on the bus

1.2.8 Bidirectional buffer

- Normal bidirectional buffers are tri-state output buffers associated with an input buffer. All the previous notes on input and output buffers apply to bidirectionals.

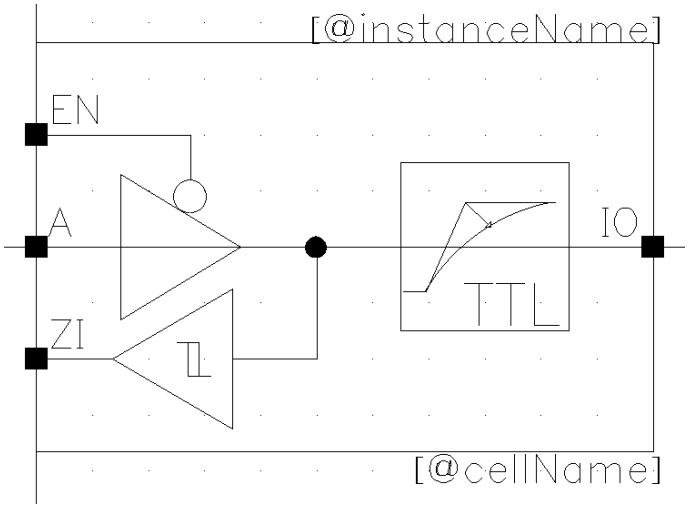


Figure 12: “Normal” bidirectional

Table 9: Modes of operation of a “normal” bidirectional buffer

EN	Function
0	Output buffer plus copy of A on ZI. The input signal arrives on A, the cell drives IO and ZI with IO = ZI = A.
1	Input buffer. The input signal arrives on IO, the cell drives ZI with ZI=IO. A is not used.

❑ Also, tri-state input buffers are available in order to build bidirectional cells tri-state on both sides to interface external & internal buses:

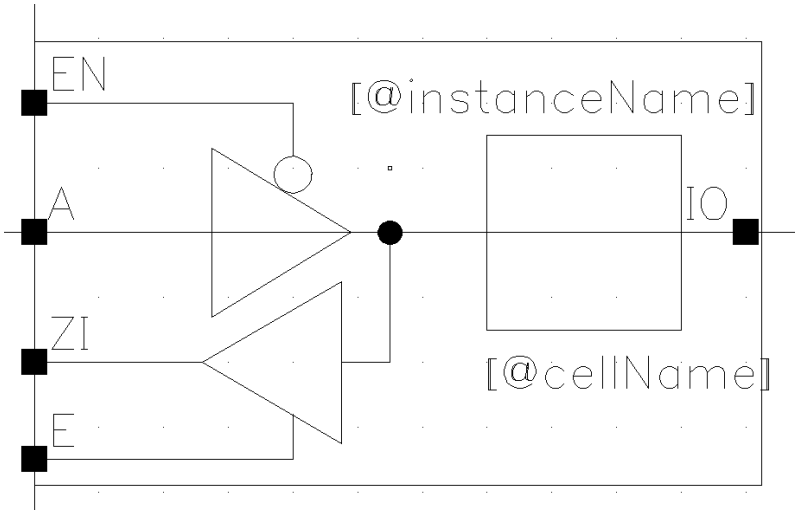


Figure 13: “true” bidirectional

• The suffix “ZI” is used in the cell name when the tri-state input option is present.
Note: Only CMOS input with high drive to core (X16) can be tri-state.

Table 10: Modes of operation of a bidirectional buffer tri-state on both sides

EN	E	Function
0	0	Output buffer. The input signal arrives on A, the cell drives IO with IO = A. ZI is in a tri-state mode.
0	1	Output buffer plus copy of A on ZI. The input signal arrives on A, the cell drives IO and ZI with IO = ZI = A.
1	0	Open circuit. Both ZI and IO are in a tri-state mode. The cell doesn’t drive ZI nor IO. A is not used.
1	1	Input buffer. The input signal arrives on IO, the cell drives ZI with ZI= IO. A is not used.

1.2.9 Pull-up and pull-down active devices - IDDQ compliance

Weak pull-up and pull-down active devices connected to the pad node are available in some of the cells of the library. They fall into two categories: Devices that are always on (U or D suffix in cell names) or devices that can be switched on/off (UQ or DQ suffix in cell names). The switch versions are useful for example when IDDQ testing is required since in this case all IOs can be put in a zero DC power consumption state.

The nominal resistance is typically 50K Ohms (See General specifications).

Table 11: Pull-up and pull-down devices

pull type	pull control pin	Function
Simple pull-up (U)	-	50K Ohm pull-up.
Pull-up with switch (UQ)	TUD=0	50K Ohm pull-up.
	TUD=vdd	Open circuit, no current.
Simple pull-down (D)	-	50K Ohm pulldown.
Pull-down with switch (DQ)	TUD=0	50K Ohm pull-down.
	TUD=vdd	Open circuit, no current.

1.2.10 Peripheral buffers

In the “OTHER” category of the MTC45200 library, two peripheral buffers are available: BUF4 and BUF8.

They are identical to B4 and B8 output buffers, but the “Z” output redirected towards the core circuit. They can be used to drive big on-chip loads.

1.2.11 Analog pads

Four analog pads are available in the “OTHER” category.

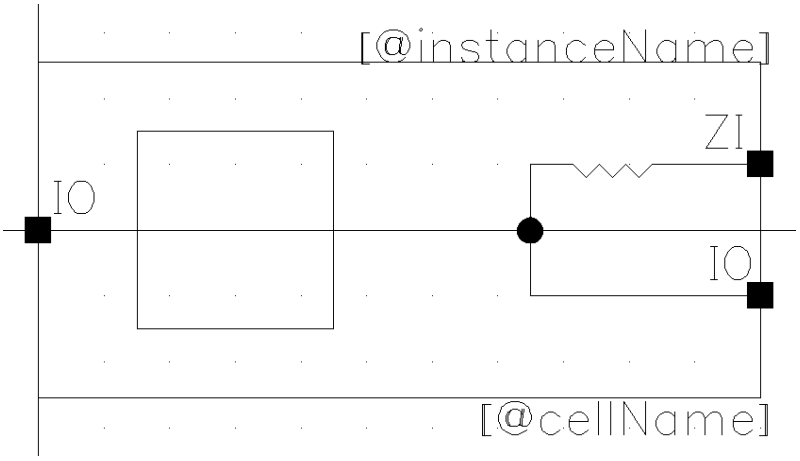


Figure 14: ANA and ANA_OD pads

❏ ANA and ANA_OD are “bidirectional” pads for analog signals. Both contain primary ESD protections in parallel with the pad plus a secondary diode protection after a series resistor. ANA has also protection diodes to vdd. Thus ANA is the best protected cell while ANA_OD can be used when diodes to vdd are not allowed in the application (Signals higher than vdd, for example).

- ZI is the access to core via the series resistor, (440 Ohms). This is the best protected pin against ESD and should be used in particular for input signals.
- IO is a direct access from the pad to the core, bypassing the series resistance. It can be used for output analog signals or any signal when a series resistance cannot be used. The metal2 width is 18.6um, allowing an equivalent current of 28mA in worst case electromigration (T=125°C). The resistance from the bonding pad to the core access is 0.64 Ohm.

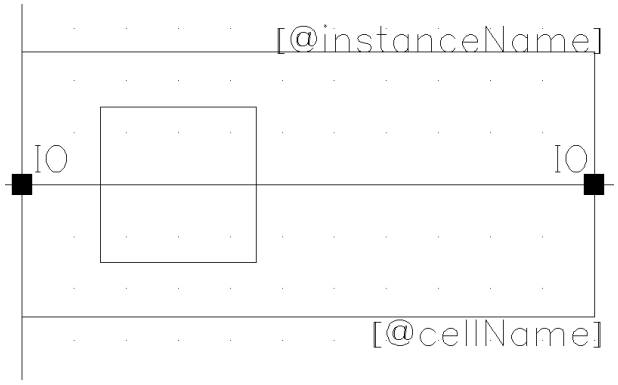


Figure 15: ANA_NOPROT pad

❏ ANA_NOPROT is a simple wire pad, without any protection device.

• The connection width is 20um (metal2), allowing an equivalent current of 30mA in worst electromigration case (T=125°C). The resistance from the bonding pad to the core access is 0.64 Ohm.

1.2.12 Crystal pad oscillators

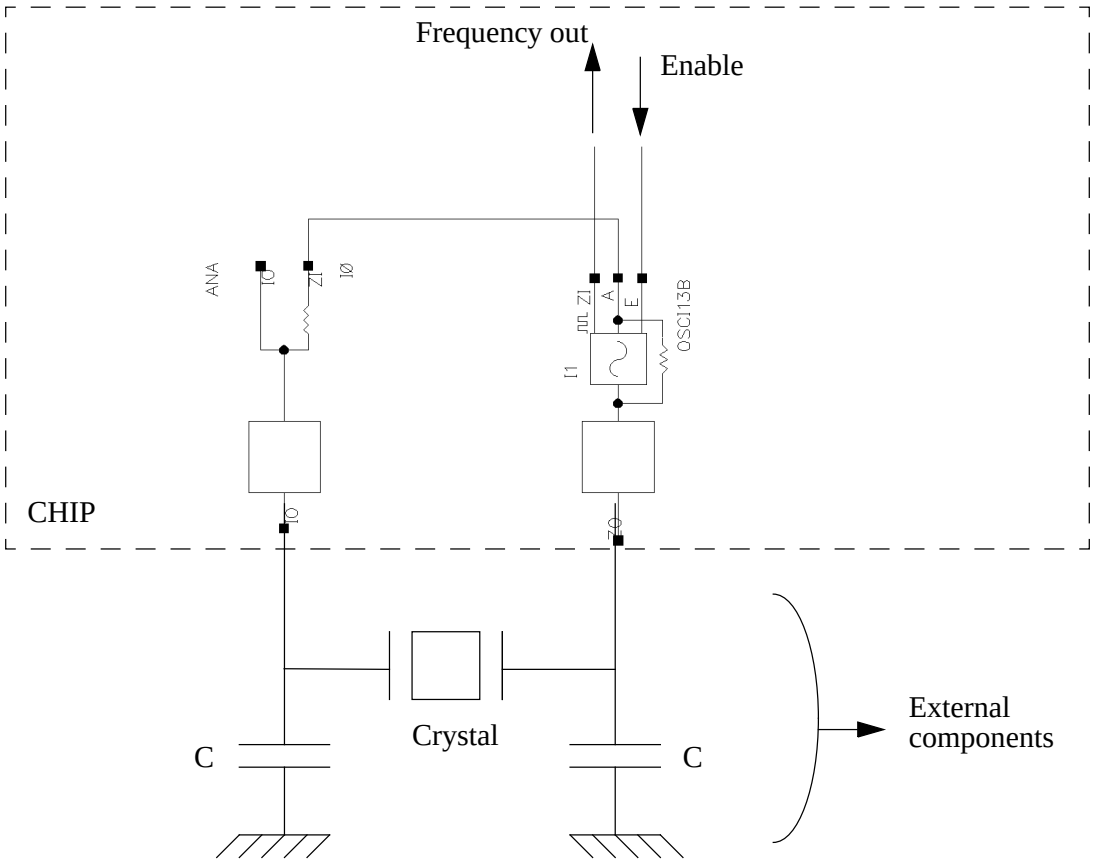


Figure 16: Crystal pad application scheme

The three crystal pad oscillators OSCI13B (13Mhz) , OSCI27B (27Mhz) and OSCI32B (32Khz) need to be used in conjunction with the ANA pad cell. The full configuration for a crystal oscillator occupies two pads.

Suggested values for C are:

- 27pF for the 32Khz oscillator and
- 16pF for the 13Mhz oscillator.

But other values may be tried depending on the environment (package type...).

- E = “1” allows oscillations while E = “0” stops them and the power consumption becomes null.

Table 12: Common crystal pad specifications

	min	typ	max	Note
Power supply	2.7V	3.3V	3.6V	
Temperature	-40 C		+ 125 C	
Static IDD			< 0.1uA	Disabled oscillator. E= 0

Table 13: 32 Khz crystal pad specifications

	min	typ	max	Note
Frequency		32 Khz		
Start-up time			500mS	
Transconductance	0.29			mA/V

Table 14: 13 Mhz crystal pad specifications

	min	typ	max	Note
Frequency		13 Mhz		
Start-up time			10mS	
Transconductance	0.6			mA/V

1.3 Supplies description

1.3.1 Power distribution in the IOs

There are 3 different metal3 power rails inside the IO cells: gndm3 , vddm3a , vddm3b.

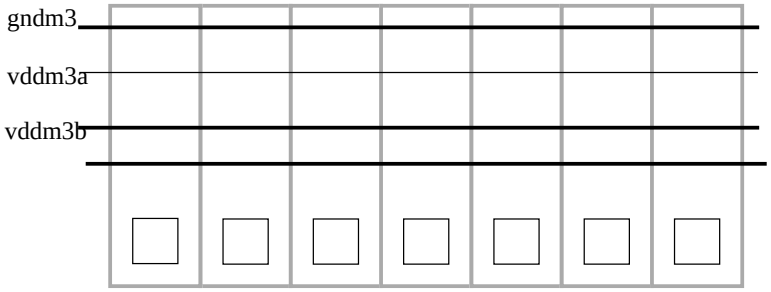


Figure 17: Power rails in IOs

The primary goal of having different rails is to minimize the effect of the noisy output buffers. To do so, the IOs are supplied as follow:

vdd & gnd: Internal supply: generic digital supply, used for core circuitry as well as pre-drivers in IOs. gnd connects the substrate throughout the chip except near the bonding pads.

1.3.2 Power pad and corner cell usage

There are a number of power supply pads and corner cells in the “SUPPLY” category of the MTC45200 library.

❑ Usual chip power distribution:

In a “normal” chip, with a unique power for the core & small circuitry in IOs, the following scheme will be used:

The VERY MINIMUM power pad set to be used in any chip is:

The pads must be placed several times throughout the periphery, depending

on the chip:

➥ The number of VDD/VSS pairs is a function of the core power consumption: The electromigration rules allow a maximum average current of 100 mA through each VDD or VSS pad.
This is an absolute maximum rating.
In practise, the number of VDD/VSS pairs must be defined by studies of voltage drops and ground bounce. The type of core circuitry will be critical in this evaluation (frequency, peak currents, etc...).

☞ This calculation is not is the scope of this document.

❑ **Chip power distribution with independent core supplies:**

In some cases, independent power pads may be needed to supply some parts of the core chip. For example to supply a sensitive analog block with a clean power distribution, or supply parts of the chip that can be powered down while others are still active, etc...
The following scheme can be used

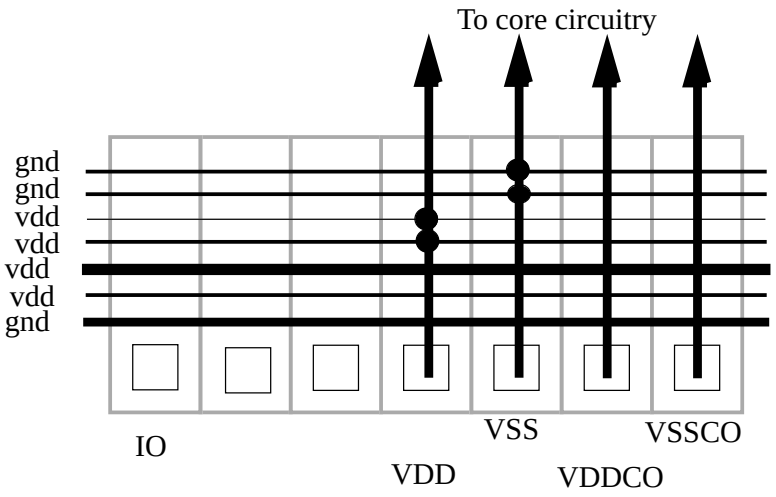


Figure 18: Chip power distribution with independent core supplies

Two cells are available in the MTC45200 library for this purpose:

VDDCO	(Internal supply for core circuitry only)
VSSCO	(Internal ground for core circuitry only)

➥ The number of VDDCO/VSSCO pads is determined as for the VDD/VSSI pads, depending on the current they are supposed to carry.

❑ **Chip power distribution when 5V must be present on chip:**

In some 5V environments with unterminated lines, the overshoot of external 5V signals may be so high that a 5V supply must be provided on the chip in order to clip the overshoots with diodes. Please refer to section 1.2.2.

1.4 Layout IO structure

1.4.1 Programmability:

❏ An important feature of the CMOS035 IO library is the possibility to program IO buffers at metal level. A unique base is common to all IOs, containing all the devices up to contact level.
Via1, metal1, via2 & metal2 are the programmable layers which connect the base components to build the different IO functions.
Upper levels (from via3 to metal5) are again common to all IOs.

- This feature makes the IO library compatible with an hybrid array chip methodology.

❏ Limitation:

- The power pads have a different base, so they cannot be programmed as IO buffers. However, all power pads have the same base so that any power pad can be replaced by another one by metal fix.
- This particular release has a polysilicon difference between 5V tolerant buffers and 3.3V buffers. This is due to an ESD clamping devices using a polysilicon gate in 3.3V buffers which needs to be further qualified before being used also in the 5V tolerant environment. For the time being, the poly gate has been removed from 5V tolerant buffers.
- The ANA_NOPROT pad is not programmable (simple wire pad).
- The crystal pad oscillators are not programmable.

1.4.2 IO floorplan and cross-section

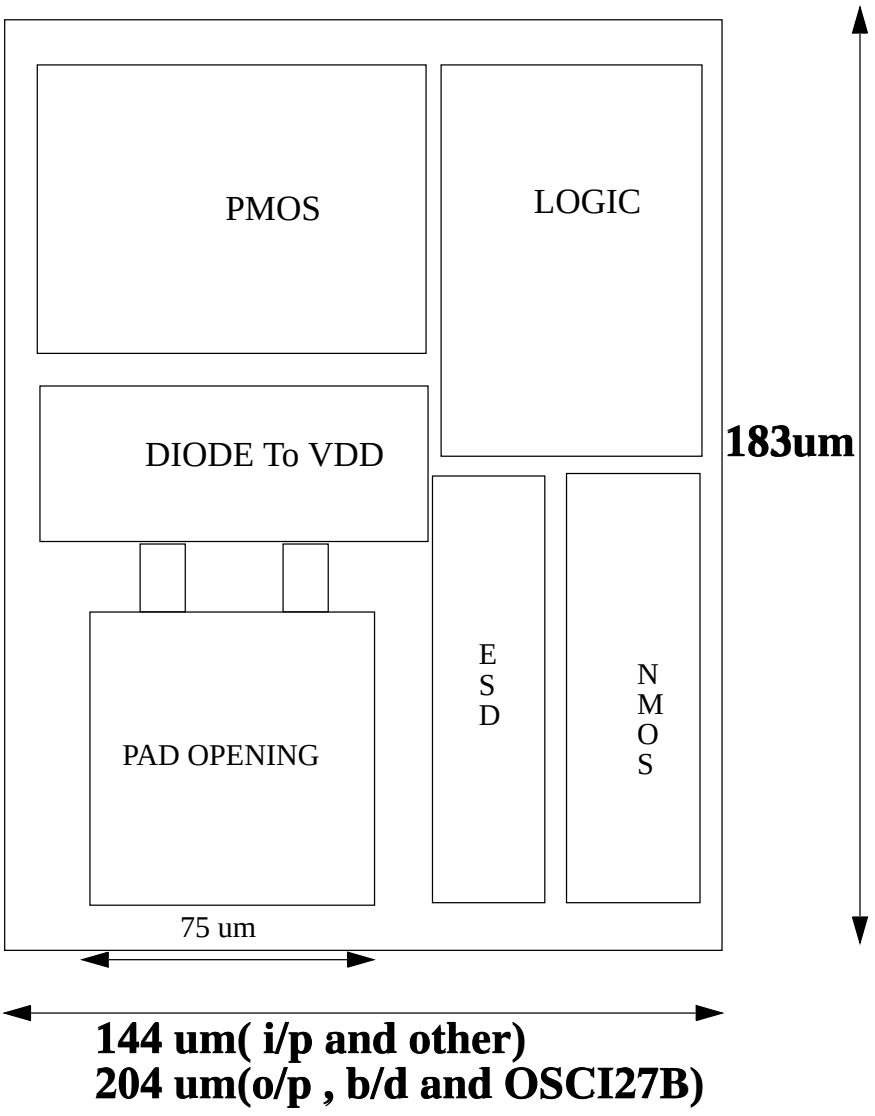


Figure 19: layout Cell floorplan

1.5 Placement and routing of IO cells

1.5.1 IO placement - latchup guard band continuity -

❏ In the “P&R” category of the library, you’ll find cells dedicated to the placement and routing of the IOs at top chip level.

❏ Abutment: All cells can be abutted to each other. The metal power ring continuity is automatically ensured by abutment.

❏ If there is free spaces between IOs (core limited chip), filler cells must be used to fill up these empty areas. There are different filler cell widths:

IOFILLER1: 1.5um wide
IOFILLER2: 3.0um wide
IOFILLER4: 6.0um wide
IOFILLER8: 12um wide
IOFILLER16: 24um wide
IOFILLER32: 48um wide
IOFILLER64: 96um wide

It is advised to start the filler cell placement by the widest cell possible and then continue with decreasing sizes until the gaps are completely filled.
(Note: When using the cell3 kit package for automatic P&R, these filler cells are automatically placed).
Filler cells contain latchup guard bands which will provide a good latchup immunity and also metal tracks to ensure the continuity of power metal rails.

1.6 Power supply pads in schematics

- ❏ Power pads have cmos.sch and symbol views. Indeed, there is some ESD circuitry inside each of them which needs to pass the LVS.
- ❏ EACH power pad used in the layout must also be present in the schematic. VSSI, VSSE, VDD and VDDE symbols only need to be instantiated. No connections are required (global nets).

❑ VDDCO and VSSCO symbols need to be specifically connected to the core, either directly or via global nets (Please refer to the next figure).

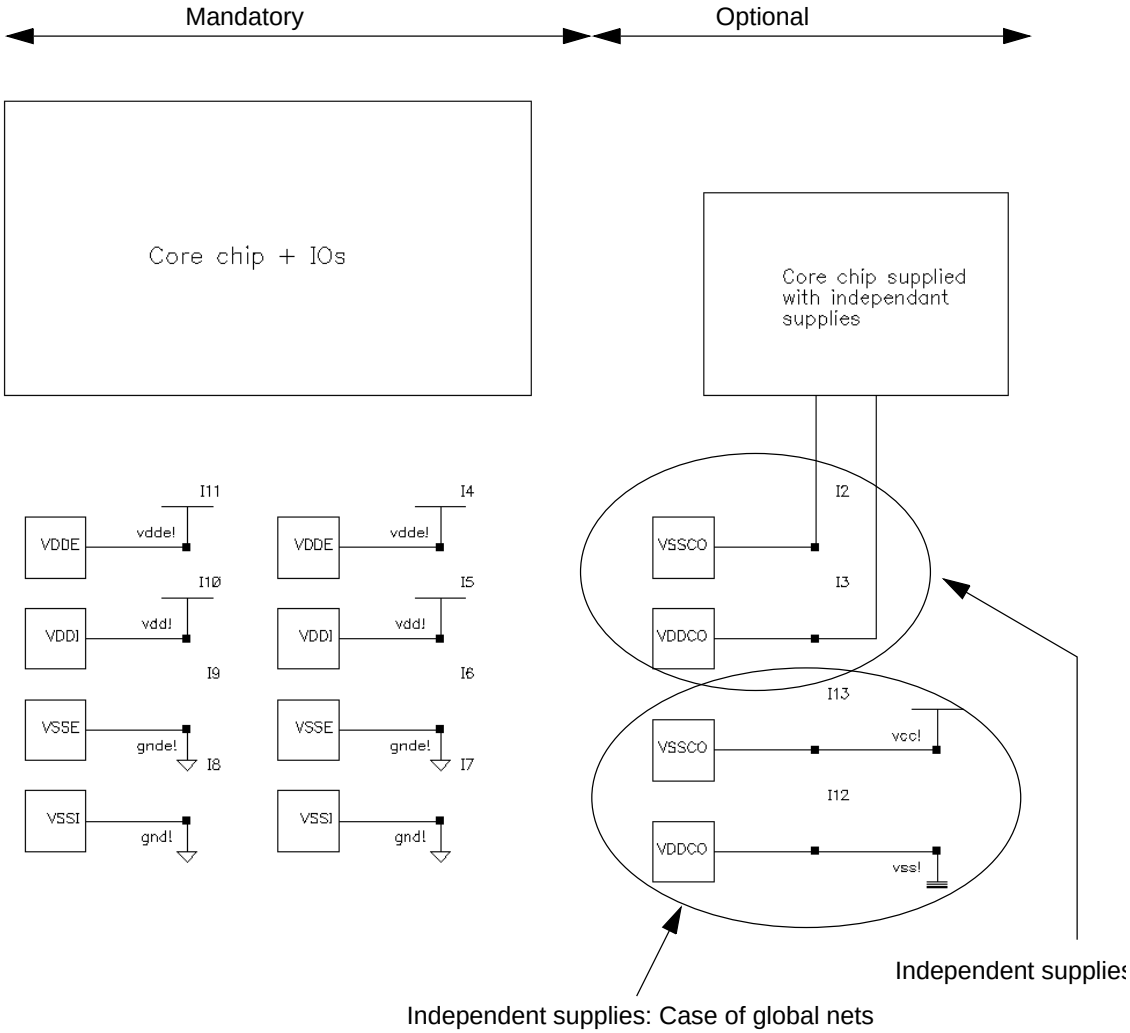


Figure 20: Power pads must be present in the top cell schematic

1.7 Diva & Dracula verifications

1.7.1 General

❑ **DRC**

➥ The ERC2 switches available in the dracula decks should not be passed on the IOs because it will flag unconnected devices present in IOs.

❑ **LVS**

The notes on DIVA LVS and DRACULA LVS in this document mainly deal with power supply issues. It is assumed as prerequisite that IO pins (signal pins) are properly labelled. In particular, the “IO label” facility of the Cell3 kit may be used to add Dracula IO labels on the chip layout.

➥ In the cmos.sch views, 2 global nets define the power supply distribution in the IOs: gnd!, vdd!. This means that on the layout these 2 nets must be identified on power pads at top level.

gnd! must be added on the pad of VSS
vdd! must be added on the pad of VDD

When the VDD and VSS pads are repeated several times around the chip as previously recommended, only one instance of each needs to be labelled. Indeed, as already mentioned, all the VDD power pads of a chip are connected together via the IO ring. Same remark for VSS.
If independent supplies are present on chip via VDDCO and VSSCO power pads, EVERY VDDCO and VSSCO pad must be labelled with the appropriate labels.

1.7.2 DIVA LVS

❑ **Preparation of the layout:**

➥ For DIVA, the Cadence global net “!” syntax must be used for power labels. Pins in metal5 purpose pin layer must be used.

1.7.3 DRACULA LVS

❑ **Preparation of the CDL netlist:**

The main concern is the presence of diodes and resistors in IO cells. For this reason, the following lines must appear in the CLD netlist of the circuit:

```
**************************************************************
* BIPOLAR Declarations                                       *
**************************************************************
*.BIPOLAR
*.RESVAL
```

These statements can be added by hand or be generated automatically by choosing the following options in the Translators->Netlist->CDL out form:

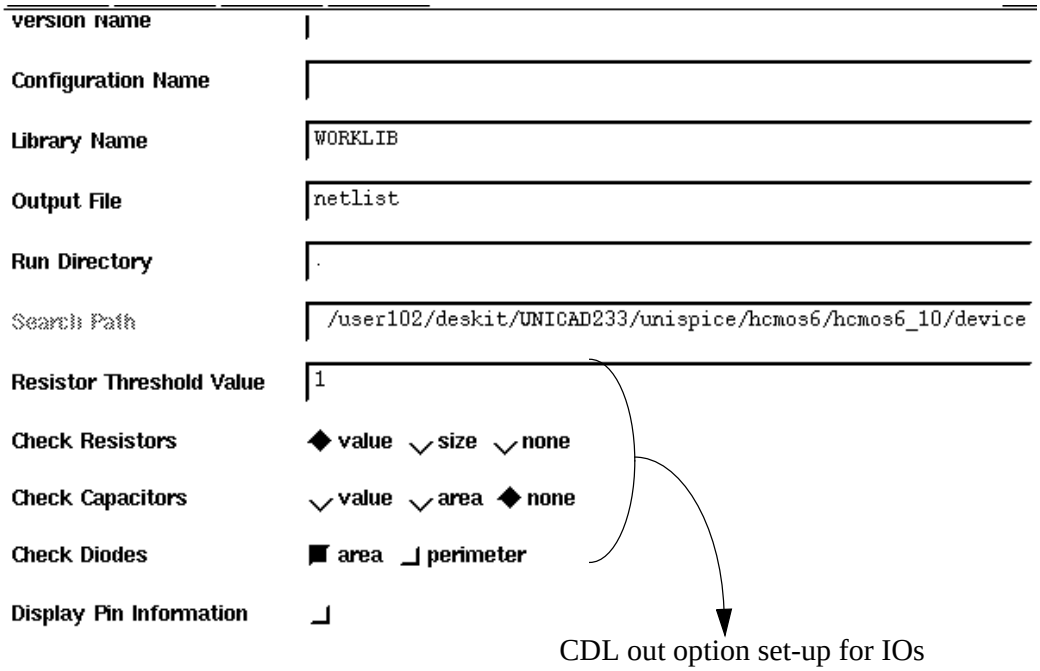


Figure 21: CDL out option form for IOs

❑ **Preparation of the layout**

➥ For DRACULA, it is recommended to use the Dracula global net ":" syntax:

❑ **Case sensitivity**

In dracula LVS, the label names can be kept as is or turned to Upper cases. In both situations, you must ensure a good compatibility between the schematic cases and the layout cases.

➥ To keep the case sensitivity:

• The supply names in the CDL netlist are in Lower cases.

• In the LOGLVS program, type the command

:CASE

to keep these lower cases.

• Use lower cases for supply labels in the layout

• By default in the dracula file, the option

CNAMES-CSEN = yes (Keep case sensitivity) is OK.

➥ To turn all cases to Upper:

• Don’t use the

:CASE

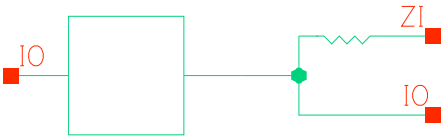
command in LOGLVS. All the CDL netlist cases will be turned to Upper cases.

• Use only Upper cases for labels in the layout and/or switch the option

CNAMES-CSEN = no (In the dracula file).

CMOS035 MTC45200	Analog Pad Buffer	ANA

SYMBOL



BEHAVIOUR

IO	ZI	IO
1	1	
1		1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
IO	1.900 pF

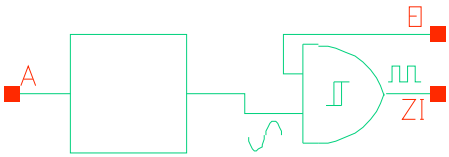
OUTPUT Pin	Max. load
IO	0.352 pF
ZI	39 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	5.0xSL	10.0xSL	20.0xSL
IO to ZI	Fall delay	0.20	0.20	0.20	0.20
IO to ZI	Rise delay	0.20	0.20	0.20	0.20

CMOS035 MTC45200	Analog Input Pad Buffer	ANA_IBUF

SYMBOL



BEHAVIOUR

A	E	ZI
1	1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	2.128 pF
E	2.0 SL

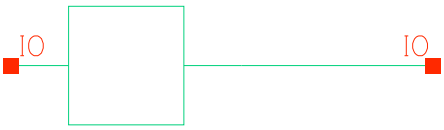
OUTPUT Pin	Max. load
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
A to ZI	Fall delay	1.74	1.81	1.87	1.98
A to ZI	Rise delay	1.97	2.03	2.08	2.16
E to ZI	Fall delay	1.16	1.23	1.29	1.40
E to ZI	Rise delay	2.10	2.16	2.21	2.29

CMOS035 MTC45200	Analog Pad Buffer with no ESD protection	ANA_NOPROT

SYMBOL



BEHAVIOUR

IO	IO
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
IO	1.900 pF

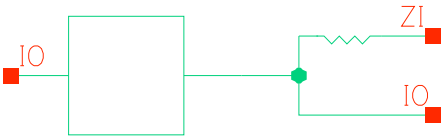
OUTPUT Pin	Max. load
IO	0.352 pF

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	5.0xSL	10.0xSL	20.0xSL
IO_F_IO_F	0.20	0.20	0.20	0.20	
IO_R_IO_R	0.20	0.20	0.20	0.20	

CMOS035 MTC45200	Analog Pad Buffer	ANA_OD

SYMBOL



BEHAVIOUR

IO	ZI	IO
1	1	
1		1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
IO	1.900 pF

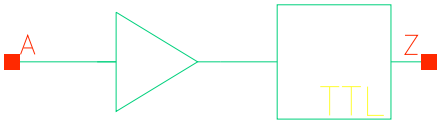
OUTPUT Pin	Max. load
IO	0.352 pF
ZI	39 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	5.0xSL	10.0xSL	20.0xSL
IO to ZI	Fall delay	0.20	0.20	0.20	0.20
IO to ZI	Rise delay	0.20	0.20	0.20	0.20

CMOS035 MTC45200	TTL Output Pad Buffer, 2mA	B2

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL

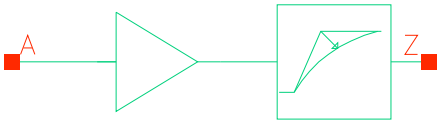
OUTPUT Pin	Max. load
Z	50.000 pF

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		12.50pF	25.00pF	37.50pF	50.00pF
A to Z	Fall delay	2.67	3.55	4.38	5.20
A to Z	Rise delay	2.30	3.04	3.76	4.47

CMOS035 MTC45200	CMOS Output Pad Buffer, 2mA, with Slew Rate Control	B2CR

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL

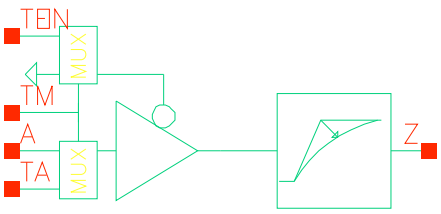
OUTPUT Pin	Max. load
Z	50.000 pF

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		12.50pF	25.00pF	37.50pF	50.00pF
A to Z	Fall delay	3.57	4.47	5.28	6.04
A to Z	Rise delay	3.47	4.45	5.36	6.23

CMOS035 MTC45200	CMOS Output Pad Buffer, 2mA, with Slew Rate Control, with Test Pins	B2CRP

SYMBOL



BEHAVIOUR

A	TM	TEN	TA	Z
-	1	0	1	1
1	0	-	-	1
-	1	1	-	Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
Z	2.810 pF

OUTPUT Pin	Max. load
Z	50.000 pF

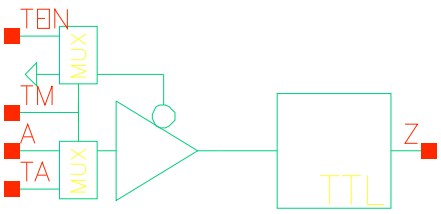
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
TEN to Z	0Z delay	1.34	1.38	1.58
TEN to Z	1Z delay	1.57	1.61	1.80
TM to Z	0Z delay	1.74	1.81	2.02
TM to Z	1Z delay	1.98	2.04	2.25

Timing/Load		12.50pF	25.00pF	37.50pF	50.00pF
A to Z	Fall delay	3.63	4.53	5.33	6.09
A to Z	Rise delay	3.54	4.53	5.43	6.31
TA to Z	Fall delay	3.96	4.86	5.67	6.43
TA to Z	Rise delay	3.82	4.80	5.71	6.58
TEN to Z	Z0 delay	3.90	4.81	5.61	6.37
TEN to Z	Z1 delay	3.79	4.78	5.68	6.55
TM to Z	Fall delay	4.14	5.04	5.84	6.60
TM to Z	Fall delay	3.97	4.87	5.68	6.44
TM to Z	Rise delay	4.25	5.24	6.14	7.01
TM to Z	Rise delay	3.71	4.70	5.60	6.47
TM to Z	Z0 delay	3.96	4.86	5.67	6.43
TM to Z	Z1 delay	3.83	4.82	5.72	6.59

CMOS035 MTC45200	TTL Output Pad Buffer, 2mA, with Test Pins	B2P

SYMBOL



BEHAVIOUR

A	TM	TEN	TA	Z
-	1	0	1	1
1	0	-	-	1
-	1	1	-	Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
Z	2.880 pF

OUTPUT Pin	Max. load
Z	50.000 pF

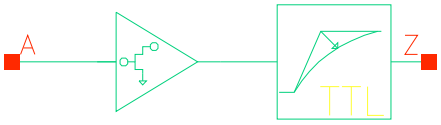
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
TEN to Z	0Z delay	1.34	1.38	1.58
TEN to Z	1Z delay	1.57	1.61	1.80
TM to Z	0Z delay	1.74	1.81	2.02
TM to Z	1Z delay	1.97	2.04	2.25

Timing/Load		12.50pF	25.00pF	37.50pF	50.00pF
A to Z	Fall delay	2.73	3.60	4.44	5.26
A to Z	Rise delay	2.38	3.12	3.84	4.55
TA to Z	Fall delay	3.06	3.94	4.77	5.59
TA to Z	Rise delay	2.65	3.40	4.12	4.83
TEN to Z	Z0 delay	2.99	3.86	4.70	5.51
TEN to Z	Z1 delay	2.62	3.37	4.09	4.80
TM to Z	Fall delay	3.24	4.11	4.95	5.77
TM to Z	Fall delay	3.06	3.94	4.78	5.60
TM to Z	Rise delay	3.09	3.83	4.55	5.26
TM to Z	Rise delay	2.55	3.29	4.01	4.72
TM to Z	Z0 delay	3.04	3.91	4.75	5.57
TM to Z	Z1 delay	2.66	3.40	4.12	4.83

CMOS035 MTC45200	TTL Open Drain Output Pad Buffer, 2mA, with Slew Rate Control	B2ROD

SYMBOL



BEHAVIOUR

A	Z
0	0
1	Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
Z	2.077 pF

OUTPUT Pin	Max. load
Z	50.000 pF

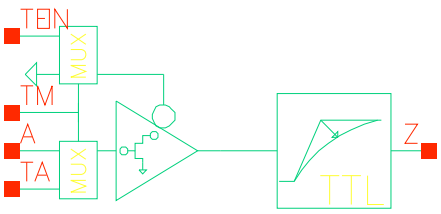
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
A to Z	0Z delay	0.94	1.00	1.17

Timing/Load		12.50pF	25.00pF	37.50pF	50.00pF
A to Z	Z0 delay	3.63	4.66	5.57	6.45

CMOS035 MTC45200	TTL Open Drain Output Pad Buffer, 2mA, with Slew Rate Control, with Test Pins	B2RODP

SYMBOL



BEHAVIOUR

A	TM	TEN	TA	Z
1	0	-	-	Z
-	1	0	0	0
0	0	-	-	0
-	1	1	-	Z
-	1	-	1	Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
Z	2.077 pF

OUTPUT Pin	Max. load
Z	50.000 pF

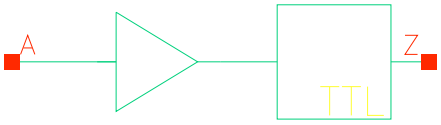
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
A to Z	0Z delay	0.95	1.00	1.18
TA to Z	0Z delay	1.24	1.28	1.49
TEN to Z	0Z delay	1.33	1.37	1.57
TM to Z	0Z delay	1.74	1.80	2.02

Timing/Load		12.50pF	25.00pF	37.50pF	50.00pF
A to Z	Z0 delay	3.69	4.71	5.63	6.50
TA to Z	Z0 delay	4.00	5.03	5.95	6.82
TEN to Z	Z0 delay	4.00	5.02	5.94	6.82
TM to Z	Z0 delay	4.18	5.20	6.12	7.00
TM to Z	Z0 delay	4.05	5.08	6.00	6.87

CMOS035 MTC45200	TTL Output Pad Buffer, 3mA	B3

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL

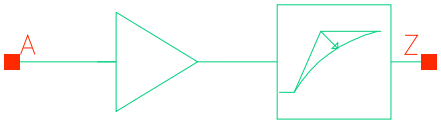
OUTPUT Pin	Max. load
Z	75.000 pF

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		18.75pF	37.50pF	56.25pF	75.00pF
A to Z	Fall delay	2.47	3.34	4.16	4.98
A to Z	Rise delay	2.26	3.00	3.72	4.43

CMOS035 MTC45200	CMOS Output Pad Buffer, 3mA, with Slew Rate Control	B3CR

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL

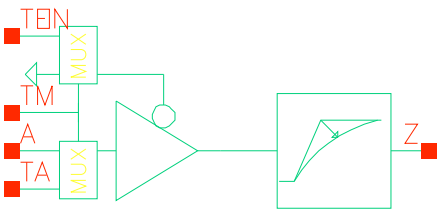
OUTPUT Pin	Max. load
Z	75.000 pF

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		18.75pF	37.50pF	56.25pF	75.00pF
A to Z	Fall delay	3.25	4.12	4.90	5.65
A to Z	Rise delay	3.41	4.40	5.30	6.17

CMOS035 MTC45200	CMOS Output Pad Buffer, 3mA, with Slew Rate Control, with Test Pins	B3CRP

SYMBOL



BEHAVIOUR

A	TM	TEN	TA	Z
-	1	0	1	1
1	0	-	-	1
-	1	1	-	Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
Z	3.492 pF

OUTPUT Pin	Max. load
Z	75.000 pF

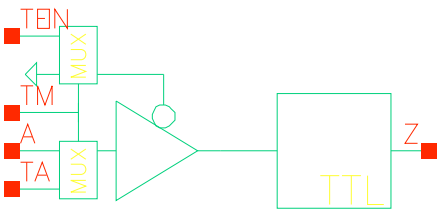
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
TEN to Z	0Z delay	1.26	1.30	1.50
TEN to Z	1Z delay	1.55	1.59	1.79
TM to Z	0Z delay	1.66	1.73	1.94
TM to Z	1Z delay	1.96	2.02	2.24

Timing/Load		18.75pF	37.50pF	56.25pF	75.00pF
A to Z	Fall delay	3.30	4.18	4.96	5.70
A to Z	Rise delay	3.48	4.47	5.38	6.25
TA to Z	Fall delay	3.64	4.51	5.29	6.04
TA to Z	Rise delay	3.76	4.75	5.65	6.52
TEN to Z	Z0 delay	3.58	4.45	5.23	5.98
TEN to Z	Z1 delay	3.73	4.72	5.62	6.50
TM to Z	Fall delay	3.81	4.68	5.47	6.22
TM to Z	Fall delay	3.64	4.51	5.30	6.05
TM to Z	Rise delay	4.19	5.18	6.08	6.95
TM to Z	Rise delay	3.65	4.64	5.54	6.41
TM to Z	Z0 delay	3.63	4.50	5.29	6.04
TM to Z	Z1 delay	3.77	4.76	5.66	6.53

CMOS035 MTC45200	TTL Output Pad Buffer, 3mA, with Test Pins	B3P

SYMBOL



BEHAVIOUR

A	TM	TEN	TA	Z
-	1	0	1	1
1	0	-	-	1
-	1	1	-	Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
Z	3.620 pF

OUTPUT Pin	Max. load
Z	75.000 pF

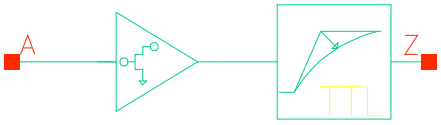
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
TEN to Z	0Z delay	1.26	1.30	1.50
TEN to Z	1Z delay	1.55	1.59	1.79
TM to Z	0Z delay	1.66	1.73	1.94
TM to Z	1Z delay	1.96	2.02	2.23

Timing/Load		18.75pF	37.50pF	56.25pF	75.00pF
A to Z	Fall delay	2.53	3.39	4.22	5.03
A to Z	Rise delay	2.34	3.08	3.80	4.51
TA to Z	Fall delay	2.86	3.73	4.55	5.37
TA to Z	Rise delay	2.61	3.36	4.07	4.79
TEN to Z	Z0 delay	2.79	3.65	4.48	5.29
TEN to Z	Z1 delay	2.58	3.33	4.05	4.76
TM to Z	Fall delay	3.04	3.90	4.73	5.54
TM to Z	Fall delay	2.87	3.73	4.56	5.37
TM to Z	Rise delay	3.04	3.79	4.51	5.22
TM to Z	Rise delay	2.50	3.25	3.97	4.68
TM to Z	Z0 delay	2.84	3.70	4.53	5.34
TM to Z	Z1 delay	2.62	3.37	4.08	4.79

CMOS035 MTC45200	TTL Open Drain Output Pad Buffer, 3mA, with Slew Rate Control	B3ROD

SYMBOL



BEHAVIOUR

A	Z
0	0
1	Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
Z	2.077 pF

OUTPUT Pin	Max. load
Z	75.000 pF

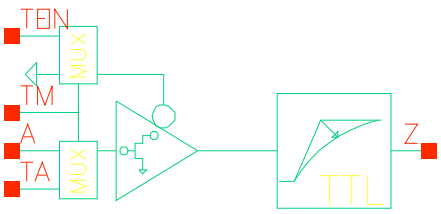
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
A to Z	0Z delay	0.94	1.00	1.17

Timing/Load		18.75pF	37.50pF	56.25pF	75.00pF
A to Z	Z0 delay	4.16	5.57	6.87	8.13

CMOS035 MTC45200	TTL Open Drain Output Pad Buffer, 3mA, with Slew Rate Control, with Test Pins	B3RODP

SYMBOL



BEHAVIOUR

A	TM	TEN	TA	Z
1	0	-	-	Z
-	1	0	0	0
0	0	-	-	0
-	1	1	-	Z
-	1	-	1	Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
Z	2.734 pF

OUTPUT Pin	Max. load
Z	75.000 pF

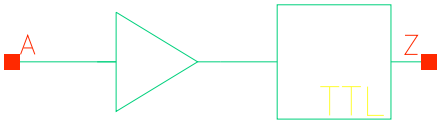
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
A to Z	0Z delay	0.87	0.93	1.10
TA to Z	0Z delay	1.12	1.16	1.36
TEN to Z	0Z delay	1.25	1.29	1.49
TM to Z	0Z delay	1.43	1.50	1.71

Timing/Load		18.75pF	37.50pF	56.25pF	75.00pF
A to Z	Z0 delay	3.38	4.38	5.27	6.13
TA to Z	Z0 delay	3.70	4.69	5.59	6.45
TEN to Z	Z0 delay	3.69	4.69	5.58	6.44
TM to Z	Z0 delay	3.88	4.87	5.76	6.62
TM to Z	Z0 delay	3.74	4.74	5.64	6.50

CMOS035 MTC45200	TTL Output Pad Buffer, 4mA	B4

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL

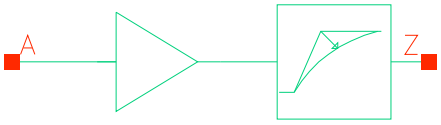
OUTPUT Pin	Max. load
Z	100.000 pF

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to Z	Fall delay	2.55	3.43	4.26	5.08
A to Z	Rise delay	2.21	2.96	3.67	4.38

CMOS035 MTC45200	CMOS Output Pad Buffer, 4mA, with Slew Rate Control	B4CR

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL

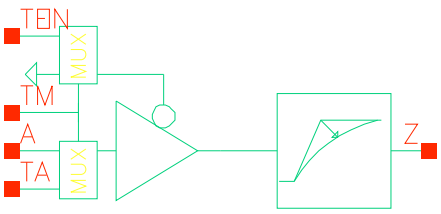
OUTPUT Pin	Max. load
Z	100.000 pF

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to Z	Fall delay	3.41	4.31	5.11	5.87
A to Z	Rise delay	3.34	4.33	5.23	6.10

CMOS035 MTC45200	CMOS Output Pad Buffer, 4mA, with Slew Rate Control, with Test Pins	B4CRP

SYMBOL



BEHAVIOUR

A	TM	TEN	TA	Z
-	1	0	1	1
1	0	-	-	1
-	1	1	-	Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
Z	3.633 pF

OUTPUT Pin	Max. load
Z	100.000 pF

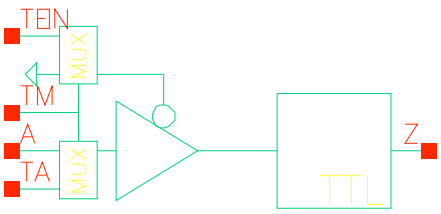
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
TEN to Z	0Z delay	1.31	1.35	1.56
TEN to Z	1Z delay	1.54	1.58	1.77
TM to Z	0Z delay	1.72	1.78	2.00
TM to Z	1Z delay	1.94	2.01	2.22

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to Z	Fall delay	3.47	4.37	5.17	5.93
A to Z	Rise delay	3.42	4.41	5.31	6.18
TA to Z	Fall delay	3.80	4.70	5.50	6.26
TA to Z	Rise delay	3.69	4.68	5.58	6.46
TEN to Z	Z0 delay	3.74	4.64	5.45	6.21
TEN to Z	Z1 delay	3.67	4.66	5.56	6.43
TM to Z	Fall delay	3.98	4.88	5.68	6.44
TM to Z	Fall delay	3.81	4.71	5.51	6.27
TM to Z	Rise delay	4.12	5.11	6.02	6.89
TM to Z	Rise delay	3.58	4.57	5.48	6.35
TM to Z	Z0 delay	3.79	4.70	5.50	6.26
TM to Z	Z1 delay	3.70	4.69	5.60	6.47

CMOS035 MTC45200	TTL Output Pad Buffer, 4mA, with Test Pins	B4P

SYMBOL



BEHAVIOUR

A	TM	TEN	TA	Z
-	1	0	1	1
1	0	-	-	1
-	1	1	-	Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
Z	3.754 pF

OUTPUT Pin	Max. load
Z	100.000 pF

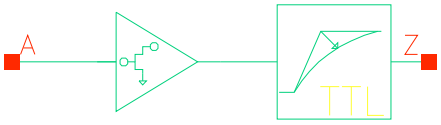
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
TEN to Z	0Z delay	1.31	1.35	1.56
TEN to Z	1Z delay	1.53	1.58	1.77
TM to Z	0Z delay	1.72	1.78	2.00
TM to Z	1Z delay	1.94	2.01	2.22

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to Z	Fall delay	2.61	3.49	4.32	5.14
A to Z	Rise delay	2.29	3.04	3.76	4.47
TA to Z	Fall delay	2.94	3.82	4.65	5.47
TA to Z	Rise delay	2.57	3.31	4.03	4.74
TEN to Z	Z0 delay	2.87	3.74	4.58	5.40
TEN to Z	Z1 delay	2.54	3.28	4.00	4.71
TM to Z	Fall delay	3.12	4.00	4.83	5.65
TM to Z	Fall delay	2.94	3.82	4.66	5.48
TM to Z	Rise delay	3.00	3.74	4.46	5.17
TM to Z	Rise delay	2.46	3.20	3.92	4.63
TM to Z	Z0 delay	2.92	3.79	4.63	5.45
TM to Z	Z1 delay	2.57	3.32	4.03	4.74

CMOS035 MTC45200	TTL Open Drain Output Pad Buffer, 4mA, with Slew Rate Control	B4ROD

SYMBOL



BEHAVIOUR

A	Z
0	0
1	Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
Z	2.732 pF

OUTPUT Pin	Max. load
Z	100.000 pF

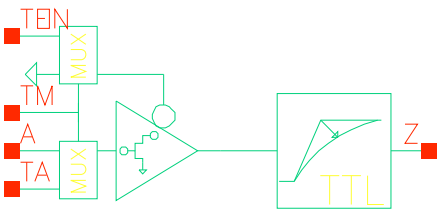
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
A to Z	0Z delay	0.92	0.98	1.15

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to Z	Z0 delay	3.49	4.51	5.43	6.30

CMOS035 MTC45200	TTL Open Drain Output Pad Buffer, 4mA, with Slew Rate Control, with Test Pins	B4RODP

SYMBOL



BEHAVIOUR

A	TM	TEN	TA	Z
1	0	-	-	Z
-	1	0	0	0
0	0	-	-	0
-	1	1	-	Z
-	1	-	1	Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
Z	2.732 pF

OUTPUT Pin	Max. load
Z	100.000 pF

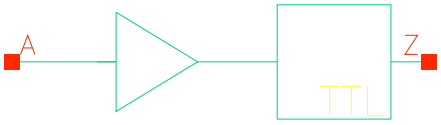
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
A to Z	0Z delay	0.93	0.98	1.16
TA to Z	0Z delay	1.22	1.26	1.47
TEN to Z	0Z delay	1.31	1.35	1.55
TM to Z	0Z delay	1.71	1.78	2.00

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to Z	Z0 delay	3.55	4.57	5.48	6.35
TA to Z	Z0 delay	3.86	4.88	5.80	6.67
TEN to Z	Z0 delay	3.86	4.88	5.79	6.67
TM to Z	Z0 delay	4.04	5.06	5.98	6.85
TM to Z	Z0 delay	3.91	4.93	5.85	6.72

CMOS035 MTC45200	TTL Output Pad Buffer, 6mA	B6

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL

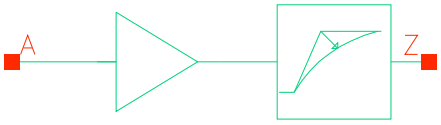
OUTPUT Pin	Max. load
Z	150.000 pF

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		37.50pF	75.00pF	112.50pF	150.00pF
A to Z	Fall delay	2.48	3.36	4.19	5.01
A to Z	Rise delay	2.17	2.91	3.63	4.34

CMOS035 MTC45200	CMOS Output Pad Buffer, 6mA, with Slew Rate Control	B6CR

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL

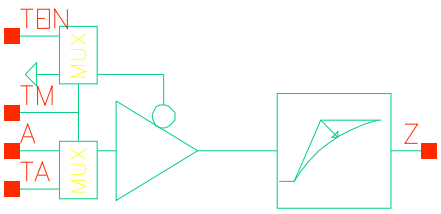
OUTPUT Pin	Max. load
Z	150.000 pF

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		37.50pF	75.00pF	112.50pF	150.00pF
A to Z	Fall delay	3.30	4.20	4.99	5.75
A to Z	Rise delay	3.28	4.26	5.16	6.03

CMOS035 MTC45200	CMOS Output Pad Buffer, 6mA, with Slew Rate Control, with Test Pins	B6CRP

SYMBOL



BEHAVIOUR

A	TM	TEN	TA	Z
-	1	0	1	1
1	0	-	-	1
-	1	1	-	Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
Z	4.453 pF

OUTPUT Pin	Max. load
Z	150.000 pF

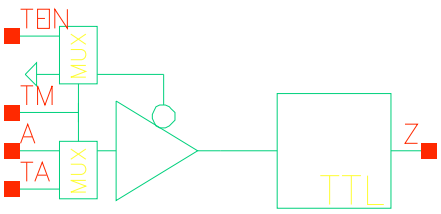
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
TEN to Z	0Z delay	1.29	1.33	1.54
TEN to Z	1Z delay	1.50	1.54	1.74
TM to Z	0Z delay	1.70	1.76	1.98
TM to Z	1Z delay	1.91	1.97	2.19

Timing/Load		37.50pF	75.00pF	112.50pF	150.00pF
A to Z	Fall delay	3.36	4.25	5.05	5.80
A to Z	Rise delay	3.35	4.34	5.24	6.11
TA to Z	Fall delay	3.69	4.58	5.38	6.14
TA to Z	Rise delay	3.63	4.61	5.51	6.38
TEN to Z	Z0 delay	3.63	4.53	5.32	6.08
TEN to Z	Z1 delay	3.60	4.59	5.49	6.35
TM to Z	Fall delay	3.87	4.76	5.56	6.31
TM to Z	Fall delay	3.70	4.59	5.39	6.15
TM to Z	Rise delay	4.06	5.04	5.94	6.81
TM to Z	Rise delay	3.52	4.50	5.40	6.27
TM to Z	Z0 delay	3.69	4.58	5.38	6.14
TM to Z	Z1 delay	3.64	4.62	5.52	6.39

CMOS035 MTC45200	TTL Output Pad Buffer, 6mA, with Test Pins	B6P

SYMBOL



BEHAVIOUR

A	TM	TEN	TA	Z
-	1	0	1	1
1	0	-	-	1
-	1	1	-	Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
Z	4.625 pF

OUTPUT Pin	Max. load
Z	150.000 pF

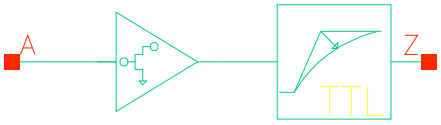
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
TEN to Z	0Z delay	1.29	1.33	1.54
TEN to Z	1Z delay	1.50	1.54	1.74
TM to Z	0Z delay	1.70	1.76	1.98
TM to Z	1Z delay	1.91	1.97	2.18

Timing/Load		37.50pF	75.00pF	112.50pF	150.00pF
A to Z	Fall delay	2.54	3.41	4.25	5.06
A to Z	Rise delay	2.25	2.99	3.71	4.42
TA to Z	Fall delay	2.87	3.75	4.58	5.40
TA to Z	Rise delay	2.52	3.27	3.98	4.69
TEN to Z	Z0 delay	2.79	3.67	4.50	5.32
TEN to Z	Z1 delay	2.49	3.24	3.95	4.66
TM to Z	Fall delay	3.04	3.92	4.76	5.57
TM to Z	Fall delay	2.87	3.75	4.58	5.40
TM to Z	Rise delay	2.95	3.70	4.41	5.12
TM to Z	Rise delay	2.41	3.16	3.88	4.59
TM to Z	Z0 delay	2.84	3.72	4.55	5.37
TM to Z	Z1 delay	2.53	3.27	3.99	4.70

CMOS035 MTC45200	TTL Open Drain Output Pad Buffer, 6mA, with Slew Rate Control	B6ROD

SYMBOL



BEHAVIOUR

A	Z
0	0
1	Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
Z	3.388 pF

OUTPUT Pin	Max. load
Z	150.000 pF

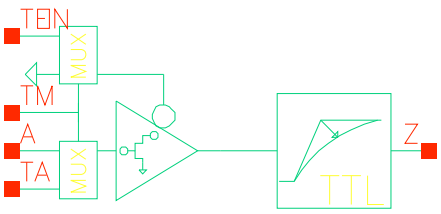
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
A to Z	0Z delay	0.90	0.96	1.13

Timing/Load		37.50pF	75.00pF	112.50pF	150.00pF
A to Z	Z0 delay	3.39	4.40	5.31	6.18

CMOS035 MTC45200	TTL Open Drain Output Pad Buffer, 6mA, with Slew Rate Control, with Test Pins	B6RODP

SYMBOL



BEHAVIOUR

A	TM	TEN	TA	Z
1	0	-	-	Z
-	1	0	0	0
0	0	-	-	0
-	1	1	-	Z
-	1	-	1	Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
Z	3.388 pF

OUTPUT Pin	Max. load
Z	150.000 pF

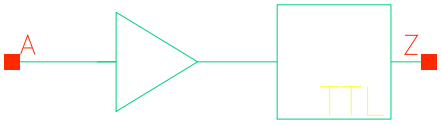
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
A to Z	0Z delay	0.91	0.96	1.14
TA to Z	0Z delay	1.20	1.24	1.44
TEN to Z	0Z delay	1.29	1.33	1.53
TM to Z	0Z delay	1.69	1.76	1.98

Timing/Load		37.50pF	75.00pF	112.50pF	150.00pF
A to Z	Z0 delay	3.44	4.46	5.37	6.23
TA to Z	Z0 delay	3.76	4.77	5.68	6.55
TEN to Z	Z0 delay	3.75	4.77	5.68	6.55
TM to Z	Z0 delay	3.94	4.95	5.86	6.73
TM to Z	Z0 delay	3.81	4.82	5.73	6.60

CMOS035 MTC45200	TTL Output Pad Buffer, 8mA	B8

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL

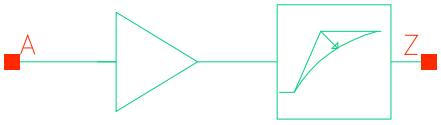
OUTPUT Pin	Max. load
Z	200.000 pF

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to Z	Fall delay	2.42	3.29	4.12	4.94
A to Z	Rise delay	2.14	2.88	3.59	4.30

CMOS035 MTC45200	CMOS Output Pad Buffer, 8mA, with Slew Rate Control	B8CR

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL

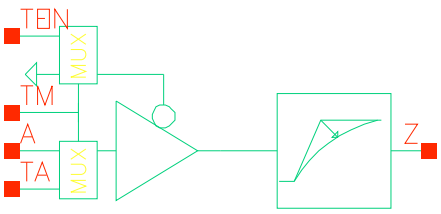
OUTPUT Pin	Max. load
Z	200.000 pF

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to Z	Fall delay	3.21	4.09	4.88	5.63
A to Z	Rise delay	3.23	4.20	5.10	5.97

CMOS035 MTC45200	CMOS Output Pad Buffer, 8mA, with Slew Rate Control, with Test Pins	B8CRP

SYMBOL



BEHAVIOUR

A	TM	TEN	TA	Z
-	1	0	1	1
1	0	-	-	1
-	1	1	-	Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
Z	5.273 pF

OUTPUT Pin	Max. load
Z	200.000 pF

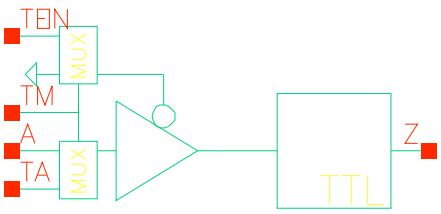
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
TEN to Z	0Z delay	1.27	1.31	1.51
TEN to Z	1Z delay	1.47	1.51	1.70
TM to Z	0Z delay	1.68	1.74	1.96
TM to Z	1Z delay	1.88	1.94	2.15

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to Z	Fall delay	3.26	4.14	4.93	5.69
A to Z	Rise delay	3.30	4.28	5.17	6.04
TA to Z	Fall delay	3.60	4.48	5.27	6.02
TA to Z	Rise delay	3.57	4.55	5.45	6.32
TEN to Z	Z0 delay	3.54	4.42	5.21	5.97
TEN to Z	Z1 delay	3.55	4.53	5.42	6.29
TM to Z	Fall delay	3.77	4.65	5.44	6.20
TM to Z	Fall delay	3.60	4.48	5.28	6.03
TM to Z	Rise delay	4.01	4.98	5.88	6.75
TM to Z	Rise delay	3.47	4.45	5.34	6.21
TM to Z	Z0 delay	3.59	4.47	5.27	6.02
TM to Z	Z1 delay	3.59	4.57	5.46	6.33

CMOS035 MTC45200	TTL Output Pad Buffer, 8mA, with Test Pins	B8P

SYMBOL



BEHAVIOUR

A	TM	TEN	TA	Z
-	1	0	1	1
1	0	-	-	1
-	1	1	-	Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
Z	5.500 pF

OUTPUT Pin	Max. load
Z	200.000 pF

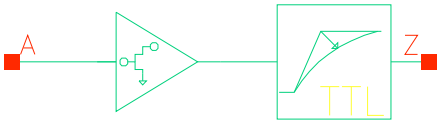
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
TEN to Z	0Z delay	1.27	1.31	1.51
TEN to Z	1Z delay	1.47	1.51	1.70
TM to Z	0Z delay	1.67	1.74	1.96
TM to Z	1Z delay	1.87	1.94	2.15

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to Z	Fall delay	2.47	3.35	4.18	5.00
A to Z	Rise delay	2.22	2.96	3.67	4.38
TA to Z	Fall delay	2.81	3.68	4.52	5.33
TA to Z	Rise delay	2.49	3.23	3.95	4.66
TEN to Z	Z0 delay	2.73	3.61	4.44	5.26
TEN to Z	Z1 delay	2.46	3.20	3.92	4.63
TM to Z	Fall delay	2.98	3.86	4.69	5.51
TM to Z	Fall delay	2.81	3.69	4.52	5.34
TM to Z	Rise delay	2.92	3.66	4.38	5.09
TM to Z	Rise delay	2.38	3.12	3.84	4.55
TM to Z	Z0 delay	2.78	3.66	4.49	5.31
TM to Z	Z1 delay	2.50	3.24	3.95	4.66

CMOS035 MTC45200	TTL Open Drain Output Pad Buffer, 8mA, with Slew Rate Control	B8ROD

SYMBOL



BEHAVIOUR

A	Z
0	0
1	Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
Z	4.047 pF

OUTPUT Pin	Max. load
Z	200.000 pF

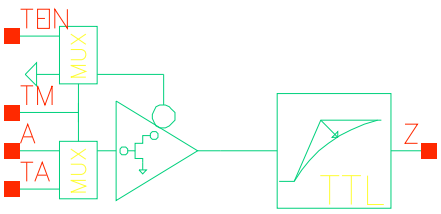
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
A to Z	0Z delay	0.88	0.94	1.11

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to Z	Z0 delay	3.29	4.30	5.20	6.06

CMOS035 MTC45200	TTL Open Drain Output Pad Buffer, 8mA, with Slew Rate Control, with Test Pins	B8RODP

SYMBOL



BEHAVIOUR

A	TM	TEN	TA	Z
1	0	-	-	Z
-	1	0	0	0
0	0	-	-	0
-	1	1	-	Z
-	1	-	1	Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
Z	4.047 pF

OUTPUT Pin	Max. load
Z	200.000 pF

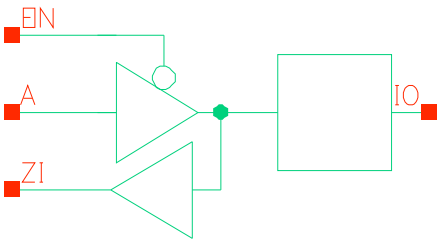
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
A to Z	0Z delay	0.88	0.94	1.11
TA to Z	0Z delay	1.18	1.22	1.42
TEN to Z	0Z delay	1.27	1.31	1.51
TM to Z	0Z delay	1.67	1.74	1.95

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to Z	Z0 delay	3.35	4.35	5.26	6.12
TA to Z	Z0 delay	3.67	4.67	5.57	6.44
TEN to Z	Z0 delay	3.66	4.66	5.57	6.43
TM to Z	Z0 delay	3.84	4.84	5.75	6.61
TM to Z	Z0 delay	3.71	4.71	5.62	6.49

CMOS035 MTC45200	CMOS Bidir Pad Buffer, 2mA	BD2C

SYMBOL



BEHAVIOUR

A	EN	IO	ZI	IO
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
IO	2.965 pF

OUTPUT Pin	Max. load
IO	50.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

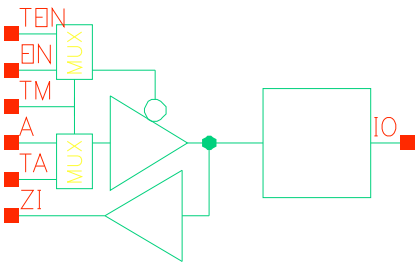
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.19	0.26	0.33	0.47
IO to ZI	Rise delay	0.19	0.28	0.37	0.54

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.08	1.13	1.29
EN to IO	1Z delay	1.35	1.40	1.54

Timing/Load		12.50pF	25.00pF	37.50pF	50.00pF
A to IO	Fall delay	2.57	3.34	4.06	4.77
A to IO	Rise delay	2.58	3.45	4.30	5.15
EN to IO	Z0 delay	2.53	3.30	4.02	4.72
EN to IO	Z1 delay	2.53	3.40	4.25	5.10

CMOS035 MTC45200	CMOS Bidir Pad Buffer, 2mA, with Test Pins	BD2CP

SYMBOL



BEHAVIOUR

A	EN	IO	TM	TEN	TA	ZI	IO
-	-	1	1	1	-	1	
-	-	-	1	0	-	-	
-	1	1	0	-	-	1	
-	0	-	0	-	-	-	
-	-	-	1	0	1		1
-	-	-	1	1	-		Z
1	0	-	0	-	-		1
-	1	-	0	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
IO	2.965 pF
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL

OUTPUT Pin	Max. load
IO	50.000 pF
ZI	81 SL

CMOS035 MTC45200	CMOS Bidir Pad Buffer, 2mA, with Test Pins	BD2CP

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

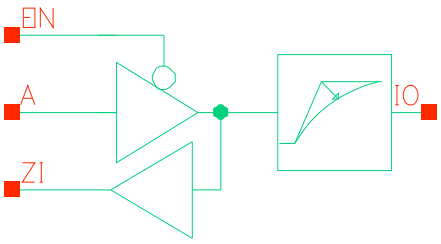
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.19	0.26	0.33	0.47
IO to ZI	Rise delay	0.19	0.28	0.37	0.54

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.08	1.13	1.29
EN to IO	1Z delay	1.35	1.40	1.54
TEN to IO	0Z delay	1.34	1.38	1.58
TEN to IO	1Z delay	1.57	1.61	1.81
TM to IO	0Z delay	1.74	1.81	2.02
TM to IO	1Z delay	1.98	2.04	2.26

Timing/Load		12.50pF	25.00pF	37.50pF	50.00pF
A to IO	Fall delay	2.57	3.34	4.06	4.77
A to IO	Rise delay	2.58	3.45	4.30	5.15
EN to IO	Z0 delay	2.53	3.30	4.02	4.72
EN to IO	Z1 delay	2.53	3.40	4.25	5.10
TA to IO	Fall delay	2.91	3.67	4.40	5.10
TA to IO	Rise delay	2.85	3.72	4.58	5.42
TEN to IO	Z0 delay	2.85	3.61	4.33	5.04
TEN to IO	Z1 delay	2.84	3.71	4.56	5.41
TM to IO	Fall delay	3.08	3.85	4.57	5.28
TM to IO	Fall delay	2.91	3.68	4.40	5.11
TM to IO	Rise delay	3.28	4.16	5.01	5.86
TM to IO	Rise delay	2.74	3.62	4.47	5.32
TM to IO	Z0 delay	3.11	3.88	4.60	5.31
TM to IO	Z0 delay	2.88	3.65	4.37	5.08
TM to IO	Z1 delay	3.23	4.10	4.95	5.80
TM to IO	Z1 delay	2.86	3.73	4.58	5.43

CMOS035 MTC45200	CMOS Bidir Pad Buffer, 2mA, with Slew Rate Control	BD2CR

SYMBOL



BEHAVIOUR

A	EN	IO	ZI	IO
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
IO	2.965 pF

OUTPUT Pin	Max. load
IO	50.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

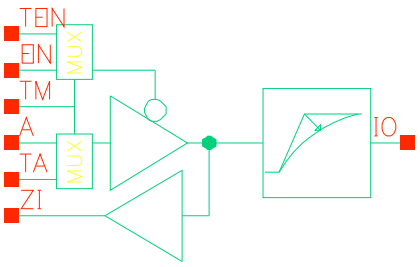
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.19	0.26	0.33	0.47
IO to ZI	Rise delay	0.19	0.28	0.37	0.54

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.08	1.13	1.29
EN to IO	1Z delay	1.35	1.40	1.55

Timing/Load		12.50pF	25.00pF	37.50pF	50.00pF
A to IO	Fall delay	3.64	4.54	5.34	6.10
A to IO	Rise delay	3.56	4.55	5.45	6.32
EN to IO	Z0 delay	3.62	4.52	5.32	6.08
EN to IO	Z1 delay	3.52	4.50	5.40	6.28

CMOS035 MTC45200	CMOS Bidir Pad Buffer, 2mA, with Slew Rate Control, with Test Pins	BD2CRP

SYMBOL



BEHAVIOUR

A	EN	IO	TM	TEN	TA	ZI	IO
-	-	1	1	1	-	1	
-	-	-	1	0	-	-	
-	1	1	0	-	-	1	
-	0	-	0	-	-	-	
-	-	-	1	0	1		1
-	-	-	1	1	-		Z
1	0	-	0	-	-		1
-	1	-	0	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
IO	2.965 pF
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL

OUTPUT Pin	Max. load
IO	50.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

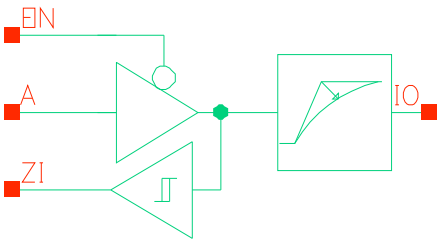
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.19	0.26	0.33	0.47
IO to ZI	Rise delay	0.19	0.28	0.37	0.54

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.08	1.13	1.29
EN to IO	1Z delay	1.35	1.40	1.55
TEN to IO	0Z delay	1.34	1.38	1.58
TEN to IO	1Z delay	1.57	1.61	1.81
TM to IO	0Z delay	1.74	1.81	2.02
TM to IO	1Z delay	1.98	2.05	2.26

Timing/Load		12.50pF	25.00pF	37.50pF	50.00pF
A to IO	Fall delay	3.64	4.54	5.34	6.10
A to IO	Rise delay	3.56	4.55	5.45	6.32
EN to IO	Z0 delay	3.62	4.52	5.32	6.08
EN to IO	Z1 delay	3.52	4.50	5.40	6.28
TA to IO	Fall delay	3.98	4.88	5.68	6.44
TA to IO	Rise delay	3.84	4.82	5.72	6.59
TEN to IO	Z0 delay	3.93	4.83	5.63	6.39
TEN to IO	Z1 delay	3.83	4.81	5.71	6.59
TM to IO	Fall delay	4.15	5.05	5.85	6.61
TM to IO	Fall delay	3.98	4.88	5.69	6.45
TM to IO	Rise delay	4.27	5.25	6.15	7.03
TM to IO	Rise delay	3.73	4.71	5.62	6.49
TM to IO	Z0 delay	4.20	5.10	5.90	6.66
TM to IO	Z0 delay	3.97	4.87	5.68	6.44
TM to IO	Z1 delay	4.22	5.20	6.10	6.98
TM to IO	Z1 delay	3.85	4.83	5.74	6.61

CMOS035 MTC45200	CMOS Schmitt Trigger Bidir Pad Buffer, 2mA, with Slew Rate Control	BD2SCR

SYMBOL



BEHAVIOUR

A	EN	IO	ZI	IO
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
IO	2.972 pF

OUTPUT Pin	Max. load
IO	50.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

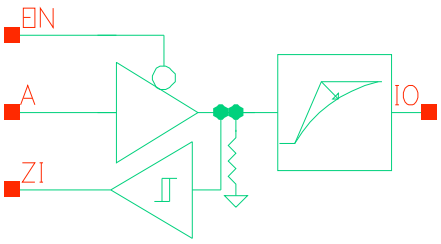
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.45	0.55	0.63	0.78
IO to ZI	Rise delay	0.42	0.52	0.61	0.78

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.08	1.13	1.29
EN to IO	1Z delay	1.35	1.40	1.55

Timing/Load		12.50pF	25.00pF	37.50pF	50.00pF
A to IO	Fall delay	3.65	4.55	5.35	6.11
A to IO	Rise delay	3.56	4.55	5.45	6.32
EN to IO	Z0 delay	3.62	4.52	5.32	6.08
EN to IO	Z1 delay	3.52	4.51	5.41	6.28

CMOS035 MTC45200	CMOS Schmitt Trigger Bidir Pad Buffer with Active Pull-Down, 2mA, with Slew Rate Control	BD2SCRD

SYMBOL



BEHAVIOUR

A	EN	IO	ZI	IO
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
IO	2.980 pF

OUTPUT Pin	Max. load
IO	50.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

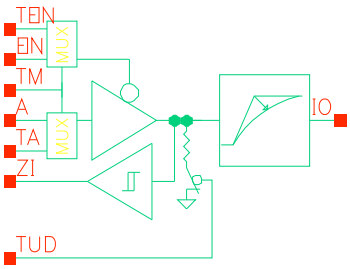
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.45	0.56	0.64	0.79
IO to ZI	Rise delay	0.43	0.53	0.62	0.79

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.09	1.14	1.30
EN to IO	1Z delay	1.32	1.37	1.52

Timing/Load		12.50pF	25.00pF	37.50pF	50.00pF
A to IO	Fall delay	3.64	4.54	5.33	6.09
A to IO	Rise delay	3.57	4.55	5.46	6.33
EN to IO	Z0 delay	3.60	4.50	5.30	6.06
EN to IO	Z1 delay	3.52	4.51	5.41	6.29

CMOS035 MTC45200	CMOS Schmitt Trigger Bidir Pad Buffer with Active Pull-Down, 2mA, with Slew Rate Control, with Test Pins	BD2SCRDQP

SYMBOL



BEHAVIOUR

A	EN	IO	TM	TEN	TA	TUD	ZI	IO
-	-	1	1	1	-	-	1	
-	-	-	1	0	-	-	-	
-	1	1	0	-	-	-	1	
-	0	-	0	-	-	-	-	
-	-	-	1	0	1	-		1
-	-	-	1	1	-	-		Z
1	0	-	0	-	-	-		1
-	1	-	0	-	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
IO	2.978 pF
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
TUD	1.9 SL

OUTPUT Pin	Max. load
IO	50.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

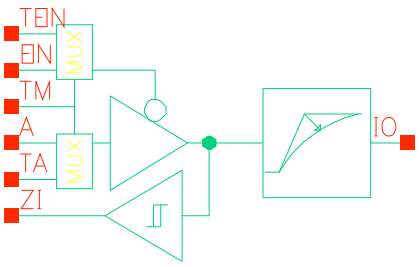
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.45	0.56	0.64	0.79
IO to ZI	Rise delay	0.43	0.53	0.62	0.79

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.09	1.14	1.30
EN to IO	1Z delay	1.35	1.40	1.55
TEN to IO	0Z delay	1.35	1.39	1.59
TEN to IO	1Z delay	1.57	1.61	1.81
TM to IO	0Z delay	1.75	1.82	2.04
TM to IO	1Z delay	1.97	2.04	2.24

Timing/Load		12.50pF	25.00pF	37.50pF	50.00pF
A to IO	Fall delay	3.65	4.55	5.35	6.11
A to IO	Rise delay	3.57	4.55	5.46	6.33
EN to IO	Z0 delay	3.62	4.52	5.32	6.08
EN to IO	Z1 delay	3.52	4.51	5.41	6.29
TA to IO	Fall delay	3.98	4.88	5.68	6.44
TA to IO	Rise delay	3.84	4.83	5.73	6.60
TEN to IO	Z0 delay	3.94	4.84	5.64	6.40
TEN to IO	Z1 delay	3.83	4.82	5.72	6.60
TM to IO	Fall delay	4.16	5.06	5.86	6.62
TM to IO	Fall delay	3.99	4.89	5.69	6.45
TM to IO	Rise delay	4.27	5.26	6.16	7.04
TM to IO	Rise delay	3.74	4.72	5.62	6.50
TM to IO	Z0 delay	4.21	5.11	5.91	6.67
TM to IO	Z0 delay	3.97	4.88	5.68	6.44
TM to IO	Z1 delay	4.22	5.21	6.11	6.99
TM to IO	Z1 delay	3.86	4.84	5.75	6.62

CMOS035 MTC45200	CMOS Schmitt Trigger Bidir Pad Buffer, 2mA, with Slew Rate Control, with Test Pins	BD2SCRP

SYMBOL



BEHAVIOUR

A	EN	IO	TM	TEN	TA	ZI	IO
-	-	1	1	1	-	1	
-	-	-	1	0	-	-	
-	1	1	0	-	-	1	
-	0	-	0	-	-	-	
-	-	-	1	0	1		1
-	-	-	1	1	-		Z
1	0	-	0	-	-		1
-	1	-	0	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
IO	2.972 pF
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL

OUTPUT Pin	Max. load
IO	50.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

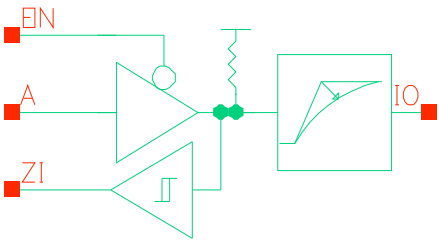
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.45	0.55	0.63	0.78
IO to ZI	Rise delay	0.42	0.52	0.61	0.78

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.08	1.13	1.29
EN to IO	1Z delay	1.35	1.40	1.55
TEN to IO	0Z delay	1.34	1.38	1.58
TEN to IO	1Z delay	1.57	1.61	1.81
TM to IO	0Z delay	1.74	1.81	2.02
TM to IO	1Z delay	1.97	2.04	2.24

Timing/Load		12.50pF	25.00pF	37.50pF	50.00pF
A to IO	Fall delay	3.65	4.55	5.35	6.11
A to IO	Rise delay	3.56	4.55	5.45	6.32
EN to IO	Z0 delay	3.62	4.52	5.32	6.08
EN to IO	Z1 delay	3.52	4.51	5.41	6.28
TA to IO	Fall delay	3.98	4.88	5.68	6.44
TA to IO	Rise delay	3.84	4.82	5.73	6.60
TEN to IO	Z0 delay	3.94	4.84	5.64	6.40
TEN to IO	Z1 delay	3.83	4.82	5.72	6.59
TM to IO	Fall delay	4.16	5.06	5.86	6.62
TM to IO	Fall delay	3.99	4.89	5.69	6.45
TM to IO	Rise delay	4.27	5.26	6.16	7.03
TM to IO	Rise delay	3.73	4.72	5.62	6.49
TM to IO	Z0 delay	4.21	5.11	5.91	6.67
TM to IO	Z0 delay	3.97	4.88	5.68	6.44
TM to IO	Z1 delay	4.22	5.21	6.11	6.98
TM to IO	Z1 delay	3.85	4.84	5.74	6.61

CMOS035 MTC45200	CMOS Schmitt Trigger Bidir Pad Buffer with Active Pull-Up, 2mA, with Slew Rate Control	BD2SCRU

SYMBOL



BEHAVIOUR

A	EN	IO	ZI	IO
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
IO	2.983 pF

OUTPUT Pin	Max. load
IO	50.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

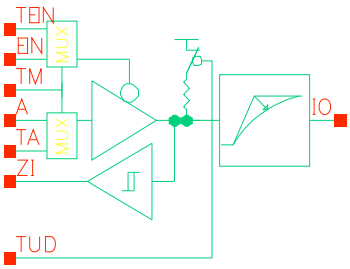
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.46	0.56	0.65	0.79
IO to ZI	Rise delay	0.43	0.53	0.61	0.79

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.07	1.12	1.28
EN to IO	1Z delay	1.39	1.44	1.58

Timing/Load		12.50pF	25.00pF	37.50pF	50.00pF
A to IO	Fall delay	3.65	4.55	5.35	6.11
A to IO	Rise delay	3.55	4.54	5.44	6.30
EN to IO	Z0 delay	3.63	4.53	5.33	6.09
EN to IO	Z1 delay	3.50	4.48	5.38	6.25

CMOS035 MTC45200	CMOS Schmitt Trigger Bidir Pad Buffer with Active Pull-Up, 2mA, with Slew Rate Control, with Test Pins	BD2SCRUQP

SYMBOL



BEHAVIOUR

A	EN	IO	TM	TEN	TA	TUD	ZI	IO
-	-	1	1	1	-	-	1	
-	-	-	1	0	-	-	-	
-	1	1	0	-	-	-	1	
-	0	-	0	-	-	-	-	
-	-	-	1	0	1	-		1
-	-	-	1	1	-	-		Z
1	0	-	0	-	-	-		1
-	1	-	0	-	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
IO	2.979 pF
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
TUD	2.3 SL

OUTPUT Pin	Max. load
IO	50.000 pF
ZI	81 SL

CMOS035 MTC45200	CMOS Schmitt Trigger Bidir Pad Buffer with Active Pull-Up, 2mA, with Slew Rate Control, with Test Pins	BD2SCRUQP

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

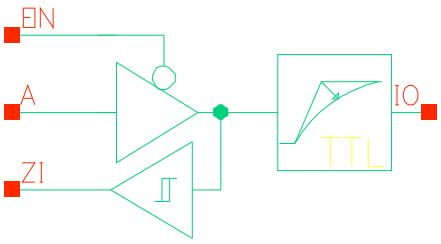
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.46	0.56	0.65	0.79
IO to ZI	Rise delay	0.43	0.53	0.61	0.79

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.08	1.13	1.29
EN to IO	1Z delay	1.39	1.44	1.58
TEN to IO	0Z delay	1.34	1.38	1.58
TEN to IO	1Z delay	1.61	1.65	1.84
TM to IO	0Z delay	1.74	1.81	2.02
TM to IO	1Z delay	2.00	2.07	2.27

Timing/Load		12.50pF	25.00pF	37.50pF	50.00pF
A to IO	Fall delay	3.65	4.55	5.35	6.11
A to IO	Rise delay	3.57	4.55	5.45	6.32
EN to IO	Z0 delay	3.63	4.53	5.33	6.09
EN to IO	Z1 delay	3.52	4.51	5.41	6.28
TA to IO	Fall delay	3.99	4.89	5.69	6.45
TA to IO	Rise delay	3.84	4.82	5.73	6.60
TEN to IO	Z0 delay	3.94	4.84	5.64	6.40
TEN to IO	Z1 delay	3.83	4.82	5.72	6.59
TM to IO	Fall delay	4.16	5.06	5.86	6.62
TM to IO	Fall delay	3.99	4.89	5.69	6.45
TM to IO	Rise delay	4.27	5.26	6.16	7.03
TM to IO	Rise delay	3.73	4.72	5.62	6.49
TM to IO	Z0 delay	4.21	5.11	5.91	6.67
TM to IO	Z0 delay	3.98	4.88	5.68	6.45
TM to IO	Z1 delay	4.22	5.21	6.11	6.98
TM to IO	Z1 delay	3.85	4.84	5.74	6.61

CMOS035 MTC45200	TTL Schmitt Trigger Bidir Pad Buffer, 2mA, with Slew Rate Control	BD2STR

SYMBOL



BEHAVIOUR

A	EN	IO	ZI	IO
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
IO	3.046 pF

OUTPUT Pin	Max. load
IO	50.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

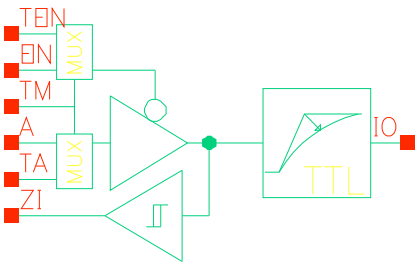
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.39	0.49	0.57	0.71
IO to ZI	Rise delay	0.36	0.45	0.54	0.71

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.08	1.13	1.29
EN to IO	1Z delay	1.35	1.40	1.55

Timing/Load		12.50pF	25.00pF	37.50pF	50.00pF
A to IO	Fall delay	3.84	4.85	5.76	6.63
A to IO	Rise delay	3.35	4.21	4.98	5.72
EN to IO	Z0 delay	3.82	4.83	5.74	6.61
EN to IO	Z1 delay	3.30	4.16	4.94	5.68

CMOS035 MTC45200	TTL Schmitt Trigger Bidir Pad Buffer, 2mA, with Slew Rate Control, with Test Pins	BD2STRP

SYMBOL



BEHAVIOUR

A	EN	IO	TM	TEN	TA	ZI	IO
-	-	1	1	1	-	1	
-	-	-	1	0	-	-	
-	1	1	0	-	-	1	
-	0	-	0	-	-	-	
-	-	-	1	0	1		1
-	-	-	1	1	-		Z
1	0	-	0	-	-		1
-	1	-	0	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
IO	3.046 pF
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL

OUTPUT Pin	Max. load
IO	50.000 pF
ZI	81 SL

CMOS035 MTC45200	TTL Schmitt Trigger Bidir Pad Buffer, 2mA, with Slew Rate Control, with Test Pins	BD2STRP

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

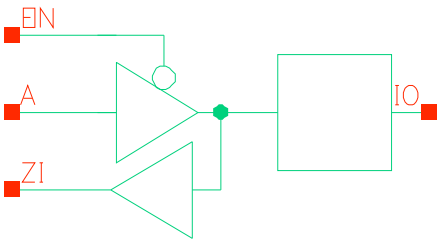
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.39	0.49	0.57	0.71
IO to ZI	Rise delay	0.36	0.45	0.54	0.71

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.08	1.13	1.29
EN to IO	1Z delay	1.35	1.40	1.55
TEN to IO	0Z delay	1.34	1.38	1.58
TEN to IO	1Z delay	1.57	1.61	1.81
TM to IO	0Z delay	1.74	1.81	2.02
TM to IO	1Z delay	1.98	2.05	2.26

Timing/Load		12.50pF	25.00pF	37.50pF	50.00pF
A to IO	Fall delay	3.84	4.85	5.76	6.63
A to IO	Rise delay	3.35	4.21	4.98	5.72
EN to IO	Z0 delay	3.82	4.83	5.74	6.61
EN to IO	Z1 delay	3.30	4.16	4.94	5.68
TA to IO	Fall delay	4.18	5.19	6.10	6.97
TA to IO	Rise delay	3.62	4.48	5.26	6.00
TEN to IO	Z0 delay	4.13	5.14	6.05	6.92
TEN to IO	Z1 delay	3.61	4.47	5.25	5.99
TM to IO	Fall delay	4.35	5.36	6.27	7.14
TM to IO	Fall delay	4.18	5.19	6.11	6.98
TM to IO	Rise delay	4.05	4.91	5.69	6.43
TM to IO	Rise delay	3.51	4.38	5.15	5.89
TM to IO	Z0 delay	4.40	5.41	6.33	7.20
TM to IO	Z0 delay	4.17	5.18	6.10	6.97
TM to IO	Z1 delay	4.00	4.86	5.64	6.38
TM to IO	Z1 delay	3.64	4.50	5.27	6.01

CMOS035 MTC45200	CMOS Bidir Pad Buffer, 4mA	BD4C

SYMBOL



BEHAVIOUR

A	EN	IO	ZI	IO
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
IO	3.787 pF

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

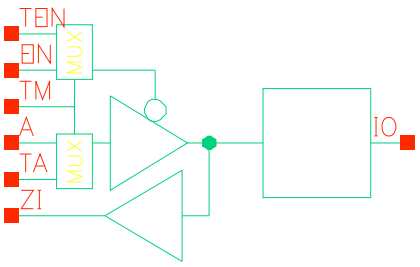
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.19	0.26	0.33	0.47
IO to ZI	Rise delay	0.19	0.28	0.37	0.54

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.06	1.11	1.27
EN to IO	1Z delay	1.31	1.36	1.51

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to IO	Fall delay	2.46	3.22	3.95	4.65
A to IO	Rise delay	2.47	3.35	4.20	5.05
EN to IO	Z0 delay	2.42	3.18	3.90	4.61
EN to IO	Z1 delay	2.42	3.30	4.15	5.00

CMOS035 MTC45200	CMOS Bidir Pad Buffer, 4mA, with Test Pins	BD4CP

SYMBOL



BEHAVIOUR

A	EN	IO	TM	TEN	TA	ZI	IO
-	-	1	1	1	-	1	
-	-	-	1	0	-	-	
-	1	1	0	-	-	1	
-	0	-	0	-	-	-	
-	-	-	1	0	1		1
-	-	-	1	1	-		Z
1	0	-	0	-	-		1
-	1	-	0	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
IO	3.787 pF
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	81 SL

CMOS035 MTC45200	CMOS Bidir Pad Buffer, 4mA, with Test Pins	BD4CP

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

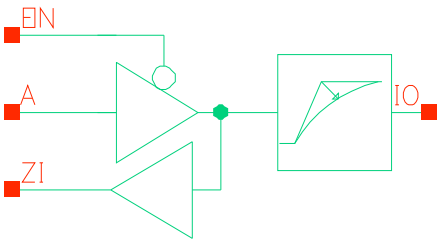
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.19	0.26	0.33	0.47
IO to ZI	Rise delay	0.19	0.28	0.37	0.54

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.06	1.11	1.27
EN to IO	1Z delay	1.31	1.36	1.51
TEN to IO	0Z delay	1.31	1.35	1.56
TEN to IO	1Z delay	1.54	1.58	1.77
TM to IO	0Z delay	1.72	1.78	2.00
TM to IO	1Z delay	1.94	2.01	2.22

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to IO	Fall delay	2.46	3.22	3.95	4.65
A to IO	Rise delay	2.47	3.35	4.20	5.05
EN to IO	Z0 delay	2.42	3.18	3.90	4.61
EN to IO	Z1 delay	2.42	3.30	4.15	5.00
TA to IO	Fall delay	2.79	3.56	4.28	4.99
TA to IO	Rise delay	2.75	3.62	4.47	5.32
TEN to IO	Z0 delay	2.73	3.50	4.22	4.92
TEN to IO	Z1 delay	2.73	3.61	4.46	5.31
TM to IO	Fall delay	2.97	3.73	4.46	5.16
TM to IO	Fall delay	2.80	3.56	4.29	4.99
TM to IO	Rise delay	3.18	4.05	4.91	5.75
TM to IO	Rise delay	2.64	3.51	4.37	5.21
TM to IO	Z0 delay	3.00	3.76	4.49	5.19
TM to IO	Z0 delay	2.77	3.53	4.26	4.96
TM to IO	Z1 delay	3.12	4.00	4.85	5.70
TM to IO	Z1 delay	2.75	3.63	4.48	5.33

CMOS035 MTC45200	CMOS Bidir Pad Buffer, 4mA, with Slew Rate Control	BD4CR

SYMBOL



BEHAVIOUR

A	EN	IO	ZI	IO
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
IO	3.787 pF

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

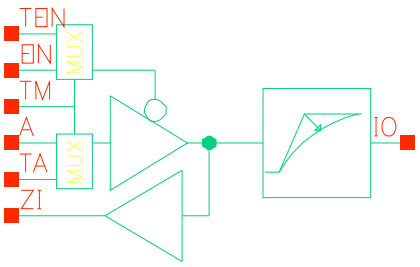
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.19	0.26	0.33	0.47
IO to ZI	Rise delay	0.19	0.28	0.37	0.54

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.06	1.11	1.27
EN to IO	1Z delay	1.32	1.36	1.51

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to IO	Fall delay	3.48	4.38	5.17	5.93
A to IO	Rise delay	3.43	4.42	5.32	6.19
EN to IO	Z0 delay	3.45	4.35	5.15	5.91
EN to IO	Z1 delay	3.39	4.37	5.27	6.15

CMOS035 MTC45200	CMOS Bidir Pad Buffer, 4mA, with Slew Rate Control, with Test Pins	BD4CRP

SYMBOL



BEHAVIOUR

A	EN	IO	TM	TEN	TA	ZI	IO
-	-	1	1	1	-	1	
-	-	-	1	0	-	-	
-	1	1	0	-	-	1	
-	0	-	0	-	-	-	
-	-	-	1	0	1		1
-	-	-	1	1	-		Z
1	0	-	0	-	-		1
-	1	-	0	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
IO	3.787 pF
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

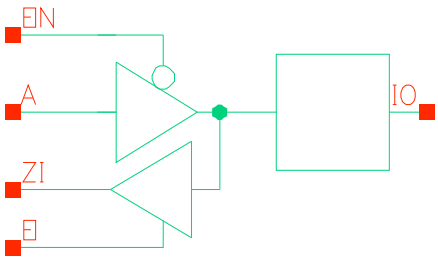
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.19	0.26	0.33	0.47
IO to ZI	Rise delay	0.19	0.28	0.37	0.54

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.06	1.11	1.27
EN to IO	1Z delay	1.32	1.36	1.51
TEN to IO	0Z delay	1.31	1.35	1.56
TEN to IO	1Z delay	1.54	1.58	1.77
TM to IO	0Z delay	1.72	1.78	2.00
TM to IO	1Z delay	1.95	2.01	2.22

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to IO	Fall delay	3.48	4.38	5.17	5.93
A to IO	Rise delay	3.43	4.42	5.32	6.19
EN to IO	Z0 delay	3.45	4.35	5.15	5.91
EN to IO	Z1 delay	3.39	4.37	5.27	6.15
TA to IO	Fall delay	3.81	4.71	5.51	6.27
TA to IO	Rise delay	3.70	4.69	5.59	6.46
TEN to IO	Z0 delay	3.76	4.66	5.46	6.22
TEN to IO	Z1 delay	3.70	4.68	5.58	6.46
TM to IO	Fall delay	3.98	4.88	5.68	6.44
TM to IO	Fall delay	3.81	4.72	5.52	6.28
TM to IO	Rise delay	4.14	5.12	6.03	6.90
TM to IO	Rise delay	3.60	4.58	5.49	6.36
TM to IO	Z0 delay	4.03	4.93	5.74	6.50
TM to IO	Z0 delay	3.80	4.71	5.51	6.27
TM to IO	Z1 delay	4.09	5.07	5.98	6.85
TM to IO	Z1 delay	3.72	4.70	5.61	6.48

CMOS035 MTC45200	CMOS Bidir Pad Buffer, 4mA	BD4HZIC

SYMBOL



BEHAVIOUR

E	EN	A	IO	ZI	IO
1	-	-	1	1	
0	-	-	-	Z	
-	0	1	-		1
-	1	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
E	5.0 SL
EN	3.8 SL
IO	3.795 pF
ZI	6.8 SL

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	322 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

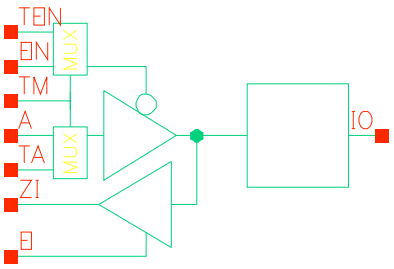
Timing/Load		1.0xSL	80.0xSL	160.0xSL	320.0xSL
E to ZI	Z0 delay	0.24	0.40	0.51	0.70
E to ZI	Z1 delay	0.17	0.32	0.41	0.59
IO to ZI	Fall delay	0.32	0.48	0.59	0.78
IO to ZI	Rise delay	0.26	0.40	0.50	0.68

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
E to ZI	0Z delay	0.33	0.38	0.57
E to ZI	1Z delay	0.26	0.32	0.53
EN to IO	0Z delay	1.06	1.11	1.27
EN to IO	1Z delay	1.31	1.36	1.51

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to IO	Fall delay	2.46	3.23	3.95	4.65
A to IO	Rise delay	2.47	3.35	4.20	5.05
EN to IO	Z0 delay	2.42	3.18	3.91	4.61
EN to IO	Z1 delay	2.42	3.30	4.15	5.00

CMOS035 MTC45200	CMOS Bidir Pad Buffer, 4mA, with Test Pins	BD4HZICP

SYMBOL



BEHAVIOUR

E	EN	A	IO	TM	TEN	TA	ZI	IO
1	-	-	1	-	-	-	1	
0	-	-	-	-	-	-	Z	
-	-	-	-	1	0	1		1
-	-	-	-	1	1	-		Z
-	0	1	-	0	-	-		1
-	1	-	-	0	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
E	5.0 SL
EN	3.8 SL
IO	3.795 pF
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
ZI	6.8 SL

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	322 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

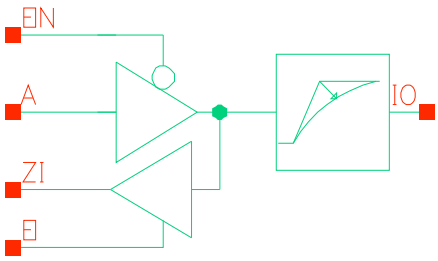
Timing/Load		1.0xSL	80.0xSL	160.0xSL	320.0xSL
E to ZI	Z0 delay	0.24	0.40	0.51	0.70
E to ZI	Z1 delay	0.17	0.32	0.41	0.59
IO to ZI	Fall delay	0.32	0.48	0.59	0.78
IO to ZI	Rise delay	0.26	0.40	0.50	0.68

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
E to ZI	0Z delay	0.33	0.38	0.57
E to ZI	1Z delay	0.26	0.32	0.53
EN to IO	0Z delay	1.06	1.11	1.27
EN to IO	1Z delay	1.31	1.36	1.51
TEN to IO	0Z delay	1.31	1.35	1.56
TEN to IO	1Z delay	1.54	1.58	1.77
TM to IO	0Z delay	1.72	1.78	2.00
TM to IO	1Z delay	1.94	2.01	2.22

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to IO	Fall delay	2.46	3.23	3.95	4.66
A to IO	Rise delay	2.47	3.35	4.20	5.05
EN to IO	Z0 delay	2.42	3.18	3.91	4.61
EN to IO	Z1 delay	2.42	3.30	4.15	5.00
TA to IO	Fall delay	2.79	3.56	4.28	4.99
TA to IO	Rise delay	2.75	3.62	4.47	5.32
TEN to IO	Z0 delay	2.73	3.50	4.22	4.92
TEN to IO	Z1 delay	2.73	3.61	4.46	5.31
TM to IO	Fall delay	2.97	3.73	4.46	5.16
TM to IO	Fall delay	2.80	3.56	4.29	4.99
TM to IO	Rise delay	3.18	4.05	4.91	5.75
TM to IO	Rise delay	2.64	3.51	4.37	5.21
TM to IO	Z0 delay	3.00	3.77	4.49	5.19
TM to IO	Z0 delay	2.77	3.53	4.26	4.96
TM to IO	Z1 delay	3.12	4.00	4.85	5.70
TM to IO	Z1 delay	2.75	3.63	4.48	5.33

CMOS035 MTC45200	CMOS Bidir Pad Buffer, 4mA, with Slew Rate Control	BD4HZICR

SYMBOL



BEHAVIOUR

E	EN	A	IO	ZI	IO
1	-	-	1	1	
0	-	-	-	Z	
-	0	1	-		1
-	1	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
E	5.0 SL
EN	3.8 SL
IO	3.795 pF
ZI	6.8 SL

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	322 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

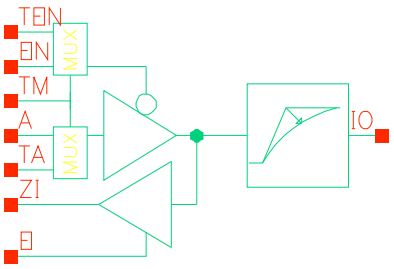
Timing/Load		1.0xSL	80.0xSL	160.0xSL	320.0xSL
E to ZI	Z0 delay	0.24	0.40	0.51	0.70
E to ZI	Z1 delay	0.17	0.32	0.41	0.59
IO to ZI	Fall delay	0.32	0.48	0.59	0.78
IO to ZI	Rise delay	0.26	0.40	0.50	0.68

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
E to ZI	0Z delay	0.33	0.38	0.57
E to ZI	1Z delay	0.26	0.32	0.53
EN to IO	0Z delay	1.06	1.11	1.27
EN to IO	1Z delay	1.32	1.36	1.51

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to IO	Fall delay	3.48	4.38	5.18	5.93
A to IO	Rise delay	3.43	4.42	5.32	6.19
EN to IO	Z0 delay	3.45	4.35	5.15	5.91
EN to IO	Z1 delay	3.39	4.38	5.28	6.15

CMOS035 MTC45200	CMOS Bidir Pad Buffer, 4mA, with Slew Rate Control, with Test Pins	BD4HZICRP

SYMBOL



BEHAVIOUR

E	EN	A	IO	TM	TEN	TA	ZI	IO
1	-	-	1	-	-	-	1	
0	-	-	-	-	-	-	Z	
-	-	-	-	1	0	1		1
-	-	-	-	1	1	-		Z
-	0	1	-	0	-	-		1
-	1	-	-	0	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
E	5.0 SL
EN	3.8 SL
IO	3.795 pF
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
ZI	6.8 SL

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	322 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

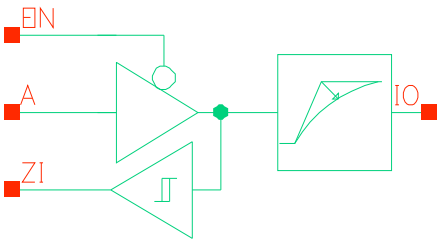
Timing/Load		1.0xSL	80.0xSL	160.0xSL	320.0xSL
E to ZI	Z0 delay	0.24	0.40	0.51	0.70
E to ZI	Z1 delay	0.17	0.32	0.41	0.59
IO to ZI	Fall delay	0.32	0.48	0.59	0.78
IO to ZI	Rise delay	0.26	0.40	0.50	0.68

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
E to ZI	0Z delay	0.33	0.38	0.57
E to ZI	1Z delay	0.26	0.32	0.53
EN to IO	0Z delay	1.06	1.11	1.27
EN to IO	1Z delay	1.32	1.36	1.51
TEN to IO	0Z delay	1.32	1.35	1.56
TEN to IO	1Z delay	1.54	1.58	1.77
TM to IO	0Z delay	1.72	1.78	2.00
TM to IO	1Z delay	1.95	2.01	2.22

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to IO	Fall delay	3.48	4.38	5.18	5.93
A to IO	Rise delay	3.43	4.42	5.32	6.19
EN to IO	Z0 delay	3.45	4.35	5.15	5.91
EN to IO	Z1 delay	3.39	4.38	5.28	6.15
TA to IO	Fall delay	3.81	4.71	5.51	6.27
TA to IO	Rise delay	3.71	4.69	5.59	6.46
TEN to IO	Z0 delay	3.76	4.66	5.46	6.22
TEN to IO	Z1 delay	3.70	4.68	5.59	6.46
TM to IO	Fall delay	3.98	4.88	5.69	6.44
TM to IO	Fall delay	3.81	4.72	5.52	6.28
TM to IO	Rise delay	4.14	5.12	6.03	6.90
TM to IO	Rise delay	3.60	4.59	5.49	6.36
TM to IO	Z0 delay	4.03	4.93	5.74	6.50
TM to IO	Z0 delay	3.80	4.71	5.51	6.27
TM to IO	Z1 delay	4.09	5.07	5.98	6.85
TM to IO	Z1 delay	3.72	4.71	5.61	6.48

CMOS035 MTC45200	CMOS Schmitt Trigger Bidir Pad Buffer, 4mA, with Slew Rate Control	BD4SCR

SYMBOL



BEHAVIOUR

A	EN	IO	ZI	IO
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
IO	3.794 pF

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

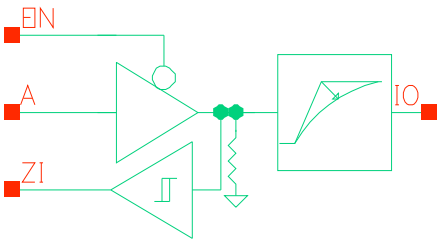
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.45	0.55	0.63	0.78
IO to ZI	Rise delay	0.42	0.52	0.61	0.78

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.06	1.11	1.27
EN to IO	1Z delay	1.32	1.36	1.51

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to IO	Fall delay	3.48	4.38	5.18	5.94
A to IO	Rise delay	3.43	4.42	5.32	6.19
EN to IO	Z0 delay	3.46	4.36	5.15	5.91
EN to IO	Z1 delay	3.39	4.38	5.28	6.15

CMOS035 MTC45200	CMOS Schmitt Trigger Bidir Pad Buffer with Active Pull-Down, 4mA, with Slew Rate Control	BD4SCRD

SYMBOL



BEHAVIOUR

A	EN	IO	ZI	IO
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
IO	3.802 pF

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

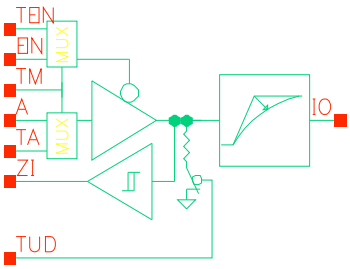
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.45	0.56	0.64	0.79
IO to ZI	Rise delay	0.43	0.53	0.62	0.79

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.06	1.11	1.27
EN to IO	1Z delay	1.30	1.35	1.50

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to IO	Fall delay	3.48	4.37	5.17	5.93
A to IO	Rise delay	3.43	4.42	5.32	6.20
EN to IO	Z0 delay	3.44	4.35	5.14	5.90
EN to IO	Z1 delay	3.39	4.38	5.28	6.15

CMOS035 MTC45200	CMOS Schmitt Trigger Bidir Pad Buffer with Active Pull-Down, 4mA, with Slew Rate Control, with Test Pins	BD4SCRDQP

SYMBOL



BEHAVIOUR

A	EN	IO	TM	TEN	TA	TUD	ZI	IO
-	-	1	1	1	-	-	1	
-	-	-	1	0	-	-	-	
-	1	1	0	-	-	-	1	
-	0	-	0	-	-	-	-	
-	-	-	1	0	1	-		1
-	-	-	1	1	-	-		Z
1	0	-	0	-	-	-		1
-	1	-	0	-	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
IO	3.799 pF
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
TUD	1.9 SL

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

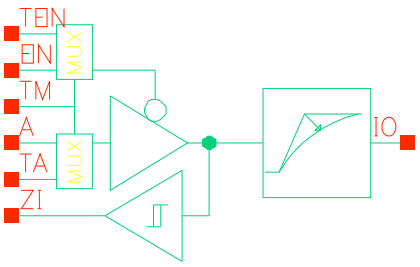
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.45	0.56	0.64	0.79
IO to ZI	Rise delay	0.43	0.53	0.62	0.79

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.06	1.11	1.27
EN to IO	1Z delay	1.32	1.36	1.51
TEN to IO	0Z delay	1.32	1.36	1.56
TEN to IO	1Z delay	1.54	1.58	1.77
TM to IO	0Z delay	1.72	1.79	2.01
TM to IO	1Z delay	1.94	2.01	2.21

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to IO	Fall delay	3.48	4.38	5.18	5.94
A to IO	Rise delay	3.43	4.42	5.32	6.20
EN to IO	Z0 delay	3.46	4.36	5.15	5.91
EN to IO	Z1 delay	3.39	4.38	5.28	6.15
TA to IO	Fall delay	3.81	4.71	5.51	6.27
TA to IO	Rise delay	3.71	4.70	5.60	6.47
TEN to IO	Z0 delay	3.77	4.67	5.47	6.23
TEN to IO	Z1 delay	3.70	4.69	5.59	6.46
TM to IO	Fall delay	3.99	4.89	5.69	6.45
TM to IO	Fall delay	3.82	4.72	5.52	6.28
TM to IO	Rise delay	4.14	5.13	6.03	6.90
TM to IO	Rise delay	3.60	4.59	5.49	6.36
TM to IO	Z0 delay	4.04	4.94	5.74	6.50
TM to IO	Z0 delay	3.81	4.71	5.51	6.27
TM to IO	Z1 delay	4.09	5.08	5.98	6.85
TM to IO	Z1 delay	3.72	4.71	5.61	6.49

CMOS035 MTC45200	CMOS Schmitt Trigger Bidir Pad Buffer, 4mA, with Slew Rate Control, with Test Pins	BD4SCRP

SYMBOL



BEHAVIOUR

A	EN	IO	TM	TEN	TA	ZI	IO
-	-	1	1	1	-	1	
-	-	-	1	0	-	-	
-	1	1	0	-	-	1	
-	0	-	0	-	-	-	
-	-	-	1	0	1		1
-	-	-	1	1	-		Z
1	0	-	0	-	-		1
-	1	-	0	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
IO	3.794 pF
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	81 SL

CMOS035 MTC45200	CMOS Schmitt Trigger Bidir Pad Buffer, 4mA, with Slew Rate Control, with Test Pins	BD4SCRP

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

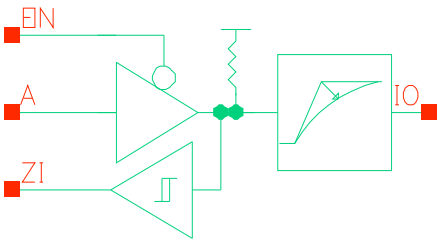
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.45	0.55	0.63	0.78
IO to ZI	Rise delay	0.42	0.52	0.61	0.78

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.06	1.11	1.27
EN to IO	1Z delay	1.32	1.36	1.51
TEN to IO	0Z delay	1.31	1.35	1.56
TEN to IO	1Z delay	1.54	1.58	1.77
TM to IO	0Z delay	1.72	1.78	2.00
TM to IO	1Z delay	1.94	2.01	2.21

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to IO	Fall delay	3.48	4.38	5.18	5.94
A to IO	Rise delay	3.43	4.42	5.32	6.19
EN to IO	Z0 delay	3.46	4.36	5.15	5.91
EN to IO	Z1 delay	3.39	4.38	5.28	6.15
TA to IO	Fall delay	3.81	4.71	5.51	6.27
TA to IO	Rise delay	3.70	4.69	5.60	6.47
TEN to IO	Z0 delay	3.77	4.67	5.47	6.23
TEN to IO	Z1 delay	3.70	4.69	5.59	6.46
TM to IO	Fall delay	3.99	4.89	5.69	6.45
TM to IO	Fall delay	3.82	4.72	5.52	6.28
TM to IO	Rise delay	4.14	5.13	6.03	6.90
TM to IO	Rise delay	3.60	4.59	5.49	6.36
TM to IO	Z0 delay	4.04	4.94	5.74	6.50
TM to IO	Z0 delay	3.81	4.71	5.51	6.27
TM to IO	Z1 delay	4.09	5.08	5.98	6.85
TM to IO	Z1 delay	3.72	4.71	5.61	6.48

CMOS035 MTC45200	CMOS Schmitt Trigger Bidir Pad Buffer with Active Pull-Up, 4mA, with Slew Rate Control	BD4SCRU

SYMBOL



BEHAVIOUR

A	EN	IO	ZI	IO
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
IO	3.805 pF

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

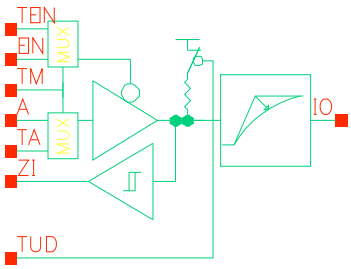
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.46	0.56	0.65	0.79
IO to ZI	Rise delay	0.43	0.53	0.61	0.79

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.05	1.10	1.26
EN to IO	1Z delay	1.33	1.38	1.53

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to IO	Fall delay	3.48	4.38	5.18	5.94
A to IO	Rise delay	3.43	4.41	5.31	6.18
EN to IO	Z0 delay	3.46	4.36	5.16	5.91
EN to IO	Z1 delay	3.38	4.37	5.27	6.14

CMOS035 MTC45200	CMOS Schmitt Trigger Bidir Pad Buffer with Active Pull-Up, 4mA, with Slew Rate Control, with Test Pins	BD4SCRUQP

SYMBOL



BEHAVIOUR

A	EN	IO	TM	TEN	TA	TUD	ZI	IO
-	-	1	1	1	-	-	1	
-	-	-	1	0	-	-	-	
-	1	1	0	-	-	-	1	
-	0	-	0	-	-	-	-	
-	-	-	1	0	1	-		1
-	-	-	1	1	-	-		Z
1	0	-	0	-	-	-		1
-	1	-	0	-	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
IO	3.800 pF
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
TUD	2.3 SL

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

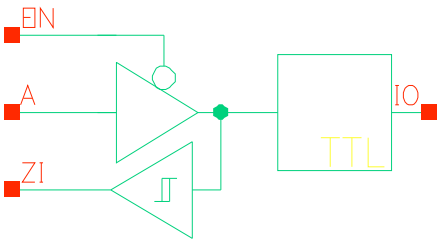
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.46	0.56	0.65	0.79
IO to ZI	Rise delay	0.43	0.53	0.61	0.79

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.06	1.11	1.27
EN to IO	1Z delay	1.33	1.38	1.53
TEN to IO	0Z delay	1.31	1.35	1.56
TEN to IO	1Z delay	1.55	1.59	1.79
TM to IO	0Z delay	1.72	1.78	2.00
TM to IO	1Z delay	1.96	2.02	2.23

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to IO	Fall delay	3.48	4.38	5.18	5.94
A to IO	Rise delay	3.43	4.42	5.32	6.19
EN to IO	Z0 delay	3.46	4.36	5.16	5.92
EN to IO	Z1 delay	3.39	4.38	5.28	6.15
TA to IO	Fall delay	3.82	4.72	5.51	6.27
TA to IO	Rise delay	3.71	4.69	5.60	6.47
TEN to IO	Z0 delay	3.77	4.67	5.47	6.23
TEN to IO	Z1 delay	3.70	4.69	5.59	6.46
TM to IO	Fall delay	3.99	4.89	5.69	6.45
TM to IO	Fall delay	3.82	4.72	5.52	6.28
TM to IO	Rise delay	4.14	5.13	6.03	6.90
TM to IO	Rise delay	3.60	4.59	5.49	6.36
TM to IO	Z0 delay	4.04	4.94	5.74	6.50
TM to IO	Z0 delay	3.81	4.71	5.51	6.27
TM to IO	Z1 delay	4.09	5.08	5.98	6.85
TM to IO	Z1 delay	3.72	4.71	5.61	6.48

CMOS035 MTC45200	TTL Five Volt tolerant Schmitt Trigger Bidir Pad Buffer, 4mA	BD4ST_FT

SYMBOL



BEHAVIOUR

A	EN	IO	ZI	IO
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
IO	3.915 pF

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

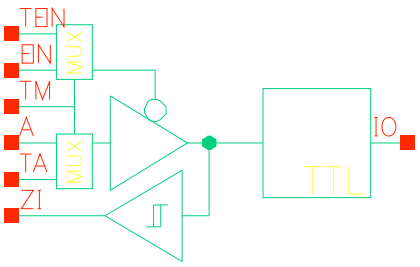
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.58	0.70	0.79	0.95
IO to ZI	Rise delay	0.75	0.85	0.94	1.11

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.09	1.14	1.32
EN to IO	1Z delay	1.41	1.47	1.64

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to IO	Fall delay	2.61	3.49	4.32	5.14
A to IO	Rise delay	2.30	3.05	3.77	4.48
EN to IO	Z0 delay	3.45	4.99	6.49	7.99
EN to IO	Z1 delay	2.29	3.04	3.76	4.47

CMOS035 MTC45200	TTL Five Volt tolerant Schmitt Trigger Bidir Pad Buffer, 4mA, with Test Pins	BD4STP_FT

SYMBOL



BEHAVIOUR

A	EN	IO	TM	TEN	TA	ZI	IO
-	-	1	1	1	-	1	
-	-	-	1	0	-	-	
-	1	1	0	-	-	1	
-	0	-	0	-	-	-	
-	-	-	1	0	1		1
-	-	-	1	1	-		Z
1	0	-	0	-	-		1
-	1	-	0	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
IO	3.915 pF
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

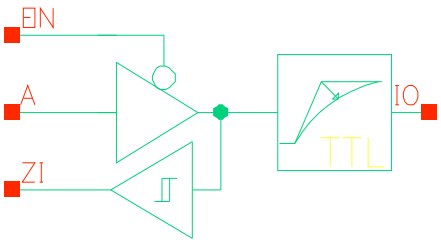
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.58	0.70	0.79	0.95
IO to ZI	Rise delay	0.75	0.85	0.94	1.11

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.09	1.14	1.32
EN to IO	1Z delay	1.41	1.47	1.64
TEN to IO	0Z delay	1.40	1.44	1.65
TEN to IO	1Z delay	1.68	1.72	1.93
TM to IO	0Z delay	1.80	1.87	2.08
TM to IO	1Z delay	2.09	2.15	2.36

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to IO	Fall delay	2.61	3.49	4.32	5.14
A to IO	Rise delay	2.30	3.05	3.77	4.48
EN to IO	Z0 delay	3.45	4.99	6.49	7.99
EN to IO	Z1 delay	2.29	3.04	3.76	4.47
TA to IO	Fall delay	2.94	3.82	4.66	5.47
TA to IO	Rise delay	2.58	3.32	4.04	4.75
TEN to IO	Z0 delay	3.83	5.37	6.87	8.37
TEN to IO	Z1 delay	2.66	3.41	4.13	4.84
TM to IO	Fall delay	3.12	4.00	4.83	5.65
TM to IO	Fall delay	2.95	3.83	4.66	5.48
TM to IO	Rise delay	3.01	3.76	4.47	5.19
TM to IO	Rise delay	2.47	3.22	3.94	4.65
TM to IO	Z0 delay	3.23	4.11	4.94	5.76
TM to IO	Z0 delay	2.95	3.83	4.66	5.48
TM to IO	Z1 delay	2.96	3.71	4.43	5.14
TM to IO	Z1 delay	2.62	3.37	4.09	4.80

CMOS035 MTC45200	TTL Schmitt Trigger Bidir Pad Buffer, 4mA, with Slew Rate Control	BD4STR

SYMBOL



BEHAVIOUR

A	EN	IO	ZI	IO
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
IO	3.919 pF

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

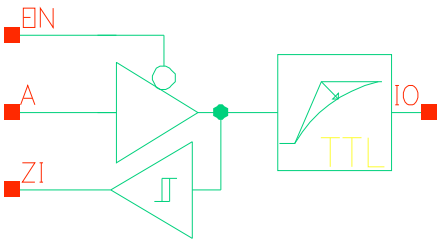
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.39	0.49	0.57	0.71
IO to ZI	Rise delay	0.36	0.45	0.54	0.71

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.06	1.11	1.27
EN to IO	1Z delay	1.32	1.36	1.51

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to IO	Fall delay	3.66	4.68	5.59	6.45
A to IO	Rise delay	3.23	4.09	4.86	5.60
EN to IO	Z0 delay	3.64	4.65	5.56	6.43
EN to IO	Z1 delay	3.18	4.05	4.82	5.56

CMOS035 MTC45200	TTL Five Volt tolerant Schmitt Trigger Bidir Pad Buffer, 4mA, with Slew Rate Control	BD4STR_FT

SYMBOL



BEHAVIOUR

A	EN	IO	ZI	IO
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
IO	3.915 pF

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

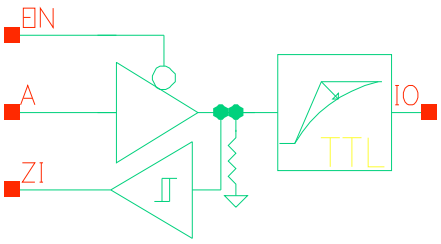
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.58	0.70	0.79	0.95
IO to ZI	Rise delay	0.75	0.85	0.94	1.11

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.09	1.14	1.32
EN to IO	1Z delay	1.41	1.47	1.64

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to IO	Fall delay	3.66	4.67	5.58	6.45
A to IO	Rise delay	3.24	4.11	4.89	5.63
EN to IO	Z0 delay	4.66	6.32	7.89	9.42
EN to IO	Z1 delay	3.23	4.10	4.88	5.62

CMOS035 MTC45200	TTL Five Volt tolerant Schmitt Trigger Bidir Pad Buffer with Active Pull-Down, 4mA, with Slew Rate Control	BD4STRD_FT

SYMBOL



BEHAVIOUR

A	EN	IO	ZI	IO
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
IO	3.912 pF

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

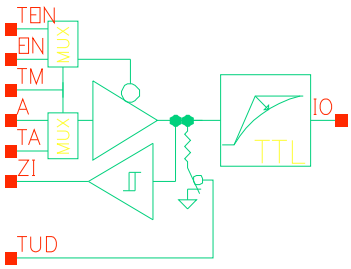
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.56	0.68	0.77	0.93
IO to ZI	Rise delay	0.83	0.92	1.01	1.18

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.09	1.15	1.33
EN to IO	1Z delay	1.40	1.45	1.62

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to IO	Fall delay	3.65	4.67	5.58	6.44
A to IO	Rise delay	3.24	4.11	4.89	5.63
EN to IO	Z0 delay	4.65	6.31	7.88	9.40
EN to IO	Z1 delay	3.23	4.11	4.88	5.62

CMOS035 MTC45200	TTL Five Volt tolerant Schmitt Trigger Bidir Pad Buffer with Active Pull-Down, 4mA, with Slew Rate Control, with Test Pins	BD4STRDQP_FT

SYMBOL



BEHAVIOUR

A	EN	IO	TM	TEN	TA	TUD	ZI	IO
-	-	1	1	1	-	-	1	
-	-	-	1	0	-	-	-	
-	1	1	0	-	-	-	1	
-	0	-	0	-	-	-	-	
-	-	-	1	0	1	-		1
-	-	-	1	1	-	-		Z
1	0	-	0	-	-	-		1
-	1	-	0	-	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
IO	3.915 pF
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
TUD	1.9 SL

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

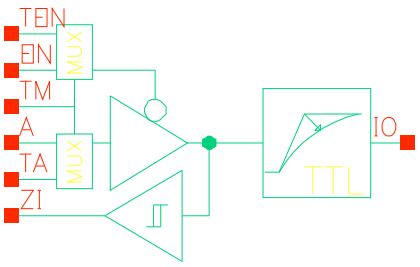
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.58	0.70	0.79	0.95
IO to ZI	Rise delay	0.83	0.93	1.02	1.18

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.09	1.15	1.33
EN to IO	1Z delay	1.41	1.47	1.64
TEN to IO	0Z delay	1.40	1.44	1.65
TEN to IO	1Z delay	1.68	1.72	1.93
TM to IO	0Z delay	1.81	1.87	2.09
TM to IO	1Z delay	2.09	2.15	2.36

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to IO	Fall delay	3.66	4.67	5.58	6.45
A to IO	Rise delay	3.24	4.11	4.89	5.63
EN to IO	Z0 delay	4.66	6.32	7.89	9.42
EN to IO	Z1 delay	3.23	4.11	4.88	5.62
TA to IO	Fall delay	3.99	5.00	5.92	6.78
TA to IO	Rise delay	3.51	4.39	5.16	5.90
TEN to IO	Z0 delay	5.04	6.70	8.26	9.79
TEN to IO	Z1 delay	3.60	4.47	5.25	5.99
TM to IO	Fall delay	4.17	5.18	6.09	6.96
TM to IO	Fall delay	4.00	5.01	5.92	6.79
TM to IO	Rise delay	3.95	4.82	5.59	6.34
TM to IO	Rise delay	3.41	4.28	5.06	5.80
TM to IO	Z0 delay	4.29	5.31	6.22	7.09
TM to IO	Z0 delay	4.01	5.03	5.94	6.81
TM to IO	Z1 delay	3.90	4.77	5.55	6.29
TM to IO	Z1 delay	3.57	4.44	5.22	5.96

CMOS035 MTC45200	TTL Schmitt Trigger Bidir Pad Buffer, 4mA, with Slew Rate Control, with Test Pins	BD4STRP

SYMBOL



BEHAVIOUR

A	EN	IO	TM	TEN	TA	ZI	IO
-	-	1	1	1	-	1	
-	-	-	1	0	-	-	
-	1	1	0	-	-	1	
-	0	-	0	-	-	-	
-	-	-	1	0	1		1
-	-	-	1	1	-		Z
1	0	-	0	-	-		1
-	1	-	0	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
IO	3.919 pF
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	81 SL

CMOS035 MTC45200	TTL Schmitt Trigger Bidir Pad Buffer, 4mA, with Slew Rate Control, with Test Pins	BD4STRP

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

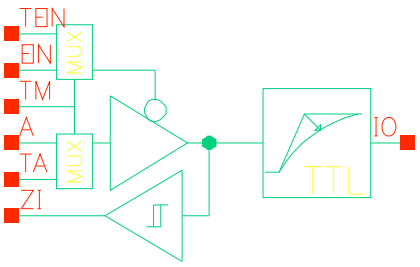
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.39	0.49	0.57	0.71
IO to ZI	Rise delay	0.36	0.45	0.54	0.71

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.06	1.11	1.27
EN to IO	1Z delay	1.32	1.36	1.51
TEN to IO	0Z delay	1.31	1.35	1.56
TEN to IO	1Z delay	1.54	1.58	1.77
TM to IO	0Z delay	1.72	1.78	2.00
TM to IO	1Z delay	1.95	2.01	2.22

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to IO	Fall delay	3.66	4.68	5.59	6.45
A to IO	Rise delay	3.23	4.09	4.86	5.60
EN to IO	Z0 delay	3.64	4.65	5.56	6.43
EN to IO	Z1 delay	3.18	4.05	4.82	5.56
TA to IO	Fall delay	4.00	5.01	5.92	6.79
TA to IO	Rise delay	3.50	4.36	5.14	5.88
TEN to IO	Z0 delay	3.95	4.96	5.88	6.74
TEN to IO	Z1 delay	3.49	4.36	5.13	5.87
TM to IO	Fall delay	4.17	5.18	6.09	6.96
TM to IO	Fall delay	4.00	5.01	5.93	6.80
TM to IO	Rise delay	3.93	4.80	5.57	6.31
TM to IO	Rise delay	3.39	4.26	5.03	5.77
TM to IO	Z0 delay	4.22	5.23	6.15	7.02
TM to IO	Z0 delay	3.99	5.00	5.92	6.79
TM to IO	Z1 delay	3.88	4.75	5.52	6.26
TM to IO	Z1 delay	3.51	4.38	5.15	5.89

CMOS035 MTC45200	TTL Five Volt tolerant Schmitt Trigger Bidir Pad Buffer, 4mA, with Slew Rate Control, with Test Pins	BD4STRP_FT

SYMBOL



BEHAVIOUR

A	EN	IO	TM	TEN	TA	ZI	IO
-	-	1	1	1	-	1	
-	-	-	1	0	-	-	
-	1	1	0	-	-	1	
-	0	-	0	-	-	-	
-	-	-	1	0	1		1
-	-	-	1	1	-		Z
1	0	-	0	-	-		1
-	1	-	0	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
IO	3.915 pF
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

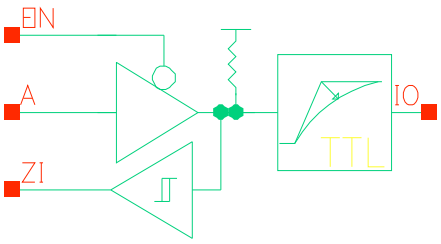
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.58	0.70	0.79	0.95
IO to ZI	Rise delay	0.75	0.85	0.94	1.11

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.09	1.14	1.32
EN to IO	1Z delay	1.41	1.47	1.64
TEN to IO	0Z delay	1.40	1.44	1.65
TEN to IO	1Z delay	1.68	1.72	1.93
TM to IO	0Z delay	1.80	1.87	2.08
TM to IO	1Z delay	2.09	2.15	2.36

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to IO	Fall delay	3.66	4.67	5.58	6.45
A to IO	Rise delay	3.24	4.11	4.89	5.63
EN to IO	Z0 delay	4.66	6.32	7.89	9.42
EN to IO	Z1 delay	3.23	4.10	4.88	5.62
TA to IO	Fall delay	3.99	5.00	5.91	6.78
TA to IO	Rise delay	3.51	4.38	5.16	5.90
TEN to IO	Z0 delay	5.04	6.70	8.26	9.79
TEN to IO	Z1 delay	3.60	4.47	5.25	5.99
TM to IO	Fall delay	4.17	5.18	6.09	6.96
TM to IO	Fall delay	4.00	5.01	5.92	6.79
TM to IO	Rise delay	3.94	4.82	5.59	6.33
TM to IO	Rise delay	3.41	4.28	5.05	5.79
TM to IO	Z0 delay	4.29	5.31	6.22	7.09
TM to IO	Z0 delay	4.01	5.03	5.94	6.81
TM to IO	Z1 delay	3.90	4.77	5.55	6.29
TM to IO	Z1 delay	3.57	4.44	5.22	5.96

CMOS035 MTC45200	TTL Five Volt tolerant Schmitt Trigger Bidir Pad Buffer with Active Pull-Up, 4mA, with Slew Rate Control	BD4STRU_FT

SYMBOL



BEHAVIOUR

A	EN	IO	ZI	IO
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
IO	3.916 pF

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

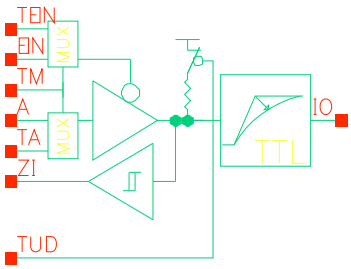
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.61	0.73	0.82	0.98
IO to ZI	Rise delay	0.72	0.81	0.90	1.07

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.08	1.14	1.32
EN to IO	1Z delay	1.43	1.48	1.65

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to IO	Fall delay	3.66	4.67	5.58	6.45
A to IO	Rise delay	3.23	4.10	4.88	5.62
EN to IO	Z0 delay	4.66	6.32	7.89	9.42
EN to IO	Z1 delay	3.22	4.09	4.87	5.61

CMOS035 MTC45200	TTL Five Volt tolerant Schmitt Trigger Bidir Pad Buffer with Active Pull-Up, 4mA, with Slew Rate Control, with Test Pins	BD4STRUQP_FT

SYMBOL



BEHAVIOUR

A	EN	IO	TM	TEN	TA	TUD	ZI	IO
-	-	1	1	1	-	-	1	
-	-	-	1	0	-	-	-	
-	1	1	0	-	-	-	1	
-	0	-	0	-	-	-	-	
-	-	-	1	0	1	-		1
-	-	-	1	1	-	-		Z
1	0	-	0	-	-	-		1
-	1	-	0	-	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
IO	3.915 pF
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
TUD	2.3 SL

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

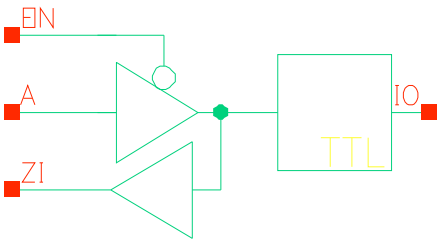
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.61	0.73	0.82	0.98
IO to ZI	Rise delay	0.75	0.85	0.94	1.11

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.09	1.14	1.32
EN to IO	1Z delay	1.43	1.48	1.65
TEN to IO	0Z delay	1.40	1.44	1.65
TEN to IO	1Z delay	1.70	1.74	1.94
TM to IO	0Z delay	1.80	1.87	2.08
TM to IO	1Z delay	2.11	2.17	2.38

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to IO	Fall delay	3.66	4.67	5.58	6.45
A to IO	Rise delay	3.24	4.11	4.89	5.63
EN to IO	Z0 delay	4.66	6.32	7.89	9.41
EN to IO	Z1 delay	3.23	4.10	4.88	5.62
TA to IO	Fall delay	3.99	5.00	5.91	6.78
TA to IO	Rise delay	3.51	4.38	5.16	5.90
TEN to IO	Z0 delay	5.04	6.70	8.26	9.79
TEN to IO	Z1 delay	3.60	4.47	5.25	5.99
TM to IO	Fall delay	4.17	5.18	6.09	6.96
TM to IO	Fall delay	4.00	5.01	5.92	6.79
TM to IO	Rise delay	3.94	4.82	5.59	6.33
TM to IO	Rise delay	3.41	4.28	5.05	5.79
TM to IO	Z0 delay	4.29	5.30	6.22	7.09
TM to IO	Z0 delay	4.01	5.03	5.94	6.81
TM to IO	Z1 delay	3.90	4.77	5.55	6.29
TM to IO	Z1 delay	3.57	4.44	5.22	5.96

CMOS035 MTC45200	TTL Five Volt tolerant Bidir Pad Buffer, 4mA	BD4T_FT

SYMBOL



BEHAVIOUR

A	EN	IO	ZI	IO
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
IO	3.919 pF

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

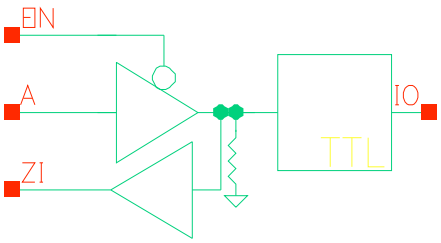
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.31	0.40	0.48	0.62
IO to ZI	Rise delay	0.34	0.43	0.51	0.68

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.09	1.14	1.32
EN to IO	1Z delay	1.41	1.47	1.64

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to IO	Fall delay	2.61	3.49	4.32	5.14
A to IO	Rise delay	2.30	3.05	3.77	4.48
EN to IO	Z0 delay	3.45	4.99	6.50	7.99
EN to IO	Z1 delay	2.29	3.04	3.76	4.47

CMOS035 MTC45200	TTL Five Volt tolerant Bidir Pad Buffer with Active Pull-Down, 4mA	BD4TD_FT

SYMBOL



BEHAVIOUR

A	EN	IO	ZI	IO
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
IO	3.918 pF

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.31	0.40	0.48	0.62

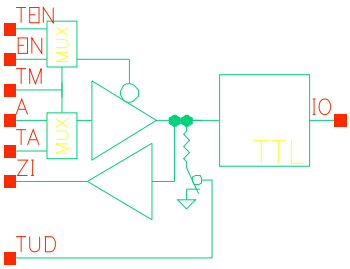
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Rise delay	0.33	0.42	0.51	0.68

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.09	1.14	1.32
EN to IO	1Z delay	1.41	1.47	1.64

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to IO	Fall delay	2.61	3.49	4.32	5.14
A to IO	Rise delay	2.30	3.05	3.77	4.48
EN to IO	Z0 delay	3.45	4.99	6.50	7.99
EN to IO	Z1 delay	2.29	3.04	3.76	4.47

CMOS035 MTC45200	TTL Five Volt tolerant Bidir Pad Buffer with Active Pull-Down, 4mA, with Test Pins	BD4TDQP_FT

SYMBOL



BEHAVIOUR

A	EN	IO	TM	TEN	TA	TUD	ZI	IO
-	-	1	1	1	-	-	1	
-	-	-	1	0	-	-	-	
-	1	1	0	-	-	-	1	
-	0	-	0	-	-	-	-	
-	-	-	1	0	1	-		1
-	-	-	1	1	-	-		Z
1	0	-	0	-	-	-		1
-	1	-	0	-	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
IO	3.925 pF
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
TUD	1.9 SL

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

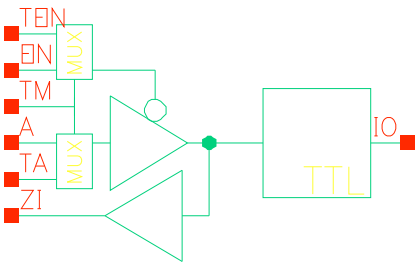
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.31	0.40	0.48	0.62
IO to ZI	Rise delay	0.34	0.43	0.51	0.68

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.09	1.14	1.32
EN to IO	1Z delay	1.42	1.47	1.64
TEN to IO	0Z delay	1.35	1.40	1.61
TEN to IO	1Z delay	1.63	1.68	1.88
TM to IO	0Z delay	1.52	1.58	1.80
TM to IO	1Z delay	2.09	2.15	2.36

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to IO	Fall delay	2.61	3.49	4.33	5.14
A to IO	Rise delay	2.30	3.05	3.77	4.48
EN to IO	Z0 delay	3.46	5.00	6.50	7.99
EN to IO	Z1 delay	2.29	3.04	3.76	4.47
TA to IO	Fall delay	2.95	3.83	4.66	5.48
TA to IO	Rise delay	2.54	3.28	4.00	4.71
TEN to IO	Z0 delay	3.83	5.37	6.88	8.37
TEN to IO	Z1 delay	2.66	3.41	4.13	4.84
TM to IO	Fall delay	3.12	4.00	4.84	5.65
TM to IO	Fall delay	2.95	3.83	4.67	5.48
TM to IO	Rise delay	3.01	3.76	4.47	5.19
TM to IO	Rise delay	2.47	3.22	3.94	4.65
TM to IO	Z0 delay	3.24	4.11	4.95	5.77
TM to IO	Z0 delay	2.96	3.83	4.67	5.49
TM to IO	Z1 delay	2.84	3.59	4.31	5.02
TM to IO	Z1 delay	2.62	3.37	4.09	4.80

CMOS035 MTC45200	TTL Five Volt tolerant Bidir Pad Buffer, 4mA, with Test Pins	BD4TP_FT

SYMBOL



BEHAVIOUR

A	EN	IO	TM	TEN	TA	ZI	IO
-	-	1	1	1	-	1	
-	-	-	1	0	-	-	
-	1	1	0	-	-	1	
-	0	-	0	-	-	-	
-	-	-	1	0	1		1
-	-	-	1	1	-		Z
1	0	-	0	-	-		1
-	1	-	0	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
IO	3.919 pF
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.31	0.40	0.48	0.62

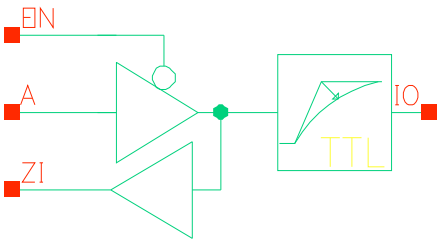
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Rise delay	0.34	0.43	0.51	0.68

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.09	1.14	1.32
EN to IO	1Z delay	1.41	1.47	1.64
TEN to IO	0Z delay	1.40	1.44	1.65
TEN to IO	1Z delay	1.68	1.72	1.93
TM to IO	0Z delay	1.80	1.87	2.08
TM to IO	1Z delay	2.09	2.15	2.36

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to IO	Fall delay	2.61	3.49	4.32	5.14
A to IO	Rise delay	2.30	3.05	3.77	4.48
EN to IO	Z0 delay	3.45	4.99	6.50	7.99
EN to IO	Z1 delay	2.29	3.04	3.76	4.47
TA to IO	Fall delay	2.95	3.82	4.66	5.48
TA to IO	Rise delay	2.58	3.32	4.04	4.75
TEN to IO	Z0 delay	3.83	5.37	6.87	8.37
TEN to IO	Z1 delay	2.66	3.41	4.13	4.84
TM to IO	Fall delay	3.12	4.00	4.83	5.65
TM to IO	Fall delay	2.95	3.83	4.66	5.48
TM to IO	Rise delay	3.01	3.76	4.47	5.19
TM to IO	Rise delay	2.47	3.22	3.94	4.65
TM to IO	Z0 delay	3.23	4.11	4.95	5.76
TM to IO	Z0 delay	2.95	3.83	4.66	5.48
TM to IO	Z1 delay	2.96	3.71	4.43	5.14
TM to IO	Z1 delay	2.62	3.37	4.09	4.80

CMOS035 MTC45200	TTL Five Volt tolerant Bidir Pad Buffer, 4mA, with Slew Rate Control	BD4TR_FT

SYMBOL



BEHAVIOUR

A	EN	IO	ZI	IO
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
IO	3.919 pF

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

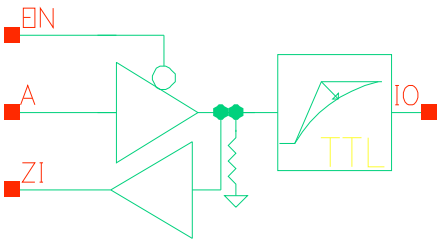
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.31	0.40	0.48	0.62
IO to ZI	Rise delay	0.34	0.43	0.51	0.68

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.09	1.14	1.32
EN to IO	1Z delay	1.42	1.47	1.64

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to IO	Fall delay	3.66	4.67	5.58	6.45
A to IO	Rise delay	3.24	4.11	4.89	5.63
EN to IO	Z0 delay	4.66	6.32	7.89	9.42
EN to IO	Z1 delay	3.23	4.10	4.88	5.62

CMOS035 MTC45200	TTL Five Volt tolerant Bidir Pad Buffer with Active Pull-Down, 4mA, with Slew Rate Control	BD4TRD_FT

SYMBOL



BEHAVIOUR

A	EN	IO	ZI	IO
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
IO	3.917 pF

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

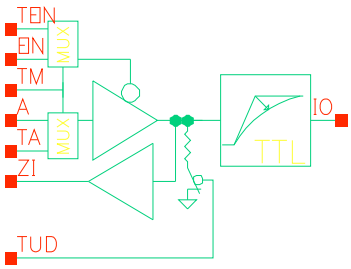
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.30	0.39	0.47	0.61
IO to ZI	Rise delay	0.35	0.44	0.53	0.70

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.09	1.15	1.33
EN to IO	1Z delay	1.40	1.45	1.62

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to IO	Fall delay	3.65	4.67	5.57	6.44
A to IO	Rise delay	3.24	4.11	4.89	5.63
EN to IO	Z0 delay	4.65	6.31	7.88	9.40
EN to IO	Z1 delay	3.23	4.10	4.88	5.62

CMOS035 MTC45200	TTL Five Volt tolerant Bidir Pad Buffer with Active Pull-Down, 4mA, with Slew Rate Control, with Test Pins	BD4TRDQP_FT

SYMBOL



BEHAVIOUR

A	EN	IO	TM	TEN	TA	TUD	ZI	IO
-	-	1	1	1	-	-	1	
-	-	-	1	0	-	-	-	
-	1	1	0	-	-	-	1	
-	0	-	0	-	-	-	-	
-	-	-	1	0	1	-		1
-	-	-	1	1	-	-		Z
1	0	-	0	-	-	-		1
-	1	-	0	-	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
IO	3.919 pF
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
TUD	1.9 SL

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.31	0.40	0.48	0.62

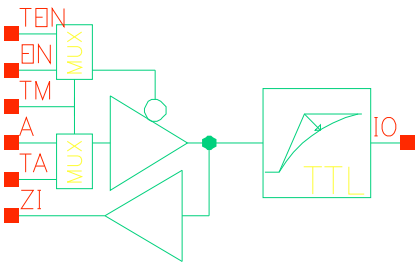
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Rise delay	0.35	0.44	0.53	0.70

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.09	1.15	1.33
EN to IO	1Z delay	1.42	1.47	1.64
TEN to IO	0Z delay	1.40	1.44	1.65
TEN to IO	1Z delay	1.68	1.72	1.93
TM to IO	0Z delay	1.81	1.87	2.09
TM to IO	1Z delay	2.09	2.15	2.37

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to IO	Fall delay	3.66	4.67	5.58	6.45
A to IO	Rise delay	3.24	4.11	4.89	5.63
EN to IO	Z0 delay	4.66	6.32	7.89	9.42
EN to IO	Z1 delay	3.23	4.10	4.88	5.62
TA to IO	Fall delay	3.99	5.01	5.91	6.78
TA to IO	Rise delay	3.51	4.38	5.16	5.90
TEN to IO	Z0 delay	5.04	6.70	8.27	9.79
TEN to IO	Z1 delay	3.60	4.47	5.25	5.99
TM to IO	Fall delay	4.17	5.18	6.09	6.96
TM to IO	Fall delay	4.00	5.01	5.92	6.79
TM to IO	Rise delay	3.94	4.82	5.59	6.34
TM to IO	Rise delay	3.41	4.28	5.05	5.80
TM to IO	Z0 delay	4.29	5.31	6.22	7.09
TM to IO	Z0 delay	4.01	5.03	5.94	6.81
TM to IO	Z1 delay	3.90	4.77	5.55	6.29
TM to IO	Z1 delay	3.56	4.44	5.21	5.95

CMOS035 MTC45200	TTL Five Volt tolerant Bidir Pad Buffer, 4mA, with Slew Rate Control, with Test Pins	BD4TRP_FT

SYMBOL



BEHAVIOUR

A	EN	IO	TM	TEN	TA	ZI	IO
-	-	1	1	1	-	1	
-	-	-	1	0	-	-	
-	1	1	0	-	-	1	
-	0	-	0	-	-	-	
-	-	-	1	0	1		1
-	-	-	1	1	-		Z
1	0	-	0	-	-		1
-	1	-	0	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
IO	3.919 pF
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

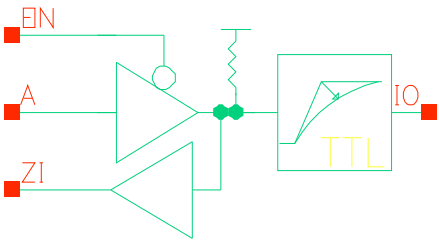
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.31	0.40	0.48	0.62
IO to ZI	Rise delay	0.34	0.43	0.51	0.68

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.09	1.14	1.32
EN to IO	1Z delay	1.42	1.47	1.64
TEN to IO	0Z delay	1.40	1.44	1.65
TEN to IO	1Z delay	1.68	1.72	1.93
TM to IO	0Z delay	1.80	1.87	2.08
TM to IO	1Z delay	2.09	2.15	2.37

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to IO	Fall delay	3.66	4.67	5.58	6.45
A to IO	Rise delay	3.24	4.11	4.89	5.63
EN to IO	Z0 delay	4.66	6.32	7.89	9.42
EN to IO	Z1 delay	3.23	4.10	4.88	5.62
TA to IO	Fall delay	3.99	5.01	5.91	6.78
TA to IO	Rise delay	3.51	4.38	5.16	5.90
TEN to IO	Z0 delay	5.04	6.70	8.27	9.79
TEN to IO	Z1 delay	3.60	4.47	5.25	5.99
TM to IO	Fall delay	4.17	5.18	6.09	6.96
TM to IO	Fall delay	4.00	5.01	5.92	6.79
TM to IO	Rise delay	3.94	4.82	5.59	6.33
TM to IO	Rise delay	3.40	4.28	5.05	5.79
TM to IO	Z0 delay	4.29	5.31	6.22	7.09
TM to IO	Z0 delay	4.01	5.03	5.94	6.81
TM to IO	Z1 delay	3.90	4.77	5.55	6.29
TM to IO	Z1 delay	3.56	4.43	5.21	5.95

CMOS035 MTC45200	TTL Five Volt tolerant Bidir Pad Buffer with Active Pull-Up, 4mA, with Slew Rate Control	BD4TRU_FT

SYMBOL



BEHAVIOUR

A	EN	IO	ZI	IO
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
IO	3.921 pF

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.33	0.42	0.50	0.64

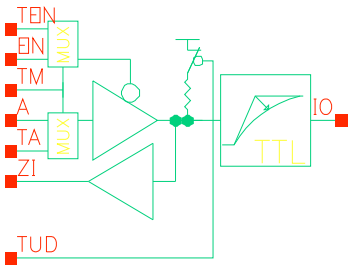
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Rise delay	0.33	0.42	0.51	0.68

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.08	1.14	1.32
EN to IO	1Z delay	1.43	1.48	1.65

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to IO	Fall delay	3.66	4.67	5.58	6.45
A to IO	Rise delay	3.23	4.10	4.88	5.62
EN to IO	Z0 delay	4.66	6.32	7.89	9.42
EN to IO	Z1 delay	3.22	4.09	4.87	5.61

CMOS035 MTC45200	TTL Five Volt tolerant Bidir Pad Buffer with Active Pull-Up, 4mA, with Slew Rate Control, with Test Pins	BD4TRUQP_FT

SYMBOL



BEHAVIOUR

A	EN	IO	TM	TEN	TA	TUD	ZI	IO
-	-	1	1	1	-	-	1	
-	-	-	1	0	-	-	-	
-	1	1	0	-	-	-	1	
-	0	-	0	-	-	-	-	
-	-	-	1	0	1	-		1
-	-	-	1	1	-	-		Z
1	0	-	0	-	-	-		1
-	1	-	0	-	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
IO	3.919 pF
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
TUD	2.3 SL

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

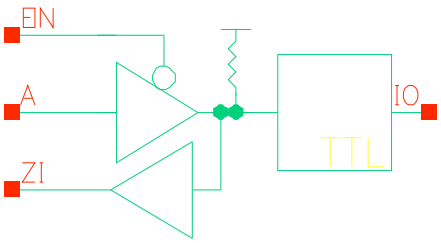
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.33	0.42	0.50	0.64
IO to ZI	Rise delay	0.34	0.43	0.51	0.68

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.09	1.14	1.32
EN to IO	1Z delay	1.43	1.48	1.65
TEN to IO	0Z delay	1.40	1.44	1.65
TEN to IO	1Z delay	1.70	1.74	1.94
TM to IO	0Z delay	1.80	1.87	2.08
TM to IO	1Z delay	2.11	2.17	2.38

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to IO	Fall delay	3.66	4.67	5.58	6.45
A to IO	Rise delay	3.24	4.11	4.89	5.63
EN to IO	Z0 delay	4.66	6.32	7.89	9.42
EN to IO	Z1 delay	3.23	4.10	4.88	5.62
TA to IO	Fall delay	3.99	5.00	5.91	6.78
TA to IO	Rise delay	3.51	4.38	5.16	5.90
TEN to IO	Z0 delay	5.04	6.70	8.27	9.79
TEN to IO	Z1 delay	3.60	4.47	5.25	5.99
TM to IO	Fall delay	4.17	5.18	6.09	6.96
TM to IO	Fall delay	4.00	5.01	5.92	6.79
TM to IO	Rise delay	3.94	4.82	5.59	6.33
TM to IO	Rise delay	3.40	4.28	5.05	5.79
TM to IO	Z0 delay	4.29	5.31	6.22	7.09
TM to IO	Z0 delay	4.01	5.03	5.94	6.81
TM to IO	Z1 delay	3.90	4.77	5.55	6.29
TM to IO	Z1 delay	3.56	4.43	5.21	5.95

CMOS035 MTC45200	TTL Five Volt tolerant Bidir Pad Buffer with Active Pull-Up, 4mA	BD4TU_FT

SYMBOL



BEHAVIOUR

A	EN	IO	ZI	IO
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
IO	3.918 pF

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

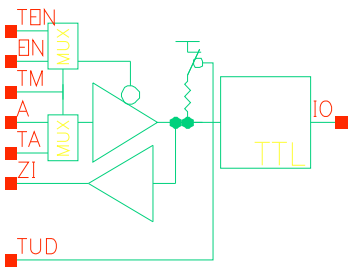
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.31	0.40	0.48	0.62
IO to ZI	Rise delay	0.33	0.42	0.51	0.68

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.09	1.14	1.32
EN to IO	1Z delay	1.41	1.47	1.64

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to IO	Fall delay	2.61	3.49	4.32	5.14
A to IO	Rise delay	2.30	3.05	3.77	4.48
EN to IO	Z0 delay	3.45	4.99	6.50	7.99
EN to IO	Z1 delay	2.29	3.04	3.76	4.47

CMOS035 MTC45200	TTL Five Volt tolerant Bidir Pad Buffer with Active Pull-Up, 4mA, with Test Pins	BD4TUQP_FT

SYMBOL



BEHAVIOUR

A	EN	IO	TM	TEN	TA	TUD	ZI	IO
-	-	1	1	1	-	-	1	
-	-	-	1	0	-	-	-	
-	1	1	0	-	-	-	1	
-	0	-	0	-	-	-	-	
-	-	-	1	0	1	-		1
-	-	-	1	1	-	-		Z
1	0	-	0	-	-	-		1
-	1	-	0	-	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
IO	3.925 pF
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
TUD	2.3 SL

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

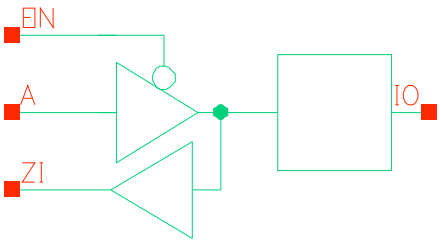
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.32	0.41	0.49	0.63
IO to ZI	Rise delay	0.34	0.43	0.51	0.68

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.09	1.14	1.32
EN to IO	1Z delay	1.42	1.47	1.64
TEN to IO	0Z delay	1.35	1.40	1.61
TEN to IO	1Z delay	1.63	1.68	1.88
TM to IO	0Z delay	1.52	1.58	1.80
TM to IO	1Z delay	2.09	2.15	2.36

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to IO	Fall delay	2.61	3.49	4.33	5.14
A to IO	Rise delay	2.30	3.05	3.77	4.48
EN to IO	Z0 delay	3.46	5.00	6.50	7.99
EN to IO	Z1 delay	2.29	3.04	3.76	4.47
TA to IO	Fall delay	2.95	3.83	4.66	5.48
TA to IO	Rise delay	2.54	3.28	4.00	4.71
TEN to IO	Z0 delay	3.83	5.37	6.88	8.37
TEN to IO	Z1 delay	2.66	3.41	4.13	4.84
TM to IO	Fall delay	3.12	4.00	4.84	5.65
TM to IO	Fall delay	2.95	3.83	4.66	5.48
TM to IO	Rise delay	3.01	3.76	4.47	5.19
TM to IO	Rise delay	2.47	3.22	3.94	4.65
TM to IO	Z0 delay	3.24	4.11	4.95	5.77
TM to IO	Z0 delay	2.95	3.83	4.67	5.49
TM to IO	Z1 delay	2.84	3.59	4.31	5.02
TM to IO	Z1 delay	2.62	3.37	4.09	4.80

CMOS035 MTC45200	CMOS Bidir Pad Buffer, 8mA	BD8C

SYMBOL



BEHAVIOUR

A	EN	IO	ZI	IO
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
IO	5.405 pF

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

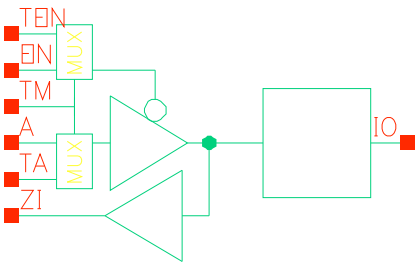
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.19	0.26	0.33	0.47
IO to ZI	Rise delay	0.19	0.28	0.37	0.54

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.01	1.06	1.22
EN to IO	1Z delay	1.25	1.30	1.44

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to IO	Fall delay	2.33	3.09	3.81	4.52
A to IO	Rise delay	2.39	3.26	4.11	4.96
EN to IO	Z0 delay	2.29	3.05	3.77	4.47
EN to IO	Z1 delay	2.34	3.21	4.06	4.91

CMOS035 MTC45200	CMOS Bidir Pad Buffer, 8mA, with Test Pins	BD8CP

SYMBOL



BEHAVIOUR

A	EN	IO	TM	TEN	TA	ZI	IO
-	-	1	1	1	-	1	
-	-	-	1	0	-	-	
-	1	1	0	-	-	1	
-	0	-	0	-	-	-	
-	-	-	1	0	1		1
-	-	-	1	1	-		Z
1	0	-	0	-	-		1
-	1	-	0	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
IO	5.405 pF
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	81 SL

CMOS035 MTC45200	CMOS Bidir Pad Buffer, 8mA, with Test Pins	BD8CP

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

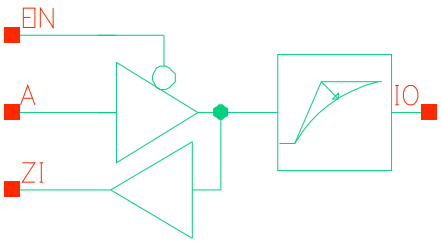
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.19	0.26	0.33	0.47
IO to ZI	Rise delay	0.19	0.28	0.37	0.54

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.01	1.06	1.22
EN to IO	1Z delay	1.25	1.30	1.44
TEN to IO	0Z delay	1.27	1.31	1.51
TEN to IO	1Z delay	1.47	1.51	1.70
TM to IO	0Z delay	1.67	1.74	1.96
TM to IO	1Z delay	1.88	1.94	2.15

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to IO	Fall delay	2.33	3.09	3.81	4.52
A to IO	Rise delay	2.39	3.26	4.11	4.96
EN to IO	Z0 delay	2.29	3.05	3.77	4.47
EN to IO	Z1 delay	2.34	3.21	4.06	4.91
TA to IO	Fall delay	2.66	3.42	4.15	4.85
TA to IO	Rise delay	2.66	3.53	4.38	5.23
TEN to IO	Z0 delay	2.60	3.36	4.08	4.79
TEN to IO	Z1 delay	2.65	3.52	4.37	5.22
TM to IO	Fall delay	2.84	3.60	4.32	5.03
TM to IO	Fall delay	2.67	3.43	4.15	4.85
TM to IO	Rise delay	3.09	3.96	4.82	5.66
TM to IO	Rise delay	2.55	3.43	4.28	5.12
TM to IO	Z0 delay	2.87	3.63	4.35	5.05
TM to IO	Z0 delay	2.64	3.40	4.12	4.82
TM to IO	Z1 delay	3.04	3.91	4.76	5.61
TM to IO	Z1 delay	2.67	3.54	4.39	5.24

CMOS035 MTC45200	CMOS Bidir Pad Buffer, 8mA, with Slew Rate Control	BD8CR

SYMBOL



BEHAVIOUR

A	EN	IO	ZI	IO
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
IO	5.405 pF

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

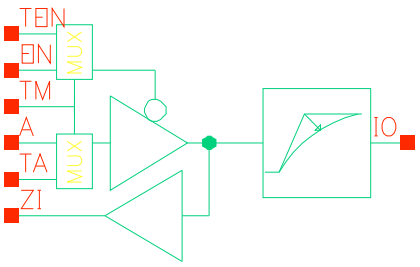
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.19	0.26	0.33	0.47
IO to ZI	Rise delay	0.19	0.28	0.37	0.54

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.01	1.06	1.22
EN to IO	1Z delay	1.25	1.30	1.44

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to IO	Fall delay	3.27	4.15	4.94	5.69
A to IO	Rise delay	3.31	4.29	5.18	6.04
EN to IO	Z0 delay	3.24	4.12	4.91	5.66
EN to IO	Z1 delay	3.27	4.24	5.13	6.00

CMOS035 MTC45200	CMOS Bidir Pad Buffer, 8mA, with Slew Rate Control, with Test Pins	BD8CRP

SYMBOL



BEHAVIOUR

A	EN	IO	TM	TEN	TA	ZI	IO
-	-	1	1	1	-	1	
-	-	-	1	0	-	-	
-	1	1	0	-	-	1	
-	0	-	0	-	-	-	
-	-	-	1	0	1		1
-	-	-	1	1	-		Z
1	0	-	0	-	-		1
-	1	-	0	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
IO	5.405 pF
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

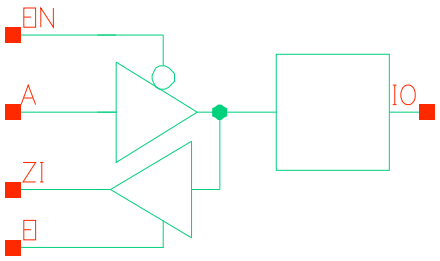
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.19	0.26	0.33	0.47
IO to ZI	Rise delay	0.19	0.28	0.37	0.54

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.01	1.06	1.22
EN to IO	1Z delay	1.25	1.30	1.44
TEN to IO	0Z delay	1.27	1.31	1.51
TEN to IO	1Z delay	1.47	1.51	1.71
TM to IO	0Z delay	1.68	1.74	1.96
TM to IO	1Z delay	1.88	1.94	2.15

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to IO	Fall delay	3.27	4.15	4.94	5.69
A to IO	Rise delay	3.31	4.29	5.18	6.04
EN to IO	Z0 delay	3.24	4.12	4.91	5.66
EN to IO	Z1 delay	3.27	4.24	5.13	6.00
TA to IO	Fall delay	3.60	4.48	5.27	6.02
TA to IO	Rise delay	3.58	4.56	5.45	6.32
TEN to IO	Z0 delay	3.56	4.44	5.22	5.98
TEN to IO	Z1 delay	3.58	4.55	5.44	6.31
TM to IO	Fall delay	3.78	4.66	5.45	6.20
TM to IO	Fall delay	3.61	4.49	5.28	6.03
TM to IO	Rise delay	4.01	4.99	5.88	6.75
TM to IO	Rise delay	3.48	4.45	5.35	6.21
TM to IO	Z0 delay	3.83	4.71	5.50	6.25
TM to IO	Z0 delay	3.59	4.47	5.27	6.02
TM to IO	Z1 delay	3.97	4.94	5.84	6.70
TM to IO	Z1 delay	3.60	4.57	5.47	6.33

CMOS035 MTC45200	CMOS Bidir Pad Buffer, 8mA	BD8HZIC

SYMBOL



BEHAVIOUR

E	EN	A	IO	ZI	IO
1	-	-	1	1	
0	-	-	-	Z	
-	0	1	-		1
-	1	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
E	5.0 SL
EN	3.8 SL
IO	5.413 pF
ZI	6.8 SL

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	322 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

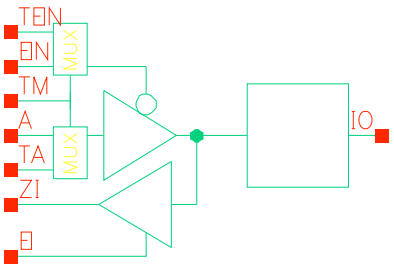
Timing/Load		1.0xSL	80.0xSL	160.0xSL	320.0xSL
E to ZI	Z0 delay	0.24	0.40	0.51	0.70
E to ZI	Z1 delay	0.17	0.32	0.41	0.59
IO to ZI	Fall delay	0.32	0.48	0.59	0.78
IO to ZI	Rise delay	0.26	0.40	0.50	0.68

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
E to ZI	0Z delay	0.33	0.38	0.57
E to ZI	1Z delay	0.26	0.32	0.53
EN to IO	0Z delay	1.01	1.06	1.22
EN to IO	1Z delay	1.25	1.30	1.44

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to IO	Fall delay	2.33	3.09	3.81	4.52
A to IO	Rise delay	2.39	3.26	4.11	4.96
EN to IO	Z0 delay	2.29	3.05	3.77	4.47
EN to IO	Z1 delay	2.34	3.21	4.06	4.91

CMOS035 MTC45200	CMOS Bidir Pad Buffer, 8mA, with Test Pins	BD8HZICP

SYMBOL



BEHAVIOUR

E	EN	A	IO	TM	TEN	TA	ZI	IO
1	-	-	1	-	-	-	1	
0	-	-	-	-	-	-	Z	
-	-	-	-	1	0	1		1
-	-	-	-	1	1	-		Z
-	0	1	-	0	-	-		1
-	1	-	-	0	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
E	5.0 SL
EN	3.8 SL
IO	5.413 pF
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
ZI	6.8 SL

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	322 SL

CMOS035 MTC45200	CMOS Bidir Pad Buffer, 8mA, with Test Pins	BD8HZICP

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

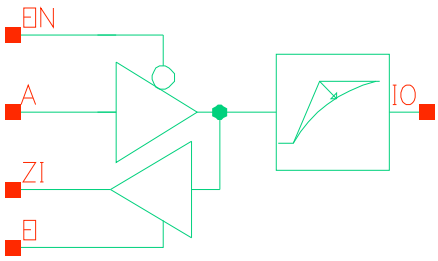
Timing/Load		1.0xSL	80.0xSL	160.0xSL	320.0xSL
E to ZI	Z0 delay	0.24	0.40	0.51	0.70
E to ZI	Z1 delay	0.17	0.32	0.41	0.59
IO to ZI	Fall delay	0.32	0.48	0.59	0.78
IO to ZI	Rise delay	0.26	0.40	0.50	0.68

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
E to ZI	0Z delay	0.33	0.38	0.57
E to ZI	1Z delay	0.26	0.32	0.53
EN to IO	0Z delay	1.01	1.06	1.22
EN to IO	1Z delay	1.25	1.30	1.44
TEN to IO	0Z delay	1.27	1.31	1.51
TEN to IO	1Z delay	1.47	1.51	1.70
TM to IO	0Z delay	1.68	1.74	1.96
TM to IO	1Z delay	1.88	1.94	2.15

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to IO	Fall delay	2.33	3.09	3.81	4.52
A to IO	Rise delay	2.39	3.26	4.11	4.96
EN to IO	Z0 delay	2.29	3.05	3.77	4.47
EN to IO	Z1 delay	2.34	3.21	4.06	4.91
TA to IO	Fall delay	2.66	3.43	4.15	4.85
TA to IO	Rise delay	2.66	3.53	4.38	5.23
TEN to IO	Z0 delay	2.60	3.36	4.08	4.79
TEN to IO	Z1 delay	2.65	3.52	4.37	5.22
TM to IO	Fall delay	2.84	3.60	4.32	5.03
TM to IO	Fall delay	2.67	3.43	4.15	4.85
TM to IO	Rise delay	3.09	3.96	4.82	5.66
TM to IO	Rise delay	2.55	3.42	4.28	5.12
TM to IO	Z0 delay	2.87	3.63	4.35	5.06
TM to IO	Z0 delay	2.64	3.40	4.12	4.82
TM to IO	Z1 delay	3.04	3.91	4.76	5.61
TM to IO	Z1 delay	2.67	3.54	4.39	5.24

CMOS035 MTC45200	CMOS Bidir Pad Buffer, 8mA, with Slew Rate Control	BD8HZICR

SYMBOL



BEHAVIOUR

E	EN	A	IO	ZI	IO
1	-	-	1	1	
0	-	-	-	Z	
-	0	1	-		1
-	1	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
E	5.0 SL
EN	3.8 SL
IO	5.412 pF
ZI	6.8 SL

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	322 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

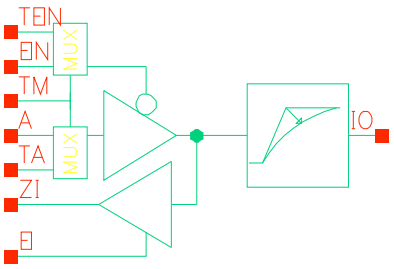
Timing/Load		1.0xSL	80.0xSL	160.0xSL	320.0xSL
E to ZI	Z0 delay	0.24	0.40	0.51	0.70
E to ZI	Z1 delay	0.17	0.32	0.41	0.59
IO to ZI	Fall delay	0.32	0.48	0.59	0.78
IO to ZI	Rise delay	0.26	0.40	0.50	0.68

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
E to ZI	0Z delay	0.33	0.38	0.57
E to ZI	1Z delay	0.26	0.32	0.53
EN to IO	0Z delay	1.01	1.06	1.22
EN to IO	1Z delay	1.25	1.30	1.44

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to IO	Fall delay	3.27	4.15	4.94	5.69
A to IO	Rise delay	3.31	4.29	5.18	6.04
EN to IO	Z0 delay	3.24	4.12	4.91	5.66
EN to IO	Z1 delay	3.27	4.24	5.14	6.00

CMOS035 MTC45200	CMOS Bidir Pad Buffer, 8mA, with Slew Rate Control, with Test Pins	BD8HZICRP

SYMBOL



BEHAVIOUR

E	EN	A	IO	TM	TEN	TA	ZI	IO
1	-	-	1	-	-	-	1	
0	-	-	-	-	-	-	Z	
-	-	-	-	1	0	1		1
-	-	-	-	1	1	-		Z
-	0	1	-	0	-	-		1
-	1	-	-	0	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
E	5.0 SL
EN	3.8 SL
IO	5.412 pF
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
ZI	6.8 SL

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	322 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	80.0xSL	160.0xSL	320.0xSL
IO to ZI	Fall delay	0.32	0.48	0.59	0.78
IO to ZI	Rise delay	0.26	0.40	0.50	0.68

Timing/Load		1.0xSL	80.0xSL	160.0xSL	320.0xSL
E to ZI	Z0 delay	0.24	0.40	0.51	0.70
E to ZI	Z1 delay	0.17	0.32	0.41	0.59

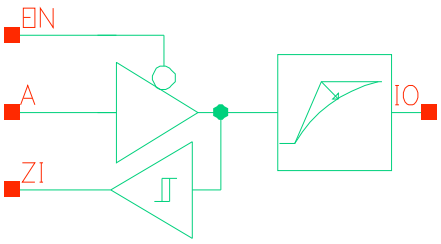
Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.01	1.06	1.22
EN to IO	1Z delay	1.25	1.30	1.44
TEN to IO	0Z delay	1.27	1.31	1.51
TEN to IO	1Z delay	1.47	1.51	1.71
TM to IO	0Z delay	1.68	1.74	1.96
TM to IO	1Z delay	1.88	1.94	2.15

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
E to ZI	0Z delay	0.33	0.38	0.57
E to ZI	1Z delay	0.26	0.32	0.53

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to IO	Fall delay	3.27	4.15	4.94	5.69
A to IO	Rise delay	3.31	4.29	5.18	6.04
EN to IO	Z0 delay	3.24	4.12	4.91	5.66
EN to IO	Z1 delay	3.27	4.24	5.14	6.00
TA to IO	Fall delay	3.60	4.48	5.27	6.02
TA to IO	Rise delay	3.58	4.56	5.45	6.32
TEN to IO	Z0 delay	3.55	4.44	5.23	5.98
TEN to IO	Z1 delay	3.58	4.55	5.44	6.31
TM to IO	Fall delay	3.77	4.65	5.45	6.20
TM to IO	Fall delay	3.60	4.49	5.28	6.03
TM to IO	Rise delay	4.02	4.99	5.88	6.75
TM to IO	Rise delay	3.48	4.45	5.35	6.21
TM to IO	Z0 delay	3.82	4.71	5.50	6.25
TM to IO	Z0 delay	3.59	4.48	5.27	6.02
TM to IO	Z1 delay	3.97	4.94	5.84	6.70
TM to IO	Z1 delay	3.60	4.57	5.47	6.33

CMOS035 MTC45200	CMOS Schmitt Trigger Bidir Pad Buffer, 8mA, with Slew Rate Control	BD8SCR

SYMBOL



BEHAVIOUR

A	EN	IO	ZI	IO
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
IO	5.412 pF

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

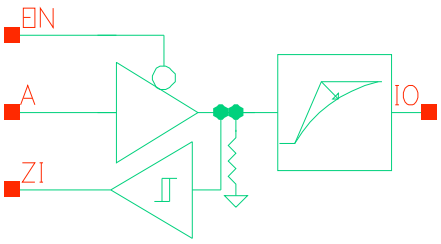
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.45	0.55	0.63	0.78
IO to ZI	Rise delay	0.42	0.52	0.61	0.78

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.01	1.06	1.22
EN to IO	1Z delay	1.25	1.30	1.44

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to IO	Fall delay	3.27	4.15	4.94	5.69
A to IO	Rise delay	3.31	4.29	5.18	6.05
EN to IO	Z0 delay	3.25	4.13	4.91	5.67
EN to IO	Z1 delay	3.27	4.24	5.14	6.00

CMOS035 MTC45200	CMOS Schmitt Trigger Bidir Pad Buffer with Active Pull-Down, 8mA, with Slew Rate Control	BD8SCRD

SYMBOL



BEHAVIOUR

A	EN	IO	ZI	IO
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
IO	5.420 pF

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

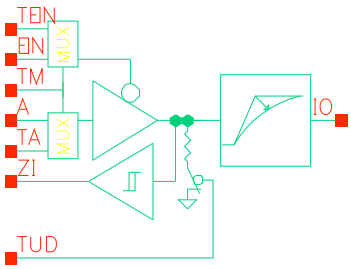
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.45	0.56	0.64	0.79
IO to ZI	Rise delay	0.43	0.53	0.62	0.79

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.02	1.07	1.22
EN to IO	1Z delay	1.24	1.29	1.44

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to IO	Fall delay	3.27	4.15	4.94	5.69
A to IO	Rise delay	3.31	4.29	5.18	6.05
EN to IO	Z0 delay	3.24	4.12	4.91	5.66
EN to IO	Z1 delay	3.27	4.24	5.14	6.01

CMOS035 MTC45200	CMOS Schmitt Trigger Bidir Pad Buffer with Active Pull-Down, 8mA, with Slew Rate Control, with Test Pins	BD8SCRDQP

SYMBOL



BEHAVIOUR

A	EN	IO	TM	TEN	TA	TUD	ZI	IO
-	-	1	1	1	-	-	1	
-	-	-	1	0	-	-	-	
-	1	1	0	-	-	-	1	
-	0	-	0	-	-	-	-	
-	-	-	1	0	1	-		1
-	-	-	1	1	-	-		Z
1	0	-	0	-	-	-		1
-	1	-	0	-	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
IO	5.417 pF
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
TUD	1.9 SL

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	81 SL

CMOS035 MTC45200	CMOS Schmitt Trigger Bidir Pad Buffer with Active Pull-Down, 8mA, with Slew Rate Control, with Test Pins	BD8SCRDQP

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

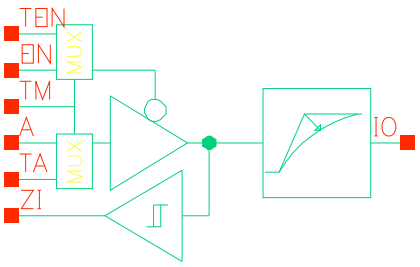
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.45	0.56	0.64	0.79
IO to ZI	Rise delay	0.43	0.53	0.62	0.79

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.02	1.07	1.22
EN to IO	1Z delay	1.25	1.30	1.44
TEN to IO	0Z delay	1.27	1.31	1.52
TEN to IO	1Z delay	1.47	1.51	1.71
TM to IO	0Z delay	1.68	1.75	1.96
TM to IO	1Z delay	1.88	1.94	2.15

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to IO	Fall delay	3.27	4.15	4.94	5.69
A to IO	Rise delay	3.31	4.29	5.18	6.05
EN to IO	Z0 delay	3.25	4.13	4.91	5.67
EN to IO	Z1 delay	3.27	4.24	5.14	6.01
TA to IO	Fall delay	3.60	4.48	5.27	6.03
TA to IO	Rise delay	3.58	4.56	5.46	6.32
TEN to IO	Z0 delay	3.56	4.44	5.23	5.98
TEN to IO	Z1 delay	3.58	4.55	5.45	6.32
TM to IO	Fall delay	3.78	4.66	5.45	6.20
TM to IO	Fall delay	3.61	4.49	5.28	6.03
TM to IO	Rise delay	4.02	4.99	5.89	6.76
TM to IO	Rise delay	3.48	4.46	5.35	6.22
TM to IO	Z0 delay	3.83	4.71	5.50	6.25
TM to IO	Z0 delay	3.60	4.48	5.27	6.02
TM to IO	Z1 delay	3.97	4.94	5.84	6.71
TM to IO	Z1 delay	3.60	4.58	5.47	6.34

CMOS035 MTC45200	CMOS Schmitt Trigger Bidir Pad Buffer, 8mA, with Slew Rate Control, with Test Pins	BD8SCRP

SYMBOL



BEHAVIOUR

A	EN	IO	TM	TEN	TA	ZI	IO
-	-	1	1	1	-	1	
-	-	-	1	0	-	-	
-	1	1	0	-	-	1	
-	0	-	0	-	-	-	
-	-	-	1	0	1		1
-	-	-	1	1	-		Z
1	0	-	0	-	-		1
-	1	-	0	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
IO	5.412 pF
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

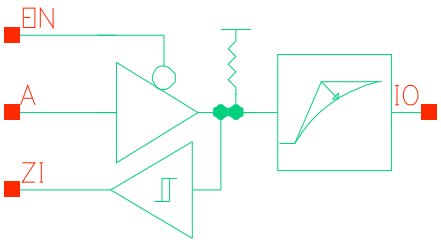
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.45	0.55	0.63	0.78
IO to ZI	Rise delay	0.42	0.52	0.61	0.78

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.01	1.06	1.22
EN to IO	1Z delay	1.25	1.30	1.44
TEN to IO	0Z delay	1.27	1.31	1.51
TEN to IO	1Z delay	1.47	1.51	1.71
TM to IO	0Z delay	1.68	1.74	1.96
TM to IO	1Z delay	1.88	1.94	2.15

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to IO	Fall delay	3.27	4.15	4.94	5.69
A to IO	Rise delay	3.31	4.29	5.18	6.05
EN to IO	Z0 delay	3.25	4.13	4.91	5.67
EN to IO	Z1 delay	3.27	4.24	5.14	6.00
TA to IO	Fall delay	3.60	4.48	5.27	6.03
TA to IO	Rise delay	3.58	4.56	5.45	6.32
TEN to IO	Z0 delay	3.56	4.44	5.23	5.98
TEN to IO	Z1 delay	3.58	4.55	5.45	6.31
TM to IO	Fall delay	3.78	4.66	5.45	6.20
TM to IO	Fall delay	3.61	4.49	5.28	6.03
TM to IO	Rise delay	4.02	4.99	5.89	6.75
TM to IO	Rise delay	3.48	4.45	5.35	6.21
TM to IO	Z0 delay	3.83	4.71	5.50	6.25
TM to IO	Z0 delay	3.60	4.48	5.27	6.02
TM to IO	Z1 delay	3.97	4.94	5.84	6.70
TM to IO	Z1 delay	3.60	4.58	5.47	6.34

CMOS035 MTC45200	CMOS Schmitt Trigger Bidir Pad Buffer with Active Pull-Up, 8mA, with Slew Rate Control	BD8SCRU

SYMBOL



BEHAVIOUR

A	EN	IO	ZI	IO
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
IO	5.422 pF

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

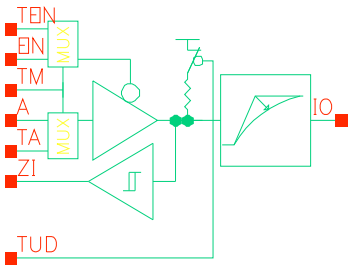
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.46	0.56	0.65	0.79
IO to ZI	Rise delay	0.43	0.53	0.61	0.79

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.01	1.06	1.22
EN to IO	1Z delay	1.26	1.30	1.45

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to IO	Fall delay	3.27	4.15	4.94	5.69
A to IO	Rise delay	3.31	4.28	5.18	6.04
EN to IO	Z0 delay	3.25	4.13	4.92	5.67
EN to IO	Z1 delay	3.26	4.24	5.13	6.00

CMOS035 MTC45200	CMOS Schmitt Trigger Bidir Pad Buffer with Active Pull-Up, 8mA, with Slew Rate Control, with Test Pins	BD8SCRUQP

SYMBOL



BEHAVIOUR

A	EN	IO	TM	TEN	TA	TUD	ZI	IO
-	-	1	1	1	-	-	1	
-	-	-	1	0	-	-	-	
-	1	1	0	-	-	-	1	
-	0	-	0	-	-	-	-	
-	-	-	1	0	1	-		1
-	-	-	1	1	-	-		Z
1	0	-	0	-	-	-		1
-	1	-	0	-	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
IO	5.418 pF
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
TUD	2.3 SL

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	81 SL

CMOS035 MTC45200	CMOS Schmitt Trigger Bidir Pad Buffer with Active Pull-Up, 8mA, with Slew Rate Control, with Test Pins	BD8SCRUQP

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

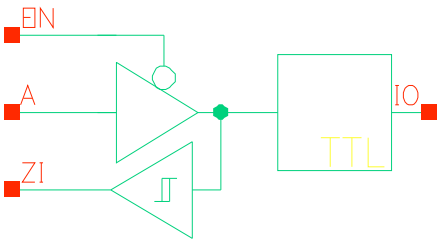
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.46	0.56	0.65	0.79
IO to ZI	Rise delay	0.43	0.53	0.61	0.79

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.01	1.06	1.22
EN to IO	1Z delay	1.26	1.30	1.45
TEN to IO	0Z delay	1.27	1.31	1.51
TEN to IO	1Z delay	1.48	1.52	1.71
TM to IO	0Z delay	1.68	1.74	1.96
TM to IO	1Z delay	1.88	1.95	2.16

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to IO	Fall delay	3.27	4.15	4.94	5.69
A to IO	Rise delay	3.31	4.29	5.18	6.05
EN to IO	Z0 delay	3.25	4.13	4.92	5.67
EN to IO	Z1 delay	3.27	4.24	5.14	6.00
TA to IO	Fall delay	3.60	4.48	5.27	6.03
TA to IO	Rise delay	3.58	4.56	5.45	6.32
TEN to IO	Z0 delay	3.56	4.44	5.23	5.98
TEN to IO	Z1 delay	3.58	4.55	5.45	6.31
TM to IO	Fall delay	3.78	4.66	5.45	6.20
TM to IO	Fall delay	3.61	4.49	5.28	6.04
TM to IO	Rise delay	4.02	4.99	5.89	6.75
TM to IO	Rise delay	3.48	4.45	5.35	6.21
TM to IO	Z0 delay	3.83	4.71	5.50	6.25
TM to IO	Z0 delay	3.60	4.48	5.27	6.02
TM to IO	Z1 delay	3.97	4.94	5.84	6.70
TM to IO	Z1 delay	3.60	4.58	5.47	6.34

CMOS035 MTC45200	TTL Five Volt tolerant Schmitt Trigger Bidir Pad Buffer, 8mA	BD8ST_FT

SYMBOL



BEHAVIOUR

A	EN	IO	ZI	IO
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
IO	5.526 pF

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

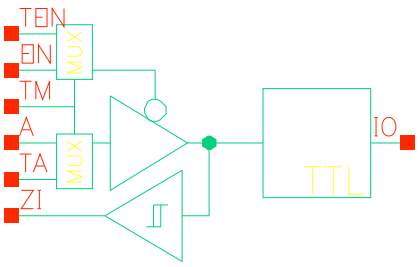
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.58	0.70	0.79	0.95
IO to ZI	Rise delay	0.75	0.85	0.94	1.11

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.04	1.10	1.28
EN to IO	1Z delay	1.34	1.39	1.56

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to IO	Fall delay	2.47	3.35	4.18	5.00
A to IO	Rise delay	2.22	2.97	3.69	4.40
EN to IO	Z0 delay	3.28	4.82	6.32	7.82
EN to IO	Z1 delay	2.21	2.96	3.68	4.39

CMOS035 MTC45200	TTL Five Volt tolerant Schmitt Trigger Bidir Pad Buffer, 8mA, with Test Pins	BD8STP_FT

SYMBOL



BEHAVIOUR

A	EN	IO	TM	TEN	TA	ZI	IO
-	-	1	1	1	-	1	
-	-	-	1	0	-	-	
-	1	1	0	-	-	1	
-	0	-	0	-	-	-	
-	-	-	1	0	1		1
-	-	-	1	1	-		Z
1	0	-	0	-	-		1
-	1	-	0	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
IO	5.526 pF
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	81 SL

CMOS035 MTC45200	TTL Five Volt tolerant Schmitt Trigger Bidir Pad Buffer, 8mA, with Test Pins	BD8STP_FT

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

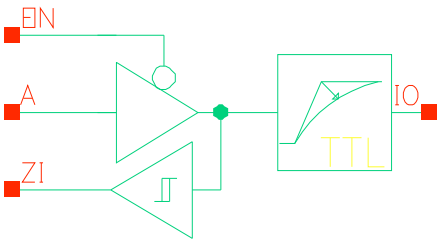
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.58	0.70	0.79	0.95
IO to ZI	Rise delay	0.75	0.85	0.94	1.11

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.04	1.10	1.28
EN to IO	1Z delay	1.34	1.39	1.56
TEN to IO	0Z delay	1.36	1.39	1.61
TEN to IO	1Z delay	1.61	1.65	1.85
TM to IO	0Z delay	1.76	1.82	2.04
TM to IO	1Z delay	2.01	2.08	2.29

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to IO	Fall delay	2.47	3.35	4.18	5.00
A to IO	Rise delay	2.22	2.97	3.69	4.40
EN to IO	Z0 delay	3.28	4.82	6.32	7.82
EN to IO	Z1 delay	2.21	2.96	3.68	4.39
TA to IO	Fall delay	2.81	3.68	4.51	5.33
TA to IO	Rise delay	2.50	3.24	3.96	4.67
TEN to IO	Z0 delay	3.66	5.20	6.70	8.20
TEN to IO	Z1 delay	2.58	3.33	4.05	4.76
TM to IO	Fall delay	2.98	3.86	4.69	5.51
TM to IO	Fall delay	2.81	3.68	4.52	5.33
TM to IO	Rise delay	2.93	3.68	4.39	5.10
TM to IO	Rise delay	2.39	3.14	3.85	4.57
TM to IO	Z0 delay	3.10	3.97	4.80	5.62
TM to IO	Z0 delay	2.81	3.69	4.52	5.34
TM to IO	Z1 delay	2.88	3.63	4.34	5.06
TM to IO	Z1 delay	2.55	3.29	4.01	4.72

CMOS035 MTC45200	TTL Schmitt Trigger Bidir Pad Buffer, 8mA, with Slew Rate Control	BD8STR

SYMBOL



BEHAVIOUR

A	EN	IO	ZI	IO
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
IO	5.639 pF

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

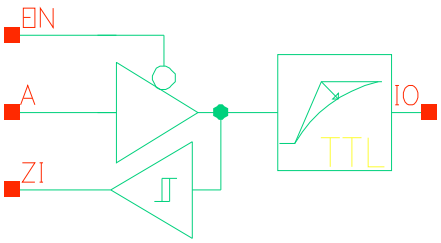
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.39	0.49	0.57	0.71
IO to ZI	Rise delay	0.36	0.45	0.54	0.71

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.01	1.06	1.22
EN to IO	1Z delay	1.25	1.30	1.44

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to IO	Fall delay	3.44	4.44	5.34	6.20
A to IO	Rise delay	3.11	3.96	4.73	5.46
EN to IO	Z0 delay	3.42	4.41	5.32	6.18
EN to IO	Z1 delay	3.07	3.92	4.69	5.42

CMOS035 MTC45200	TTL Five Volt tolerant Schmitt Trigger Bidir Pad Buffer, 8mA, with Slew Rate Control	BD8STR_FT

SYMBOL



BEHAVIOUR

A	EN	IO	ZI	IO
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
IO	5.526 pF

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

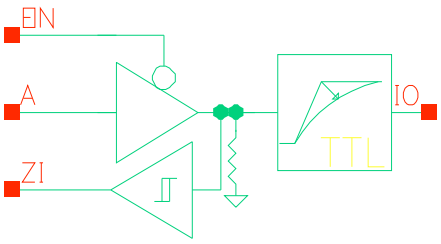
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.58	0.70	0.79	0.95
IO to ZI	Rise delay	0.75	0.85	0.94	1.11

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.04	1.10	1.28
EN to IO	1Z delay	1.34	1.39	1.56

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to IO	Fall delay	3.44	4.43	5.33	6.20
A to IO	Rise delay	3.13	3.99	4.76	5.49
EN to IO	Z0 delay	4.39	6.04	7.60	9.13
EN to IO	Z1 delay	3.12	3.98	4.75	5.49

CMOS035 MTC45200	TTL Five Volt tolerant Schmitt Trigger Bidir Pad Buffer with Active Pull-Down, 8mA, with Slew Rate Control	BD8STRD_FT

SYMBOL



BEHAVIOUR

A	EN	IO	ZI	IO
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
IO	5.523 pF

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

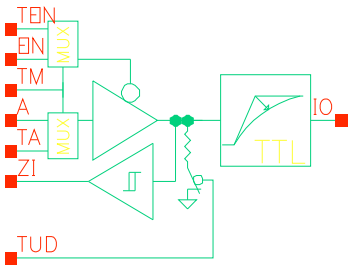
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.56	0.68	0.77	0.93
IO to ZI	Rise delay	0.82	0.92	1.01	1.18

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.04	1.10	1.28
EN to IO	1Z delay	1.33	1.39	1.55

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to IO	Fall delay	3.43	4.43	5.33	6.19
A to IO	Rise delay	3.13	3.99	4.76	5.49
EN to IO	Z0 delay	4.39	6.04	7.60	9.13
EN to IO	Z1 delay	3.12	3.98	4.75	5.49

CMOS035 MTC45200	TTL Five Volt tolerant Schmitt Trigger Bidir Pad Buffer with Active Pull-Down, 8mA, with Slew Rate Control, with Test Pins	BD8STRDQP_FT

SYMBOL



BEHAVIOUR

A	EN	IO	TM	TEN	TA	TUD	ZI	IO
-	-	1	1	1	-	-	1	
-	-	-	1	0	-	-	-	
-	1	1	0	-	-	-	1	
-	0	-	0	-	-	-	-	
-	-	-	1	0	1	-		1
-	-	-	1	1	-	-		Z
1	0	-	0	-	-	-		1
-	1	-	0	-	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
IO	5.526 pF
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
TUD	1.9 SL

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

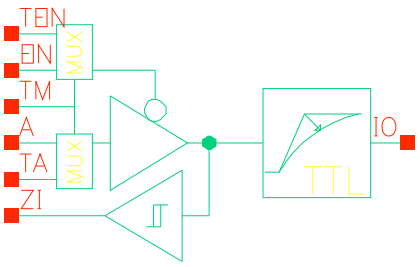
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.58	0.70	0.79	0.95
IO to ZI	Rise delay	0.83	0.93	1.01	1.18

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.04	1.10	1.28
EN to IO	1Z delay	1.34	1.39	1.56
TEN to IO	0Z delay	1.36	1.40	1.61
TEN to IO	1Z delay	1.61	1.65	1.85
TM to IO	0Z delay	1.76	1.83	2.04
TM to IO	1Z delay	2.01	2.07	2.29

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to IO	Fall delay	3.44	4.43	5.33	6.20
A to IO	Rise delay	3.13	3.99	4.76	5.49
EN to IO	Z0 delay	4.39	6.04	7.60	9.13
EN to IO	Z1 delay	3.12	3.98	4.75	5.49
TA to IO	Fall delay	3.77	4.77	5.67	6.53
TA to IO	Rise delay	3.40	4.26	5.03	5.77
TEN to IO	Z0 delay	4.77	6.42	7.98	9.51
TEN to IO	Z1 delay	3.49	4.35	5.12	5.86
TM to IO	Fall delay	3.95	4.94	5.84	6.71
TM to IO	Fall delay	3.78	4.77	5.67	6.54
TM to IO	Rise delay	3.84	4.70	5.46	6.20
TM to IO	Rise delay	3.30	4.16	4.93	5.66
TM to IO	Z0 delay	4.07	5.07	5.97	6.84
TM to IO	Z0 delay	3.79	4.79	5.69	6.56
TM to IO	Z1 delay	3.79	4.65	5.42	6.16
TM to IO	Z1 delay	3.45	4.31	5.08	5.82

CMOS035 MTC45200	TTL Schmitt Trigger Bidir Pad Buffer, 8mA, with Slew Rate Control, with Test Pins	BD8STRP

SYMBOL



BEHAVIOUR

A	EN	IO	TM	TEN	TA	ZI	IO
-	-	1	1	1	-	1	
-	-	-	1	0	-	-	
-	1	1	0	-	-	1	
-	0	-	0	-	-	-	
-	-	-	1	0	1		1
-	-	-	1	1	-		Z
1	0	-	0	-	-		1
-	1	-	0	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
IO	5.639 pF
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	81 SL

CMOS035 MTC45200	TTL Schmitt Trigger Bidir Pad Buffer, 8mA, with Slew Rate Control, with Test Pins	BD8STRP

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

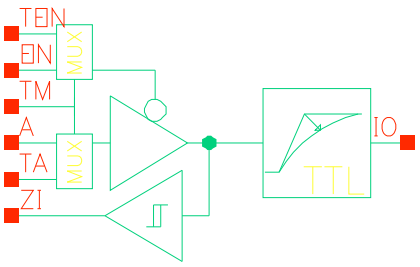
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.39	0.49	0.57	0.71
IO to ZI	Rise delay	0.36	0.45	0.54	0.71

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.01	1.06	1.22
EN to IO	1Z delay	1.25	1.30	1.44
TEN to IO	0Z delay	1.27	1.31	1.51
TEN to IO	1Z delay	1.47	1.51	1.71
TM to IO	0Z delay	1.68	1.74	1.96
TM to IO	1Z delay	1.88	1.94	2.15

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to IO	Fall delay	3.44	4.44	5.34	6.20
A to IO	Rise delay	3.11	3.96	4.73	5.46
EN to IO	Z0 delay	3.42	4.41	5.32	6.18
EN to IO	Z1 delay	3.07	3.92	4.69	5.42
TA to IO	Fall delay	3.78	4.77	5.67	6.54
TA to IO	Rise delay	3.39	4.24	5.00	5.74
TEN to IO	Z0 delay	3.73	4.73	5.63	6.49
TEN to IO	Z1 delay	3.38	4.23	5.00	5.73
TM to IO	Fall delay	3.95	4.95	5.85	6.71
TM to IO	Fall delay	3.78	4.78	5.68	6.54
TM to IO	Rise delay	3.82	4.67	5.44	6.17
TM to IO	Rise delay	3.28	4.13	4.90	5.63
TM to IO	Z0 delay	4.00	5.00	5.90	6.76
TM to IO	Z0 delay	3.77	4.77	5.67	6.53
TM to IO	Z1 delay	3.77	4.62	5.39	6.12
TM to IO	Z1 delay	3.40	4.25	5.02	5.75

CMOS035 MTC45200	TTL Five Volt tolerant Schmitt Trigger Bidir Pad Buffer, 8mA, with Slew Rate Control, with Test Pins	BD8STRP_FT

SYMBOL



BEHAVIOUR

A	EN	IO	TM	TEN	TA	ZI	IO
-	-	1	1	1	-	1	
-	-	-	1	0	-	-	
-	1	1	0	-	-	1	
-	0	-	0	-	-	-	
-	-	-	1	0	1		1
-	-	-	1	1	-		Z
1	0	-	0	-	-		1
-	1	-	0	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
IO	5.526 pF
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

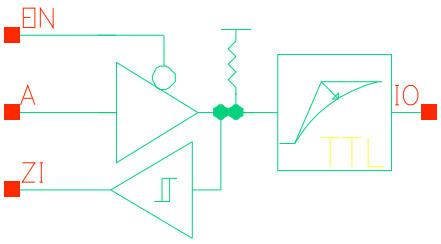
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.58	0.70	0.79	0.95
IO to ZI	Rise delay	0.75	0.85	0.94	1.11

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.04	1.10	1.28
EN to IO	1Z delay	1.34	1.39	1.56
TEN to IO	0Z delay	1.35	1.39	1.60
TEN to IO	1Z delay	1.61	1.65	1.85
TM to IO	0Z delay	1.76	1.82	2.04
TM to IO	1Z delay	2.01	2.07	2.29

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to IO	Fall delay	3.44	4.43	5.33	6.20
A to IO	Rise delay	3.13	3.99	4.76	5.49
EN to IO	Z0 delay	4.39	6.04	7.60	9.13
EN to IO	Z1 delay	3.12	3.98	4.75	5.49
TA to IO	Fall delay	3.77	4.77	5.67	6.53
TA to IO	Rise delay	3.40	4.26	5.03	5.77
TEN to IO	Z0 delay	4.77	6.42	7.98	9.51
TEN to IO	Z1 delay	3.49	4.35	5.12	5.85
TM to IO	Fall delay	3.95	4.94	5.84	6.71
TM to IO	Fall delay	3.78	4.77	5.67	6.54
TM to IO	Rise delay	3.84	4.69	5.46	6.20
TM to IO	Rise delay	3.30	4.16	4.92	5.66
TM to IO	Z0 delay	4.07	5.07	5.97	6.84
TM to IO	Z0 delay	3.79	4.79	5.69	6.56
TM to IO	Z1 delay	3.79	4.65	5.42	6.15
TM to IO	Z1 delay	3.46	4.32	5.09	5.82

CMOS035 MTC45200	TTL Five Volt tolerant Schmitt Trigger Bidir Pad Buffer with Active Pull-Up, 8mA, with Slew Rate Control	BD8STRU_FT

SYMBOL



BEHAVIOUR

A	EN	IO	ZI	IO
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
IO	5.528 pF

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

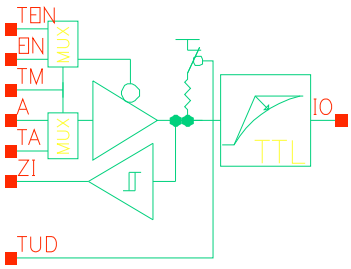
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.61	0.73	0.82	0.98
IO to ZI	Rise delay	0.71	0.81	0.90	1.07

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.04	1.10	1.28
EN to IO	1Z delay	1.34	1.40	1.57

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to IO	Fall delay	3.43	4.43	5.33	6.20
A to IO	Rise delay	3.13	3.99	4.75	5.49
EN to IO	Z0 delay	4.39	6.04	7.60	9.13
EN to IO	Z1 delay	3.12	3.98	4.75	5.48

CMOS035 MTC45200	TTL Five Volt tolerant Schmitt Trigger Bidir Pad Buffer with Active Pull-Up, 8mA, with Slew Rate Control, with Test Pins	BD8STRUQP_FT

SYMBOL



BEHAVIOUR

A	EN	IO	TM	TEN	TA	TUD	ZI	IO
-	-	1	1	1	-	-	1	
-	-	-	1	0	-	-	-	
-	1	1	0	-	-	-	1	
-	0	-	0	-	-	-	-	
-	-	-	1	0	1	-		1
-	-	-	1	1	-	-		Z
1	0	-	0	-	-	-		1
-	1	-	0	-	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
IO	5.526 pF
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
TUD	2.3 SL

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

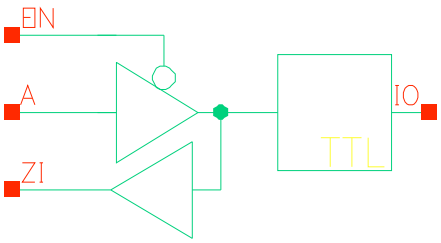
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.61	0.73	0.82	0.98
IO to ZI	Rise delay	0.75	0.85	0.94	1.11

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.04	1.10	1.28
EN to IO	1Z delay	1.34	1.40	1.57
TEN to IO	0Z delay	1.35	1.39	1.60
TEN to IO	1Z delay	1.61	1.65	1.86
TM to IO	0Z delay	1.76	1.82	2.04
TM to IO	1Z delay	2.02	2.08	2.30

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to IO	Fall delay	3.43	4.43	5.33	6.20
A to IO	Rise delay	3.13	3.99	4.76	5.49
EN to IO	Z0 delay	4.39	6.04	7.60	9.13
EN to IO	Z1 delay	3.12	3.98	4.75	5.49
TA to IO	Fall delay	3.77	4.76	5.67	6.53
TA to IO	Rise delay	3.40	4.26	5.03	5.77
TEN to IO	Z0 delay	4.77	6.42	7.98	9.51
TEN to IO	Z1 delay	3.49	4.35	5.12	5.85
TM to IO	Fall delay	3.94	4.94	5.84	6.71
TM to IO	Fall delay	3.77	4.77	5.67	6.54
TM to IO	Rise delay	3.84	4.69	5.46	6.20
TM to IO	Rise delay	3.30	4.16	4.92	5.66
TM to IO	Z0 delay	4.07	5.07	5.97	6.84
TM to IO	Z0 delay	3.79	4.79	5.69	6.56
TM to IO	Z1 delay	3.79	4.65	5.42	6.15
TM to IO	Z1 delay	3.46	4.32	5.09	5.82

CMOS035 MTC45200	TTL Five Volt tolerant Bidir Pad Buffer, 8mA	BD8T_FT

SYMBOL



BEHAVIOUR

A	EN	IO	ZI	IO
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
IO	5.530 pF

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

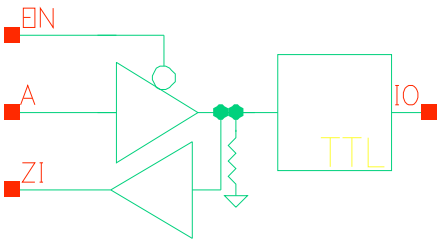
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.31	0.40	0.48	0.62
IO to ZI	Rise delay	0.34	0.43	0.51	0.68

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.04	1.10	1.28
EN to IO	1Z delay	1.34	1.39	1.56

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to IO	Fall delay	2.47	3.35	4.18	5.00
A to IO	Rise delay	2.22	2.97	3.69	4.40
EN to IO	Z0 delay	3.28	4.82	6.32	7.82
EN to IO	Z1 delay	2.21	2.96	3.68	4.39

CMOS035 MTC45200	TTL Five Volt tolerant Bidir Pad Buffer with Active Pull-Down, 8mA	BD8TD_FT

SYMBOL



BEHAVIOUR

A	EN	IO	ZI	IO
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
IO	5.529 pF

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

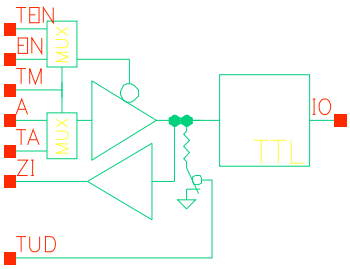
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.31	0.40	0.48	0.62
IO to ZI	Rise delay	0.33	0.42	0.51	0.68

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.04	1.10	1.28
EN to IO	1Z delay	1.34	1.39	1.56

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to IO	Fall delay	2.47	3.35	4.18	5.00
A to IO	Rise delay	2.22	2.97	3.69	4.40
EN to IO	Z0 delay	3.28	4.82	6.32	7.82
EN to IO	Z1 delay	2.21	2.96	3.68	4.39

CMOS035 MTC45200	TTL Five Volt tolerant Bidir Pad Buffer with Active Pull-Down, 8mA, with Test Pins	BD8TDQP_FT

SYMBOL



BEHAVIOUR

A	EN	IO	TM	TEN	TA	TUD	ZI	IO
-	-	1	1	1	-	-	1	
-	-	-	1	0	-	-	-	
-	1	1	0	-	-	-	1	
-	0	-	0	-	-	-	-	
-	-	-	1	0	1	-		1
-	-	-	1	1	-	-		Z
1	0	-	0	-	-	-		1
-	1	-	0	-	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
IO	5.535 pF
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
TUD	1.9 SL

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.31	0.40	0.48	0.62

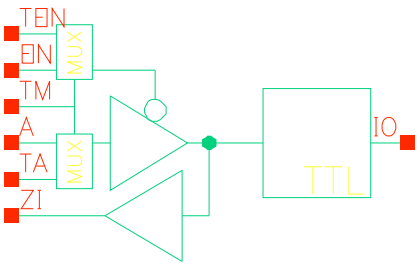
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Rise delay	0.34	0.43	0.51	0.68

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.04	1.10	1.28
EN to IO	1Z delay	1.34	1.39	1.56
TEN to IO	0Z delay	1.31	1.35	1.56
TEN to IO	1Z delay	1.56	1.60	1.80
TM to IO	0Z delay	1.48	1.54	1.76
TM to IO	1Z delay	2.01	2.08	2.29

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to IO	Fall delay	2.48	3.35	4.18	5.00
A to IO	Rise delay	2.22	2.97	3.69	4.40
EN to IO	Z0 delay	3.29	4.82	6.33	7.82
EN to IO	Z1 delay	2.21	2.96	3.68	4.39
TA to IO	Fall delay	2.81	3.68	4.52	5.33
TA to IO	Rise delay	2.46	3.20	3.92	4.63
TEN to IO	Z0 delay	3.66	5.20	6.71	8.20
TEN to IO	Z1 delay	2.58	3.33	4.05	4.76
TM to IO	Fall delay	2.99	3.86	4.69	5.51
TM to IO	Fall delay	2.82	3.69	4.52	5.34
TM to IO	Rise delay	2.93	3.68	4.39	5.10
TM to IO	Rise delay	2.39	3.14	3.85	4.56
TM to IO	Z0 delay	3.10	3.97	4.81	5.62
TM to IO	Z0 delay	2.82	3.69	4.52	5.34
TM to IO	Z1 delay	2.76	3.51	4.22	4.93
TM to IO	Z1 delay	2.54	3.29	4.01	4.72

CMOS035 MTC45200	TTL Five Volt tolerant Bidir Pad Buffer, 8mA, with Test Pins	BD8TP_FT

SYMBOL



BEHAVIOUR

A	EN	IO	TM	TEN	TA	ZI	IO
-	-	1	1	1	-	1	
-	-	-	1	0	-	-	
-	1	1	0	-	-	1	
-	0	-	0	-	-	-	
-	-	-	1	0	1		1
-	-	-	1	1	-		Z
1	0	-	0	-	-		1
-	1	-	0	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
IO	5.530 pF
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

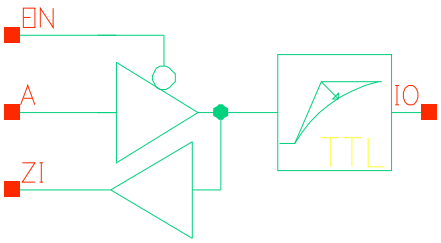
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.31	0.40	0.48	0.62
IO to ZI	Rise delay	0.34	0.43	0.51	0.68

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.04	1.10	1.28
EN to IO	1Z delay	1.34	1.39	1.56
TEN to IO	0Z delay	1.36	1.39	1.61
TEN to IO	1Z delay	1.61	1.65	1.85
TM to IO	0Z delay	1.76	1.82	2.04
TM to IO	1Z delay	2.01	2.08	2.29

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to IO	Fall delay	2.47	3.35	4.18	5.00
A to IO	Rise delay	2.22	2.97	3.69	4.40
EN to IO	Z0 delay	3.28	4.82	6.32	7.82
EN to IO	Z1 delay	2.21	2.96	3.68	4.39
TA to IO	Fall delay	2.81	3.68	4.51	5.33
TA to IO	Rise delay	2.50	3.24	3.96	4.67
TEN to IO	Z0 delay	3.66	5.20	6.70	8.20
TEN to IO	Z1 delay	2.58	3.33	4.05	4.76
TM to IO	Fall delay	2.98	3.86	4.69	5.51
TM to IO	Fall delay	2.81	3.69	4.52	5.34
TM to IO	Rise delay	2.93	3.68	4.39	5.10
TM to IO	Rise delay	2.39	3.14	3.85	4.56
TM to IO	Z0 delay	3.10	3.97	4.80	5.62
TM to IO	Z0 delay	2.81	3.69	4.52	5.34
TM to IO	Z1 delay	2.88	3.63	4.34	5.06
TM to IO	Z1 delay	2.55	3.29	4.01	4.72

CMOS035 MTC45200	TTL Five Volt tolerant Bidir Pad Buffer, 8mA, with Slew Rate Control	BD8TR_FT

SYMBOL



BEHAVIOUR

A	EN	IO	ZI	IO
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
IO	5.530 pF

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

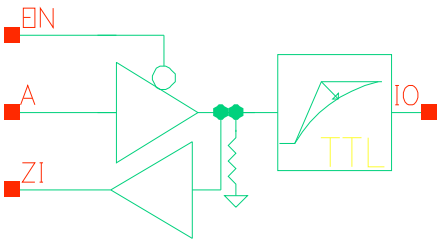
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.31	0.40	0.48	0.62
IO to ZI	Rise delay	0.34	0.43	0.51	0.68

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.04	1.10	1.28
EN to IO	1Z delay	1.34	1.39	1.56

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to IO	Fall delay	3.44	4.43	5.33	6.20
A to IO	Rise delay	3.13	3.99	4.76	5.49
EN to IO	Z0 delay	4.39	6.04	7.60	9.13
EN to IO	Z1 delay	3.12	3.98	4.75	5.49

CMOS035 MTC45200	TTL Five Volt tolerant Bidir Pad Buffer with Active Pull-Down, 8mA, with Slew Rate Control	BD8TRD_FT

SYMBOL



BEHAVIOUR

A	EN	IO	ZI	IO
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
IO	5.528 pF

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

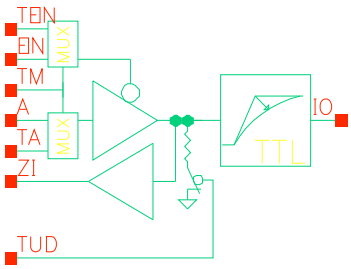
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.30	0.39	0.47	0.61
IO to ZI	Rise delay	0.35	0.44	0.52	0.69

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.04	1.10	1.28
EN to IO	1Z delay	1.33	1.38	1.55

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to IO	Fall delay	3.43	4.43	5.33	6.19
A to IO	Rise delay	3.13	3.99	4.76	5.49
EN to IO	Z0 delay	4.39	6.04	7.60	9.12
EN to IO	Z1 delay	3.12	3.98	4.75	5.49

CMOS035 MTC45200	TTL Five Volt tolerant Bidir Pad Buffer with Active Pull-Down, 8mA, with Slew Rate Control, with Test Pins	BD8TRDQP_FT

SYMBOL



BEHAVIOUR

A	EN	IO	TM	TEN	TA	TUD	ZI	IO
-	-	1	1	1	-	-	1	
-	-	-	1	0	-	-	-	
-	1	1	0	-	-	-	1	
-	0	-	0	-	-	-	-	
-	-	-	1	0	1	-		1
-	-	-	1	1	-	-		Z
1	0	-	0	-	-	-		1
-	1	-	0	-	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
IO	5.530 pF
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
TUD	1.9 SL

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

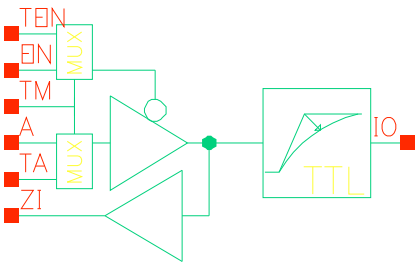
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.31	0.40	0.48	0.62
IO to ZI	Rise delay	0.35	0.44	0.52	0.69

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.04	1.10	1.28
EN to IO	1Z delay	1.34	1.39	1.56
TEN to IO	0Z delay	1.36	1.40	1.61
TEN to IO	1Z delay	1.61	1.65	1.85
TM to IO	0Z delay	1.76	1.83	2.04
TM to IO	1Z delay	2.01	2.08	2.29

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to IO	Fall delay	3.44	4.43	5.33	6.20
A to IO	Rise delay	3.13	3.99	4.76	5.49
EN to IO	Z0 delay	4.39	6.04	7.60	9.13
EN to IO	Z1 delay	3.12	3.98	4.75	5.49
TA to IO	Fall delay	3.77	4.77	5.67	6.53
TA to IO	Rise delay	3.40	4.26	5.03	5.77
TEN to IO	Z0 delay	4.77	6.42	7.98	9.51
TEN to IO	Z1 delay	3.49	4.35	5.12	5.86
TM to IO	Fall delay	3.95	4.94	5.84	6.71
TM to IO	Fall delay	3.78	4.77	5.68	6.54
TM to IO	Rise delay	3.83	4.69	5.46	6.20
TM to IO	Rise delay	3.30	4.16	4.92	5.66
TM to IO	Z0 delay	4.07	5.07	5.97	6.84
TM to IO	Z0 delay	3.79	4.79	5.69	6.56
TM to IO	Z1 delay	3.79	4.65	5.42	6.16
TM to IO	Z1 delay	3.45	4.31	5.08	5.82

CMOS035 MTC45200	TTL Five Volt tolerant Bidir Pad Buffer, 8mA, with Slew Rate Control, with Test Pins	BD8TRP_FT

SYMBOL



BEHAVIOUR

A	EN	IO	TM	TEN	TA	ZI	IO
-	-	1	1	1	-	1	
-	-	-	1	0	-	-	
-	1	1	0	-	-	1	
-	0	-	0	-	-	-	
-	-	-	1	0	1		1
-	-	-	1	1	-		Z
1	0	-	0	-	-		1
-	1	-	0	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
IO	5.530 pF
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

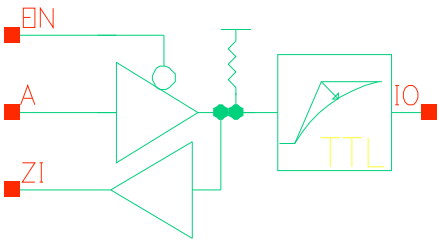
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.31	0.40	0.48	0.62
IO to ZI	Rise delay	0.34	0.43	0.51	0.68

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.04	1.10	1.28
EN to IO	1Z delay	1.34	1.39	1.56
TEN to IO	0Z delay	1.35	1.39	1.60
TEN to IO	1Z delay	1.61	1.65	1.85
TM to IO	0Z delay	1.76	1.82	2.04
TM to IO	1Z delay	2.01	2.08	2.29

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to IO	Fall delay	3.44	4.43	5.33	6.20
A to IO	Rise delay	3.13	3.99	4.76	5.49
EN to IO	Z0 delay	4.39	6.04	7.60	9.13
EN to IO	Z1 delay	3.12	3.98	4.75	5.49
TA to IO	Fall delay	3.77	4.77	5.67	6.53
TA to IO	Rise delay	3.40	4.26	5.03	5.77
TEN to IO	Z0 delay	4.77	6.42	7.98	9.51
TEN to IO	Z1 delay	3.49	4.35	5.12	5.85
TM to IO	Fall delay	3.95	4.94	5.84	6.71
TM to IO	Fall delay	3.78	4.77	5.68	6.54
TM to IO	Rise delay	3.83	4.69	5.46	6.20
TM to IO	Rise delay	3.30	4.16	4.92	5.66
TM to IO	Z0 delay	4.07	5.07	5.97	6.84
TM to IO	Z0 delay	3.79	4.79	5.69	6.56
TM to IO	Z1 delay	3.79	4.65	5.42	6.15
TM to IO	Z1 delay	3.45	4.31	5.08	5.82

CMOS035 MTC45200	TTL Five Volt tolerant Bidir Pad Buffer with Active Pull-Up, 8mA, with Slew Rate Control	BD8TRU_FT

SYMBOL



BEHAVIOUR

A	EN	IO	ZI	IO
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
IO	5.532 pF

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

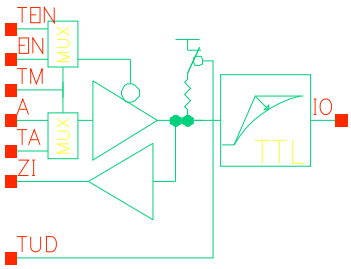
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.33	0.42	0.50	0.64
IO to ZI	Rise delay	0.33	0.42	0.51	0.68

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.04	1.10	1.28
EN to IO	1Z delay	1.34	1.40	1.57

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to IO	Fall delay	3.44	4.43	5.33	6.20
A to IO	Rise delay	3.13	3.99	4.75	5.49
EN to IO	Z0 delay	4.39	6.04	7.60	9.13
EN to IO	Z1 delay	3.12	3.98	4.75	5.48

CMOS035 MTC45200	TTL Five Volt tolerant Bidir Pad Buffer with Active Pull-Up, 8mA, with Slew Rate Control, with Test Pins	BD8TRUQP_FT

SYMBOL



BEHAVIOUR

A	EN	IO	TM	TEN	TA	TUD	ZI	IO
-	-	1	1	1	-	-	1	
-	-	-	1	0	-	-	-	
-	1	1	0	-	-	-	1	
-	0	-	0	-	-	-	-	
-	-	-	1	0	1	-		1
-	-	-	1	1	-	-		Z
1	0	-	0	-	-	-		1
-	1	-	0	-	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
IO	5.531 pF
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
TUD	2.3 SL

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

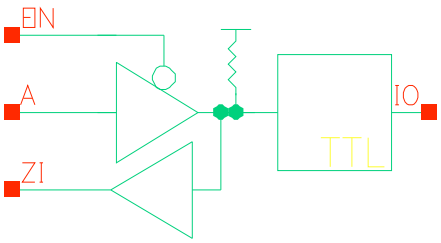
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.33	0.42	0.50	0.64
IO to ZI	Rise delay	0.34	0.43	0.51	0.68

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.04	1.10	1.28
EN to IO	1Z delay	1.34	1.40	1.57
TEN to IO	0Z delay	1.35	1.39	1.60
TEN to IO	1Z delay	1.61	1.65	1.86
TM to IO	0Z delay	1.76	1.82	2.04
TM to IO	1Z delay	2.02	0.79	1.19

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to IO	Fall delay	3.43	4.43	5.33	6.20
A to IO	Rise delay	3.13	3.99	4.76	5.49
EN to IO	Z0 delay	4.39	6.04	7.60	9.13
EN to IO	Z1 delay	3.12	3.98	4.75	5.49
TA to IO	Fall delay	3.77	4.76	5.67	6.53
TA to IO	Rise delay	3.40	4.26	5.03	5.77
TEN to IO	Z0 delay	4.77	6.42	7.98	9.51
TEN to IO	Z1 delay	3.49	4.35	5.12	5.85
TM to IO	Fall delay	3.94	4.94	5.84	6.71
TM to IO	Fall delay	3.77	4.77	5.67	6.54
TM to IO	Rise delay	3.83	4.69	5.46	6.20
TM to IO	Rise delay	3.30	4.16	4.92	5.66
TM to IO	Z0 delay	4.07	5.07	5.97	6.84
TM to IO	Z0 delay	3.79	4.79	5.69	6.56
TM to IO	Z1 delay	3.79	4.65	5.42	6.15
TM to IO	Z1 delay	3.45	4.31	5.08	5.82

CMOS035 MTC45200	TTL Five Volt tolerant Bidir Pad Buffer with Active Pull-Up, 8mA	BD8TU_FT

SYMBOL



BEHAVIOUR

A	EN	IO	ZI	IO
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
IO	5.529 pF

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

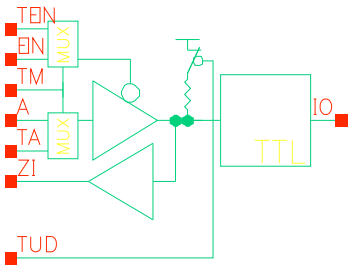
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.31	0.40	0.48	0.62
IO to ZI	Rise delay	0.33	0.42	0.51	0.68

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.04	1.10	1.28
EN to IO	1Z delay	1.34	1.39	1.56

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to IO	Fall delay	2.47	3.35	4.18	5.00
A to IO	Rise delay	2.22	2.97	3.69	4.40
EN to IO	Z0 delay	3.28	4.82	6.32	7.82
EN to IO	Z1 delay	2.21	2.96	3.68	4.39

CMOS035 MTC45200	TTL Five Volt tolerant Bidir Pad Buffer with Active Pull-Up, 8mA, with Test Pins	BD8TUQP_FT

SYMBOL



BEHAVIOUR

A	EN	IO	TM	TEN	TA	TUD	ZI	IO
-	-	1	1	1	-	-	1	
-	-	-	1	0	-	-	-	
-	1	1	0	-	-	-	1	
-	0	-	0	-	-	-	-	
-	-	-	1	0	1	-		1
-	-	-	1	1	-	-		Z
1	0	-	0	-	-	-		1
-	1	-	0	-	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
IO	5.536 pF
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
TUD	2.3 SL

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Fall delay	0.32	0.41	0.49	0.63

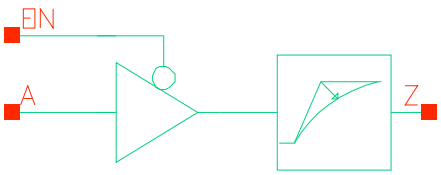
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
IO to ZI	Rise delay	0.34	0.43	0.51	0.68

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	1.04	1.10	1.28
EN to IO	1Z delay	1.34	1.39	1.56
TEN to IO	0Z delay	1.31	1.35	1.56
TEN to IO	1Z delay	1.56	1.60	1.80
TM to IO	0Z delay	1.48	1.54	1.76
TM to IO	1Z delay	2.01	2.08	2.29

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to IO	Fall delay	2.48	3.35	4.18	5.00
A to IO	Rise delay	2.22	2.97	3.69	4.40
EN to IO	Z0 delay	3.28	4.82	6.33	7.82
EN to IO	Z1 delay	2.21	2.96	3.68	4.39
TA to IO	Fall delay	2.81	3.68	4.52	5.33
TA to IO	Rise delay	2.46	3.20	3.92	4.63
TEN to IO	Z0 delay	3.66	5.20	6.71	8.20
TEN to IO	Z1 delay	2.58	3.33	4.05	4.76
TM to IO	Fall delay	2.99	3.86	4.69	5.51
TM to IO	Fall delay	2.81	3.69	4.52	5.34
TM to IO	Rise delay	2.93	3.68	4.39	5.10
TM to IO	Rise delay	2.39	3.14	3.85	4.56
TM to IO	Z0 delay	3.10	3.97	4.80	5.62
TM to IO	Z0 delay	2.82	3.69	4.52	5.34
TM to IO	Z1 delay	2.76	3.51	4.22	4.93
TM to IO	Z1 delay	2.54	3.29	4.01	4.72

CMOS035 MTC45200	CMOS Tristate Output Pad Buffer, 2mA, with Slew Rate Control	BT2CR

SYMBOL



BEHAVIOUR

EN	A	Z
1	-	Z
0	1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
Z	2.810 pF

OUTPUT Pin	Max. load
Z	50.000 pF

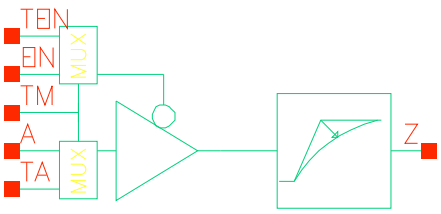
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to Z	0Z delay	1.08	1.13	1.29
EN to Z	1Z delay	1.35	1.39	1.54

Timing/Load		12.50pF	25.00pF	37.50pF	50.00pF
A to Z	Fall delay	3.63	4.53	5.33	6.09
A to Z	Rise delay	3.54	4.53	5.43	6.31
EN to Z	Z0 delay	3.61	4.51	5.31	6.07
EN to Z	Z1 delay	3.50	4.49	5.39	6.26

CMOS035 MTC45200	CMOS Tristate Output Pad Buffer, 2mA, with Slew Rate Control, with Test Pins	BT2CRP

SYMBOL



BEHAVIOUR

EN	A	TM	TEN	TA	Z
-	-	1	0	1	1
1	-	0	-	-	Z
0	1	0	-	-	1
-	-	1	1	-	Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
Z	2.810 pF

OUTPUT Pin	Max. load
Z	50.000 pF

CMOS035 MTC45200	CMOS Tristate Output Pad Buffer, 2mA, with Slew Rate Control, with Test Pins	BT2CRP

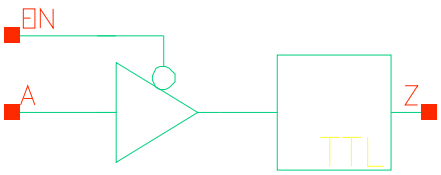
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to Z	0Z delay	1.08	1.13	1.29
EN to Z	1Z delay	1.35	1.39	1.54
TEN to Z	0Z delay	1.34	1.38	1.58
TEN to Z	1Z delay	1.57	1.61	1.80
TM to Z	0Z delay	1.74	1.81	2.02
TM to Z	1Z delay	1.98	2.04	2.25

Timing/Load		12.50pF	25.00pF	37.50pF	50.00pF
A to Z	Fall delay	3.63	4.53	5.33	6.09
A to Z	Rise delay	3.54	4.53	5.43	6.31
EN to Z	Z0 delay	3.61	4.51	5.31	6.07
EN to Z	Z1 delay	3.50	4.49	5.39	6.26
TA to Z	Fall delay	3.96	4.86	5.67	6.43
TA to Z	Rise delay	3.82	4.80	5.71	6.58
TEN to Z	Z0 delay	3.92	4.82	5.62	6.38
TEN to Z	Z1 delay	3.81	4.80	5.70	6.57
TM to Z	Fall delay	4.14	5.04	5.84	6.60
TM to Z	Fall delay	3.97	4.87	5.68	6.44
TM to Z	Rise delay	4.25	5.24	6.14	7.01
TM to Z	Rise delay	3.71	4.70	5.60	6.47
TM to Z	Z0 delay	4.19	5.09	5.89	6.66
TM to Z	Z0 delay	3.96	4.86	5.67	6.43
TM to Z	Z1 delay	4.20	5.19	6.09	6.96
TM to Z	Z1 delay	3.83	4.82	5.72	6.59

CMOS035 MTC45200	TTL Five Volt tolerant Tristate Output Pad Buffer, 3mA	BT3_FT

SYMBOL



BEHAVIOUR

EN	A	Z
1	-	Z
0	1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
Z	3.707 pF

OUTPUT Pin	Max. load
Z	75.000 pF

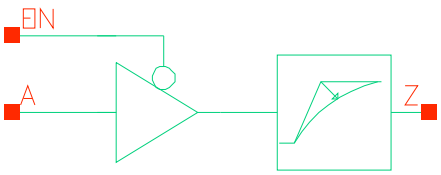
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to Z	0Z delay	1.03	1.08	1.26
EN to Z	1Z delay	1.43	1.49	1.66

Timing/Load		18.75pF	37.50pF	56.25pF	75.00pF
A to Z	Fall delay	2.53	3.39	4.22	5.04
A to Z	Rise delay	2.34	3.09	3.81	4.52
EN to Z	Z0 delay	3.38	4.91	6.41	7.90
EN to Z	Z1 delay	2.33	3.08	3.80	4.51

CMOS035 MTC45200	CMOS Tristate Output Pad Buffer, 3mA, with Slew Rate Control	BT3CR

SYMBOL



BEHAVIOUR

EN	A	Z
1	-	Z
0	1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
Z	3.492 pF

OUTPUT Pin	Max. load
Z	75.000 pF

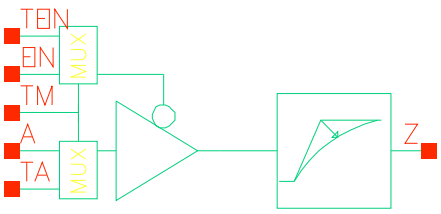
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to Z	0Z delay	1.00	1.05	1.21
EN to Z	1Z delay	1.33	1.38	1.52

Timing/Load		18.75pF	37.50pF	56.25pF	75.00pF
A to Z	Fall delay	3.30	4.18	4.96	5.71
A to Z	Rise delay	3.49	4.47	5.38	6.25
EN to Z	Z0 delay	3.28	4.15	4.93	5.68
EN to Z	Z1 delay	3.44	4.43	5.33	6.20

CMOS035 MTC45200	CMOS Tristate Output Pad Buffer, 3mA, with Slew Rate Control, with Test Pins	BT3CRP

SYMBOL



BEHAVIOUR

EN	A	TM	TEN	TA	Z
-	-	1	0	1	1
1	-	0	-	-	Z
0	1	0	-	-	1
-	-	1	1	-	Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
Z	3.492 pF

OUTPUT Pin	Max. load
Z	75.000 pF

CMOS035 MTC45200	CMOS Tristate Output Pad Buffer, 3mA, with Slew Rate Control, with Test Pins	BT3CRP

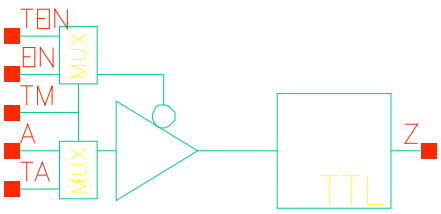
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to Z	0Z delay	1.00	1.05	1.21
EN to Z	1Z delay	1.33	1.38	1.52
TEN to Z	0Z delay	1.26	1.30	1.50
TEN to Z	1Z delay	1.55	1.59	1.79
TM to Z	0Z delay	1.66	1.73	1.94
TM to Z	1Z delay	1.96	2.02	2.24

Timing/Load		18.75pF	37.50pF	56.25pF	75.00pF
A to Z	Fall delay	3.30	4.18	4.96	5.70
A to Z	Rise delay	3.48	4.47	5.38	6.25
EN to Z	Z0 delay	3.28	4.15	4.93	5.68
EN to Z	Z1 delay	3.44	4.43	5.33	6.20
TA to Z	Fall delay	3.64	4.51	5.29	6.04
TA to Z	Rise delay	3.76	4.75	5.65	6.52
TEN to Z	Z0 delay	3.59	4.46	5.25	6.00
TEN to Z	Z1 delay	3.75	4.74	5.64	6.51
TM to Z	Fall delay	3.81	4.68	5.47	6.22
TM to Z	Fall delay	3.64	4.51	5.30	6.05
TM to Z	Rise delay	4.19	5.18	6.08	6.95
TM to Z	Rise delay	3.65	4.64	5.54	6.41
TM to Z	Z0 delay	3.86	4.73	5.52	6.27
TM to Z	Z0 delay	3.63	4.50	5.29	6.04
TM to Z	Z1 delay	4.14	5.13	6.03	6.90
TM to Z	Z1 delay	3.77	4.76	5.66	6.53

CMOS035 MTC45200	TTL Five Volt tolerant Tristate Output Pad Buffer, 3mA, with Test Pins	BT3P_FT

SYMBOL



BEHAVIOUR

EN	A	TM	TEN	TA	Z
-	-	1	0	1	1
1	-	0	-	-	Z
0	1	0	-	-	1
-	-	1	1	-	Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
Z	3.707 pF

OUTPUT Pin	Max. load
Z	75.000 pF

CMOS035 MTC45200	TTL Five Volt tolerant Tristate Output Pad Buffer, 3mA, with Test Pins	BT3P_FT

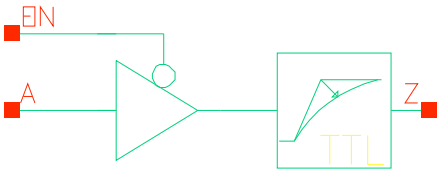
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to Z	0Z delay	1.03	1.08	1.26
EN to Z	1Z delay	1.43	1.49	1.66
TEN to Z	0Z delay	1.34	1.38	1.59
TEN to Z	1Z delay	1.70	1.74	1.95
TM to Z	0Z delay	1.74	1.81	2.02
TM to Z	1Z delay	2.11	2.17	2.38

Timing/Load		18.75pF	37.50pF	56.25pF	75.00pF
A to Z	Fall delay	2.53	3.39	4.22	5.04
A to Z	Rise delay	2.34	3.09	3.81	4.52
EN to Z	Z0 delay	3.38	4.91	6.41	7.90
EN to Z	Z1 delay	2.33	3.08	3.80	4.51
TA to Z	Fall delay	2.87	3.73	4.56	5.37
TA to Z	Rise delay	2.62	3.37	4.09	4.80
TEN to Z	Z0 delay	3.76	5.29	6.79	8.28
TEN to Z	Z1 delay	2.70	3.45	4.17	4.88
TM to Z	Fall delay	3.04	3.90	4.73	5.54
TM to Z	Fall delay	2.87	3.73	4.56	5.37
TM to Z	Rise delay	3.05	3.80	4.52	5.23
TM to Z	Rise delay	2.51	3.26	3.98	4.69
TM to Z	Z0 delay	3.15	4.02	4.84	5.66
TM to Z	Z0 delay	2.87	3.73	4.56	5.37
TM to Z	Z1 delay	3.00	3.75	4.47	5.18
TM to Z	Z1 delay	2.67	3.41	4.13	4.84

CMOS035 MTC45200	TTL Five Volt tolerant Tristate Output Pad Buffer, 3mA, with Slew Rate Control	BT3R_FT

SYMBOL



BEHAVIOUR

EN	A	Z
1	-	Z
0	1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
Z	3.706 pF

OUTPUT Pin	Max. load
Z	75.000 pF

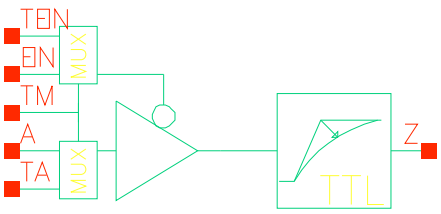
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to Z	0Z delay	1.03	1.08	1.26
EN to Z	1Z delay	1.44	1.49	1.66

Timing/Load		18.75pF	37.50pF	56.25pF	75.00pF
A to Z	Fall delay	3.49	4.47	5.36	6.22
A to Z	Rise delay	3.29	4.16	4.94	5.68
EN to Z	Z0 delay	4.48	6.12	7.67	9.19
EN to Z	Z1 delay	3.29	4.16	4.93	5.68

CMOS035 MTC45200	TTL Five Volt tolerant Tristate Output Pad Buffer, 3mA, with Slew Rate Control, with Test Pins	BT3RP_FT

SYMBOL



BEHAVIOUR

EN	A	TM	TEN	TA	Z
-	-	1	0	1	1
1	-	0	-	-	Z
0	1	0	-	-	1
-	-	1	1	-	Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
Z	3.706 pF

OUTPUT Pin	Max. load
Z	75.000 pF

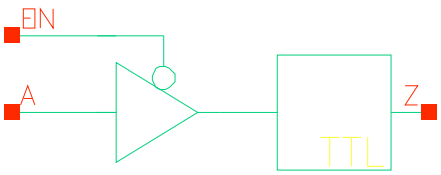
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to Z	0Z delay	1.03	1.08	1.26
EN to Z	1Z delay	1.44	1.49	1.66
TEN to Z	0Z delay	1.34	1.38	1.59
TEN to Z	1Z delay	1.70	1.74	1.95
TM to Z	0Z delay	1.74	1.81	2.02
TM to Z	1Z delay	2.11	2.17	2.39

Timing/Load		18.75pF	37.50pF	56.25pF	75.00pF
A to Z	Fall delay	3.49	4.47	5.36	6.22
A to Z	Rise delay	3.29	4.16	4.94	5.68
EN to Z	Z0 delay	4.48	6.12	7.67	9.19
EN to Z	Z1 delay	3.29	4.16	4.93	5.68
TA to Z	Fall delay	3.82	4.81	5.70	6.56
TA to Z	Rise delay	3.57	4.44	5.21	5.96
TEN to Z	Z0 delay	4.86	6.50	8.05	9.57
TEN to Z	Z1 delay	3.65	4.52	5.30	6.04
TM to Z	Fall delay	4.00	4.98	5.87	6.73
TM to Z	Fall delay	3.83	4.81	5.71	6.56
TM to Z	Rise delay	4.00	4.87	5.65	6.39
TM to Z	Rise delay	3.46	4.33	5.11	5.85
TM to Z	Z0 delay	4.12	5.11	6.00	6.86
TM to Z	Z0 delay	3.84	4.83	5.72	6.58
TM to Z	Z1 delay	3.95	4.82	5.60	6.34
TM to Z	Z1 delay	3.62	4.49	5.27	6.01

CMOS035 MTC45200	TTL Five Volt tolerant Tristate Output Pad Buffer, 4mA	BT4_FT

SYMBOL



BEHAVIOUR

EN	A	Z
1	-	Z
0	1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
Z	3.819 pF

OUTPUT Pin	Max. load
Z	100.000 pF

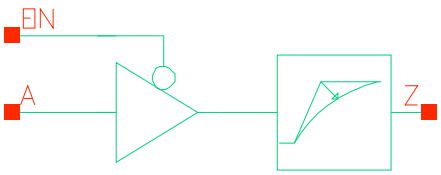
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to Z	0Z delay	1.09	1.14	1.32
EN to Z	1Z delay	1.41	1.47	1.64

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to Z	Fall delay	2.61	3.49	4.32	5.14
A to Z	Rise delay	2.30	3.05	3.76	4.48
EN to Z	Z0 delay	3.45	4.99	6.50	7.99
EN to Z	Z1 delay	2.29	3.04	3.75	4.47

CMOS035 MTC45200	CMOS Tristate Output Pad Buffer, 4mA, with Slew Rate Control	BT4CR

SYMBOL



BEHAVIOUR

EN	A	Z
1	-	Z
0	1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
Z	3.633 pF

OUTPUT Pin	Max. load
Z	100.000 pF

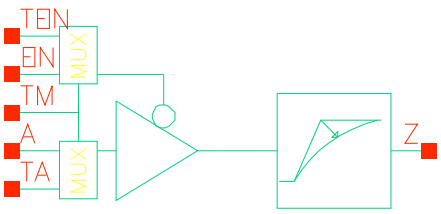
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to Z	0Z delay	1.06	1.11	1.27
EN to Z	1Z delay	1.31	1.36	1.51

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to Z	Fall delay	3.47	4.37	5.17	5.93
A to Z	Rise delay	3.42	4.41	5.31	6.18
EN to Z	Z0 delay	3.44	4.35	5.14	5.90
EN to Z	Z1 delay	3.37	4.36	5.27	6.14

CMOS035 MTC45200	CMOS Tristate Output Pad Buffer, 4mA, with Slew Rate Control, with Test Pins	BT4CRP

SYMBOL



BEHAVIOUR

EN	A	TM	TEN	TA	Z
-	-	1	0	1	1
1	-	0	-	-	Z
0	1	0	-	-	1
-	-	1	1	-	Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
Z	3.633 pF

OUTPUT Pin	Max. load
Z	100.000 pF

CMOS035 MTC45200	CMOS Tristate Output Pad Buffer, 4mA, with Slew Rate Control, with Test Pins	BT4CRP

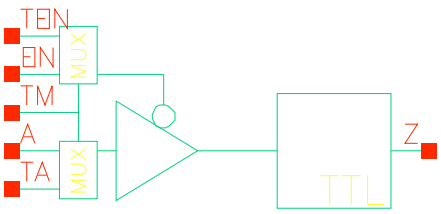
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to Z	0Z delay	1.06	1.11	1.27
EN to Z	1Z delay	1.31	1.36	1.51
TEN to Z	0Z delay	1.31	1.35	1.56
TEN to Z	1Z delay	1.54	1.58	1.77
TM to Z	0Z delay	1.72	1.78	2.00
TM to Z	1Z delay	1.94	2.01	2.22

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to Z	Fall delay	3.47	4.37	5.17	5.93
A to Z	Rise delay	3.42	4.41	5.31	6.18
EN to Z	Z0 delay	3.44	4.35	5.14	5.90
EN to Z	Z1 delay	3.37	4.36	5.27	6.14
TA to Z	Fall delay	3.80	4.70	5.50	6.26
TA to Z	Rise delay	3.69	4.68	5.58	6.46
TEN to Z	Z0 delay	3.76	4.66	5.46	6.22
TEN to Z	Z1 delay	3.68	4.67	5.58	6.45
TM to Z	Fall delay	3.98	4.88	5.68	6.44
TM to Z	Fall delay	3.81	4.71	5.51	6.27
TM to Z	Rise delay	4.12	5.11	6.02	6.89
TM to Z	Rise delay	3.58	4.57	5.48	6.35
TM to Z	Z0 delay	4.03	4.93	5.73	6.49
TM to Z	Z0 delay	3.79	4.70	5.50	6.26
TM to Z	Z1 delay	4.07	5.06	5.97	6.84
TM to Z	Z1 delay	3.70	4.69	5.60	6.47

CMOS035 MTC45200	TTL Five Volt tolerant Tristate Output Pad Buffer, 4mA, with Test Pins	BT4P_FT

SYMBOL



BEHAVIOUR

EN	A	TM	TEN	TA	Z
-	-	1	0	1	1
1	-	0	-	-	Z
0	1	0	-	-	1
-	-	1	1	-	Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
Z	3.819 pF

OUTPUT Pin	Max. load
Z	100.000 pF

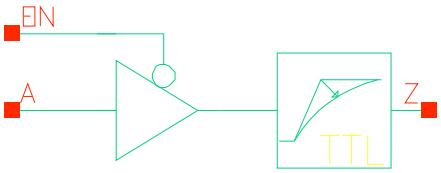
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to Z	0Z delay	1.09	1.14	1.32
EN to Z	1Z delay	1.41	1.47	1.64
TEN to Z	0Z delay	1.40	1.44	1.65
TEN to Z	1Z delay	1.68	1.72	1.93
TM to Z	0Z delay	1.80	1.87	2.08
TM to Z	1Z delay	2.09	2.15	2.36

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to Z	Fall delay	2.61	3.49	4.32	5.14
A to Z	Rise delay	2.30	3.05	3.76	4.48
EN to Z	Z0 delay	3.45	4.99	6.50	7.99
EN to Z	Z1 delay	2.29	3.04	3.75	4.47
TA to Z	Fall delay	2.94	3.82	4.66	5.47
TA to Z	Rise delay	2.57	3.32	4.04	4.75
TEN to Z	Z0 delay	3.83	5.37	6.87	8.37
TEN to Z	Z1 delay	2.66	3.41	4.12	4.84
TM to Z	Fall delay	3.12	4.00	4.83	5.65
TM to Z	Fall delay	2.95	3.82	4.66	5.48
TM to Z	Rise delay	3.00	3.75	4.47	5.18
TM to Z	Rise delay	2.46	3.21	3.93	4.64
TM to Z	Z0 delay	3.23	4.11	4.94	5.76
TM to Z	Z0 delay	2.95	3.83	4.66	5.48
TM to Z	Z1 delay	2.95	3.70	4.42	5.13
TM to Z	Z1 delay	2.62	3.37	4.09	4.80

CMOS035 MTC45200	TTL Five Volt tolerant Tristate Output Pad Buffer, 4mA, with Slew Rate Control	BT4R_FT

SYMBOL



BEHAVIOUR

EN	A	Z
1	-	Z
0	1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
Z	3.819 pF

OUTPUT Pin	Max. load
Z	100.000 pF

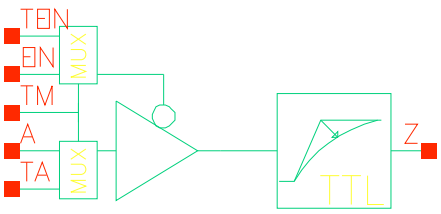
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to Z	0Z delay	1.09	1.14	1.32
EN to Z	1Z delay	1.42	1.47	1.64

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to Z	Fall delay	3.65	4.67	5.58	6.45
A to Z	Rise delay	3.23	4.10	4.88	5.62
EN to Z	Z0 delay	4.66	6.32	7.89	9.42
EN to Z	Z1 delay	3.22	4.10	4.87	5.62

CMOS035 MTC45200	TTL Five Volt tolerant Tristate Output Pad Buffer, 4mA, with Slew Rate Control, with Test Pins	BT4RP_FT

SYMBOL



BEHAVIOUR

EN	A	TM	TEN	TA	Z
-	-	1	0	1	1
1	-	0	-	-	Z
0	1	0	-	-	1
-	-	1	1	-	Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
Z	3.819 pF

OUTPUT Pin	Max. load
Z	100.000 pF

CMOS035 MTC45200	TTL Five Volt tolerant Tristate Output Pad Buffer, 4mA, with Slew Rate Control, with Test Pins	BT4RP_FT

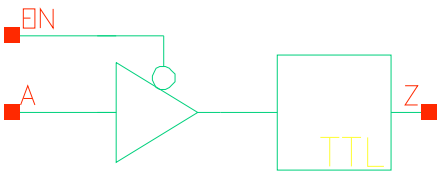
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to Z	0Z delay	1.09	1.14	1.32
EN to Z	1Z delay	1.42	1.47	1.64
TEN to Z	0Z delay	1.40	1.44	1.65
TEN to Z	1Z delay	1.68	1.72	1.93
TM to Z	0Z delay	1.80	1.87	2.08
TM to Z	1Z delay	2.09	2.15	2.36

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to Z	Fall delay	3.65	4.67	5.58	6.45
A to Z	Rise delay	3.23	4.10	4.88	5.62
EN to Z	Z0 delay	4.66	6.32	7.89	9.42
EN to Z	Z1 delay	3.22	4.10	4.87	5.62
TA to Z	Fall delay	3.98	5.00	5.91	6.78
TA to Z	Rise delay	3.50	4.38	5.15	5.90
TEN to Z	Z0 delay	5.03	6.70	8.27	9.79
TEN to Z	Z1 delay	3.59	4.46	5.24	5.98
TM to Z	Fall delay	4.16	5.17	6.09	6.96
TM to Z	Fall delay	3.99	5.00	5.92	6.79
TM to Z	Rise delay	3.94	4.81	5.59	6.33
TM to Z	Rise delay	3.40	4.27	5.05	5.79
TM to Z	Z0 delay	4.29	5.30	6.21	7.09
TM to Z	Z0 delay	4.01	5.02	5.94	6.81
TM to Z	Z1 delay	3.89	4.76	5.54	6.28
TM to Z	Z1 delay	3.55	4.43	5.21	5.95

CMOS035 MTC45200	TTL Five Volt tolerant Tristate Output Pad Buffer, 6mA	BT6_FT

SYMBOL



BEHAVIOUR

EN	A	Z
1	-	Z
0	1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
Z	4.640 pF

OUTPUT Pin	Max. load
Z	150.000 pF

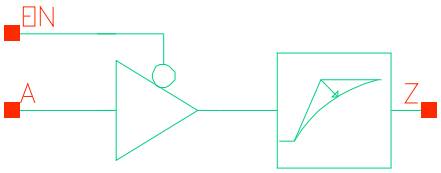
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to Z	0Z delay	1.06	1.12	1.30
EN to Z	1Z delay	1.38	1.43	1.60

Timing/Load		37.50pF	75.00pF	112.50pF	150.00pF
A to Z	Fall delay	2.53	3.41	4.25	5.06
A to Z	Rise delay	2.25	3.00	3.72	4.43
EN to Z	Z0 delay	3.36	4.90	6.40	7.90
EN to Z	Z1 delay	2.24	2.99	3.71	4.42

CMOS035 MTC45200	CMOS Tristate Output Pad Buffer, 6mA, with Slew Rate Control	BT6CR

SYMBOL



BEHAVIOUR

EN	A	Z
1	-	Z
0	1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
Z	4.453 pF

OUTPUT Pin	Max. load
Z	150.000 pF

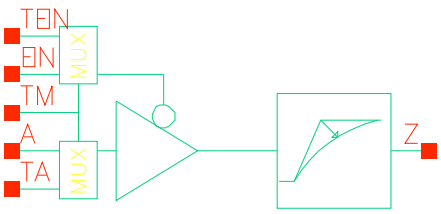
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to Z	0Z delay	1.04	1.09	1.25
EN to Z	1Z delay	1.28	1.33	1.48

Timing/Load		37.50pF	75.00pF	112.50pF	150.00pF
A to Z	Fall delay	3.36	4.25	5.05	5.80
A to Z	Rise delay	3.35	4.34	5.24	6.11
EN to Z	Z0 delay	3.34	4.23	5.02	5.78
EN to Z	Z1 delay	3.31	4.29	5.19	6.06

CMOS035 MTC45200	CMOS Tristate Output Pad Buffer, 6mA, with Slew Rate Control, with Test Pins	BT6CRP

SYMBOL



BEHAVIOUR

EN	A	TM	TEN	TA	Z
-	-	1	0	1	1
1	-	0	-	-	Z
0	1	0	-	-	1
-	-	1	1	-	Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
Z	4.453 pF

OUTPUT Pin	Max. load
Z	150.000 pF

CMOS035 MTC45200	CMOS Tristate Output Pad Buffer, 6mA, with Slew Rate Control, with Test Pins	BT6CRP

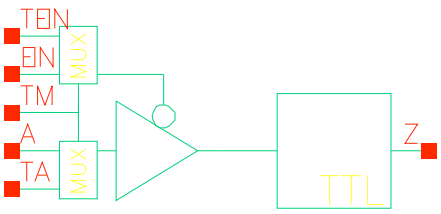
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to Z	0Z delay	1.04	1.09	1.25
EN to Z	1Z delay	1.28	1.33	1.48
TEN to Z	0Z delay	1.29	1.33	1.54
TEN to Z	1Z delay	1.50	1.54	1.74
TM to Z	0Z delay	1.70	1.76	1.98
TM to Z	1Z delay	1.91	1.97	2.19

Timing/Load		37.50pF	75.00pF	112.50pF	150.00pF
A to Z	Fall delay	3.36	4.25	5.05	5.80
A to Z	Rise delay	3.35	4.34	5.24	6.11
EN to Z	Z0 delay	3.34	4.23	5.02	5.78
EN to Z	Z1 delay	3.31	4.29	5.19	6.06
TA to Z	Fall delay	3.69	4.59	5.38	6.14
TA to Z	Rise delay	3.63	4.61	5.51	6.38
TEN to Z	Z0 delay	3.65	4.54	5.34	6.09
TEN to Z	Z1 delay	3.62	4.60	5.50	6.37
TM to Z	Fall delay	3.87	4.76	5.56	6.31
TM to Z	Fall delay	3.70	4.59	5.39	6.15
TM to Z	Rise delay	4.06	5.04	5.94	6.81
TM to Z	Rise delay	3.52	4.50	5.40	6.27
TM to Z	Z0 delay	3.92	4.81	5.61	6.37
TM to Z	Z0 delay	3.69	4.58	5.38	6.14
TM to Z	Z1 delay	4.01	4.99	5.89	6.76
TM to Z	Z1 delay	3.64	4.62	5.52	6.39

CMOS035 MTC45200	TTL Five Volt tolerant Tristate Output Pad Buffer, 6mA, with Test Pins	BT6P_FT

SYMBOL



BEHAVIOUR

EN	A	TM	TEN	TA	Z
-	-	1	0	1	1
1	-	0	-	-	Z
0	1	0	-	-	1
-	-	1	1	-	Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
Z	4.640 pF

OUTPUT Pin	Max. load
Z	150.000 pF

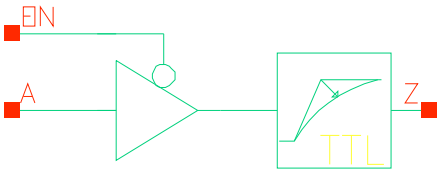
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to Z	0Z delay	1.06	1.12	1.30
EN to Z	1Z delay	1.38	1.43	1.60
TEN to Z	0Z delay	1.38	1.42	1.63
TEN to Z	1Z delay	1.64	1.68	1.89
TM to Z	0Z delay	1.78	1.85	2.06
TM to Z	1Z delay	2.05	2.12	2.32

Timing/Load		37.50pF	75.00pF	112.50pF	150.00pF
A to Z	Fall delay	2.53	3.41	4.25	5.06
A to Z	Rise delay	2.25	3.00	3.72	4.43
EN to Z	Z0 delay	3.36	4.90	6.40	7.90
EN to Z	Z1 delay	2.24	2.99	3.71	4.42
TA to Z	Fall delay	2.87	3.75	4.58	5.40
TA to Z	Rise delay	2.53	3.28	3.99	4.71
TEN to Z	Z0 delay	3.74	5.28	6.78	8.27
TEN to Z	Z1 delay	2.61	3.36	4.08	4.79
TM to Z	Fall delay	3.04	3.92	4.75	5.57
TM to Z	Fall delay	2.87	3.75	4.58	5.40
TM to Z	Rise delay	2.96	3.71	4.43	5.14
TM to Z	Rise delay	2.42	3.17	3.89	4.60
TM to Z	Z0 delay	3.16	4.03	4.87	5.68
TM to Z	Z0 delay	2.87	3.75	4.59	5.40
TM to Z	Z1 delay	2.91	3.66	4.38	5.09
TM to Z	Z1 delay	2.58	3.32	4.04	4.75

CMOS035 MTC45200	TTL Five Volt tolerant Tristate Output Pad Buffer, 6mA, with Slew Rate Control	BT6R_FT

SYMBOL



BEHAVIOUR

EN	A	Z
1	-	Z
0	1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
Z	4.639 pF

OUTPUT Pin	Max. load
Z	150.000 pF

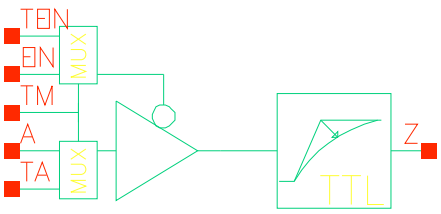
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to Z	0Z delay	1.06	1.12	1.30
EN to Z	1Z delay	1.37	1.43	1.60

Timing/Load		37.50pF	75.00pF	112.50pF	150.00pF
A to Z	Fall delay	3.53	4.54	5.45	6.32
A to Z	Rise delay	3.17	4.04	4.81	5.55
EN to Z	Z0 delay	4.51	6.17	7.74	9.27
EN to Z	Z1 delay	3.17	4.03	4.81	5.55

CMOS035 MTC45200	TTL Five Volt tolerant Tristate Output Pad Buffer, 6mA, with Slew Rate Control, with Test Pins	BT6RP_FT

SYMBOL



BEHAVIOUR

EN	A	TM	TEN	TA	Z
-	-	1	0	1	1
1	-	0	-	-	Z
0	1	0	-	-	1
-	-	1	1	-	Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
Z	4.639 pF

OUTPUT Pin	Max. load
Z	150.000 pF

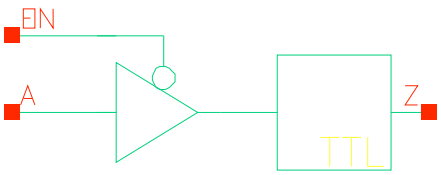
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to Z	0Z delay	1.07	1.12	1.30
EN to Z	1Z delay	1.37	1.43	1.60
TEN to Z	0Z delay	1.38	1.41	1.62
TEN to Z	1Z delay	1.64	1.68	1.89
TM to Z	0Z delay	1.78	1.84	2.06
TM to Z	1Z delay	2.05	2.12	2.32

Timing/Load		37.50pF	75.00pF	112.50pF	150.00pF
A to Z	Fall delay	3.53	4.54	5.45	6.32
A to Z	Rise delay	3.17	4.04	4.81	5.55
EN to Z	Z0 delay	4.51	6.17	7.74	9.27
EN to Z	Z1 delay	3.17	4.03	4.81	5.55
TA to Z	Fall delay	3.87	4.88	5.78	6.65
TA to Z	Rise delay	3.44	4.31	5.09	5.83
TEN to Z	Z0 delay	4.89	6.55	8.12	9.64
TEN to Z	Z1 delay	3.53	4.40	5.17	5.91
TM to Z	Fall delay	4.04	5.05	5.96	6.83
TM to Z	Fall delay	3.87	4.88	5.79	6.66
TM to Z	Rise delay	3.88	4.74	5.52	6.26
TM to Z	Rise delay	3.34	4.21	4.98	5.72
TM to Z	Z0 delay	4.17	5.18	6.09	6.96
TM to Z	Z0 delay	3.89	4.90	5.81	6.68
TM to Z	Z1 delay	3.83	4.70	5.47	6.21
TM to Z	Z1 delay	3.50	4.37	5.14	5.88

CMOS035 MTC45200	TTL Five Volt tolerant Tristate Output Pad Buffer, 8mA	BT8_FT

SYMBOL



BEHAVIOUR

EN	A	Z
1	-	Z
0	1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
Z	5.430 pF

OUTPUT Pin	Max. load
Z	200.000 pF

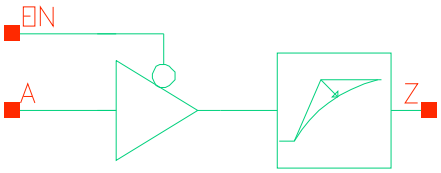
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to Z	0Z delay	1.04	1.10	1.28
EN to Z	1Z delay	1.34	1.39	1.56

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to Z	Fall delay	2.47	3.35	4.18	5.00
A to Z	Rise delay	2.22	2.97	3.69	4.40
EN to Z	Z0 delay	3.28	4.82	6.33	7.82
EN to Z	Z1 delay	2.21	2.96	3.68	4.39

CMOS035 MTC45200	CMOS Tristate Output Pad Buffer, 8mA, with Slew Rate Control	BT8CR

SYMBOL



BEHAVIOUR

EN	A	Z
1	-	Z
0	1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
Z	5.272 pF

OUTPUT Pin	Max. load
Z	200.000 pF

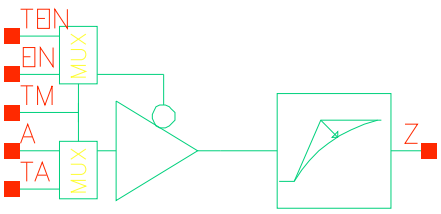
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to Z	0Z delay	1.01	1.06	1.22
EN to Z	1Z delay	1.25	1.30	1.44

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to Z	Fall delay	3.26	4.14	4.93	5.69
A to Z	Rise delay	3.30	4.28	5.17	6.04
EN to Z	Z0 delay	3.24	4.12	4.91	5.66
EN to Z	Z1 delay	3.26	4.24	5.13	6.00

CMOS035 MTC45200	CMOS Tristate Output Pad Buffer, 8mA, with Slew Rate Control, with Test Pins	BT8CRP

SYMBOL



BEHAVIOUR

EN	A	TM	TEN	TA	Z
-	-	1	0	1	1
1	-	0	-	-	Z
0	1	0	-	-	1
-	-	1	1	-	Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.8 SL
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
Z	5.272 pF

OUTPUT Pin	Max. load
Z	200.000 pF

CMOS035 MTC45200	CMOS Tristate Output Pad Buffer, 8mA, with Slew Rate Control, with Test Pins	BT8CRP

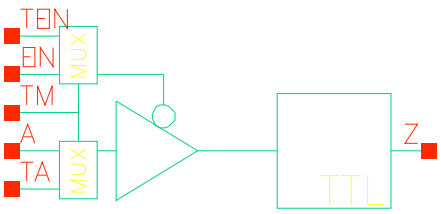
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to Z	0Z delay	1.01	1.06	1.22
EN to Z	1Z delay	1.25	1.30	1.44
TEN to Z	0Z delay	1.27	1.31	1.51
TEN to Z	1Z delay	1.47	1.51	1.70
TM to Z	0Z delay	1.68	1.74	1.96
TM to Z	1Z delay	1.88	1.94	2.15

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to Z	Fall delay	3.26	4.14	4.93	5.69
A to Z	Rise delay	3.30	4.28	5.17	6.04
EN to Z	Z0 delay	3.24	4.12	4.91	5.66
EN to Z	Z1 delay	3.26	4.24	5.13	6.00
TA to Z	Fall delay	3.60	4.48	5.27	6.02
TA to Z	Rise delay	3.57	4.55	5.45	6.32
TEN to Z	Z0 delay	3.55	4.43	5.22	5.98
TEN to Z	Z1 delay	3.57	4.55	5.44	6.31
TM to Z	Fall delay	3.77	4.65	5.44	6.20
TM to Z	Fall delay	3.60	4.48	5.28	6.03
TM to Z	Rise delay	4.01	4.98	5.88	6.75
TM to Z	Rise delay	3.47	4.45	5.34	6.21
TM to Z	Z0 delay	3.82	4.70	5.50	6.25
TM to Z	Z0 delay	3.59	4.47	5.27	6.02
TM to Z	Z1 delay	3.96	4.94	5.83	6.70
TM to Z	Z1 delay	3.59	4.57	5.46	6.33

CMOS035 MTC45200	TTL Five Volt tolerant Tristate Output Pad Buffer, 8mA, with Test Pins	BT8P_FT

SYMBOL



BEHAVIOUR

EN	A	TM	TEN	TA	Z
-	-	1	0	1	1
1	-	0	-	-	Z
0	1	0	-	-	1
-	-	1	1	-	Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
Z	5.430 pF

OUTPUT Pin	Max. load
Z	200.000 pF

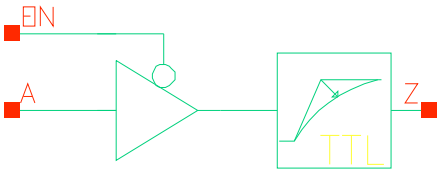
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to Z	0Z delay	1.04	1.10	1.28
EN to Z	1Z delay	1.34	1.39	1.56
TEN to Z	0Z delay	1.36	1.39	1.61
TEN to Z	1Z delay	1.61	1.65	1.85
TM to Z	0Z delay	1.76	1.82	2.04
TM to Z	1Z delay	2.01	2.08	2.29

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to Z	Fall delay	2.47	3.35	4.18	5.00
A to Z	Rise delay	2.22	2.97	3.69	4.40
EN to Z	Z0 delay	3.28	4.82	6.33	7.82
EN to Z	Z1 delay	2.21	2.96	3.68	4.39
TA to Z	Fall delay	2.81	3.68	4.51	5.33
TA to Z	Rise delay	2.50	3.24	3.96	4.67
TEN to Z	Z0 delay	3.66	5.20	6.70	8.20
TEN to Z	Z1 delay	2.58	3.33	4.05	4.76
TM to Z	Fall delay	2.98	3.86	4.69	5.51
TM to Z	Fall delay	2.81	3.68	4.52	5.33
TM to Z	Rise delay	2.93	3.67	4.39	5.10
TM to Z	Rise delay	2.39	3.13	3.85	4.56
TM to Z	Z0 delay	3.09	3.97	4.80	5.62
TM to Z	Z0 delay	2.81	3.69	4.52	5.34
TM to Z	Z1 delay	2.88	3.63	4.34	5.05
TM to Z	Z1 delay	2.54	3.29	4.01	4.72

CMOS035 MTC45200	TTL Five Volt tolerant Tristate Output Pad Buffer, 8mA, with Slew Rate Control	BT8R_FT

SYMBOL



BEHAVIOUR

EN	A	Z
1	-	Z
0	1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
Z	5.430 pF

OUTPUT Pin	Max. load
Z	200.000 pF

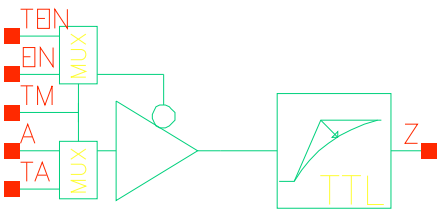
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to Z	0Z delay	1.04	1.10	1.28
EN to Z	1Z delay	1.34	1.39	1.56

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to Z	Fall delay	3.43	4.43	5.33	6.20
A to Z	Rise delay	3.12	3.98	4.75	5.49
EN to Z	Z0 delay	4.39	6.04	7.61	9.13
EN to Z	Z1 delay	3.12	3.98	4.75	5.49

CMOS035 MTC45200	TTL Five Volt tolerant Tristate Output Pad Buffer, 8mA, with Slew Rate Control, with Test Pins	BT8RP_FT

SYMBOL



BEHAVIOUR

EN	A	TM	TEN	TA	Z
-	-	1	0	1	1
1	-	0	-	-	Z
0	1	0	-	-	1
-	-	1	1	-	Z

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL
EN	3.7 SL
TA	1.7 SL
TEN	1.7 SL
TM	1.4 SL
Z	5.430 pF

OUTPUT Pin	Max. load
Z	200.000 pF

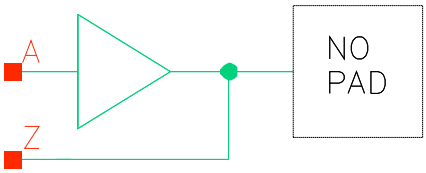
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to Z	0Z delay	1.04	1.10	1.28
EN to Z	1Z delay	1.34	1.39	1.56
TEN to Z	0Z delay	1.35	1.39	1.60
TEN to Z	1Z delay	1.61	1.65	1.85
TM to Z	0Z delay	1.76	1.82	2.04
TM to Z	1Z delay	2.01	2.08	2.29

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to Z	Fall delay	3.43	4.43	5.33	6.20
A to Z	Rise delay	3.12	3.98	4.75	5.49
EN to Z	Z0 delay	4.39	6.04	7.61	9.13
EN to Z	Z1 delay	3.12	3.98	4.75	5.49
TA to Z	Fall delay	3.77	4.76	5.67	6.53
TA to Z	Rise delay	3.40	4.26	5.03	5.76
TEN to Z	Z0 delay	4.77	6.42	7.98	9.51
TEN to Z	Z1 delay	3.49	4.35	5.12	5.85
TM to Z	Fall delay	3.94	4.94	5.84	6.71
TM to Z	Fall delay	3.77	4.77	5.67	6.54
TM to Z	Rise delay	3.83	4.69	5.46	6.20
TM to Z	Rise delay	3.29	4.15	4.92	5.66
TM to Z	Z0 delay	4.07	5.07	5.97	6.84
TM to Z	Z0 delay	3.79	4.79	5.69	6.56
TM to Z	Z1 delay	3.78	4.65	5.42	6.15
TM to Z	Z1 delay	3.45	4.31	5.08	5.82

CMOS035 MTC45200	Peripheral Buffer, 4mA	BUF4

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL

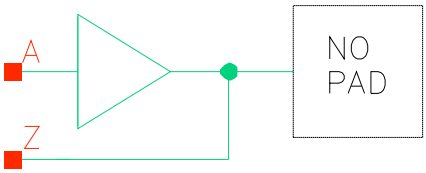
OUTPUT Pin	Max. load
Z	100.000 pF

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF
A to Z	Fall delay	2.40	3.17	3.89	4.60
A to Z	Rise delay	2.39	3.26	4.12	4.96

CMOS035 MTC45200	Peripheral Buffer, 8mA	BUF8

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	3.7 SL

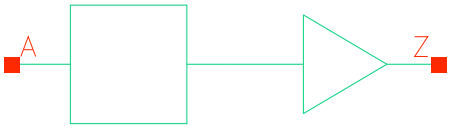
OUTPUT Pin	Max. load
Z	200.000 pF

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF
A to Z	Fall delay	2.28	3.04	3.76	4.46
A to Z	Rise delay	2.31	3.18	4.03	4.88

CMOS035 MTC45200	CMOS Input Pad Buffer	IBUF

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	2.122 pF

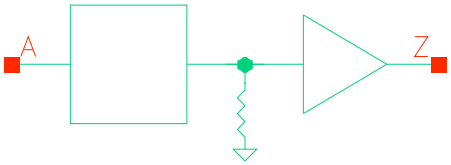
OUTPUT Pin	Max. load
Z	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
A to Z	Fall delay	0.19	0.26	0.33	0.47
A to Z	Rise delay	0.19	0.28	0.37	0.54

CMOS035 MTC45200	CMOS Input Pad Buffer with Active Pull-Down	IBUFD

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	2.131 pF

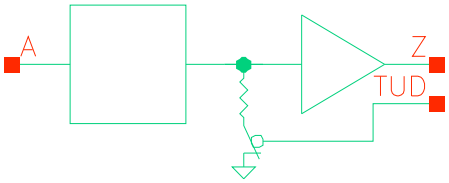
OUTPUT Pin	Max. load
Z	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
A to Z	Fall delay	0.19	0.26	0.34	0.47
A to Z	Rise delay	0.20	0.29	0.38	0.55

CMOS035 MTC45200	CMOS Input Pad Buffer with Active Pull-Down and Test Pin	IBUFDQ

SYMBOL



BEHAVIOUR

A	TUD	Z
1	-	1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	2.128 pF
TUD	1.9 SL

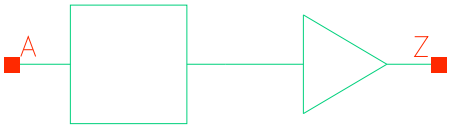
OUTPUT Pin	Max. load
Z	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
A to Z	Fall delay	0.19	0.27	0.34	0.48
A to Z	Rise delay	0.20	0.29	0.38	0.55

CMOS035 MTC45200	CMOS Input Pad Buffer	IBUFH

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	2.121 pF

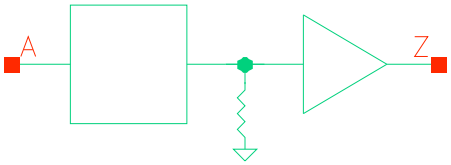
OUTPUT Pin	Max. load
Z	322 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	80.0xSL	160.0xSL	320.0xSL
A to Z	Fall delay	0.27	0.39	0.48	0.67
A to Z	Rise delay	0.27	0.38	0.47	0.64

CMOS035 MTC45200	CMOS Input Pad Buffer with Active Pull-Down	IBUFHD

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	2.129 pF

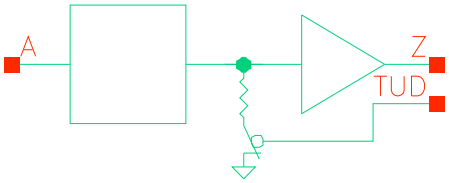
OUTPUT Pin	Max. load
Z	322 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	80.0xSL	160.0xSL	320.0xSL
A to Z	Fall delay	0.27	0.39	0.48	0.67
A to Z	Rise delay	0.28	0.39	0.48	0.65

CMOS035 MTC45200	CMOS Input Pad Buffer with Active Pull-Down and Test Pin	IBUFHDQ

SYMBOL



BEHAVIOUR

A	TUD	Z
1	-	1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	2.127 pF
TUD	1.9 SL

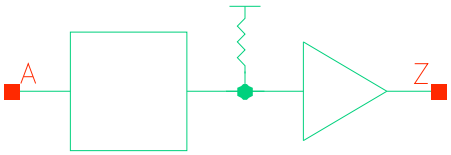
OUTPUT Pin	Max. load
Z	322 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	80.0xSL	160.0xSL	320.0xSL
A to Z	Fall delay	0.27	0.39	0.48	0.67
A to Z	Rise delay	0.28	0.39	0.48	0.65

CMOS035 MTC45200	CMOS Input Pad Buffer with Active Pull-Up	IBUFHU

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	2.132 pF

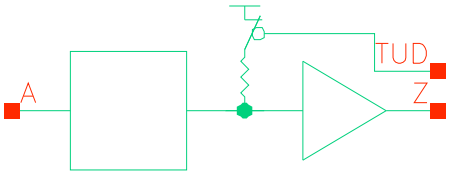
OUTPUT Pin	Max. load
Z	322 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	80.0xSL	160.0xSL	320.0xSL
A to Z	Fall delay	0.28	0.40	0.49	0.68
A to Z	Rise delay	0.27	0.38	0.47	0.64

CMOS035 MTC45200	CMOS Input Pad Buffer with Active Pull-Up and Test Pin	IBUFHUQ

SYMBOL



BEHAVIOUR

A	TUD	Z
1	-	1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	2.128 pF
TUD	2.3 SL

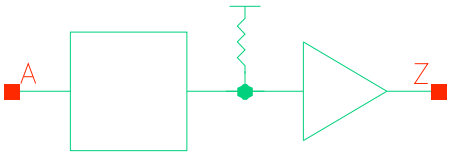
OUTPUT Pin	Max. load
Z	322 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	80.0xSL	160.0xSL	320.0xSL
A to Z	Fall delay	0.28	0.40	0.49	0.68
A to Z	Rise delay	0.28	0.38	0.47	0.64

CMOS035 MTC45200	CMOS Input Pad Buffer with Active Pull-Up	IBUFU

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	2.133 pF

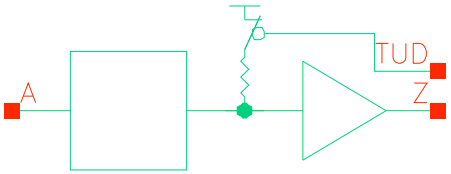
OUTPUT Pin	Max. load
Z	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
A to Z	Fall delay	0.20	0.27	0.34	0.48
A to Z	Rise delay	0.20	0.28	0.37	0.54

CMOS035 MTC45200	CMOS Input Pad Buffer with Active Pull-Up and Test Pin	IBUFUQ

SYMBOL



BEHAVIOUR

A	TUD	Z
1	-	1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	2.129 pF
TUD	2.3 SL

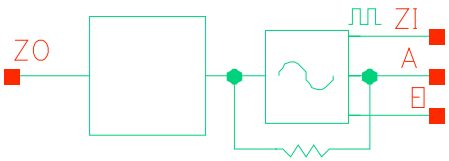
OUTPUT Pin	Max. load
Z	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
A to Z	Fall delay	0.20	0.27	0.34	0.48
A to Z	Rise delay	0.20	0.28	0.37	0.54

CMOS035 MTC45200	Oscillator 13 Mhz	OSCI13B

SYMBOL



BEHAVIOUR

A	E	ZI	ZO
1	1	0	
0	1		1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	10.7 SL
E	8.4 SL

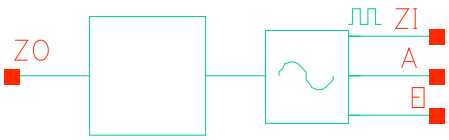
OUTPUT Pin	Max. load
ZI	39 SL
ZO	0.352 pF

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
A to ZI	Fall delay	1.71	1.84	1.98	2.24
A to ZI	Rise delay	11.28	12.06	12.87	14.48
A to ZO	Fall delay	0.82	0.87	0.93	1.04
A to ZO	Rise delay	8.94	9.56	10.21	11.51
E to ZI	Fall delay	0.25	0.30	0.34	0.43
E to ZI	Rise delay	0.23	0.27	0.31	0.38
E to ZO	Fall delay	1.04	1.10	1.16	1.27
E to ZO	Rise delay	8.99	9.61	10.26	11.56

CMOS035 MTC45200	Oscillator 27 Mhz	OSCI27B

SYMBOL



BEHAVIOUR

A	E	ZI	ZO
0	1	0	
1	1		0

ABSTRACT

Cell Length	Cell Height	Cell Area
204.00 um	183.00 um	37332

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	98.7 SL
E	56.3 SL

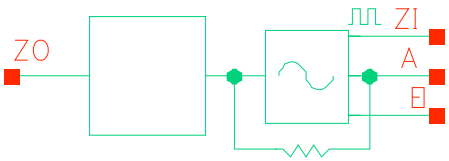
OUTPUT Pin	Max. load
ZI	39 SL
ZO	0.352 pF

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
A to ZI	Fall delay	0.59	0.61	0.62	0.65
A to ZI	Rise delay	0.46	0.48	0.49	0.52
A to ZO	Fall delay	0.32	0.33	0.34	0.36
A to ZO	Rise delay	0.39	0.41	0.42	0.45
E to ZI	Fall delay	0.23	0.25	0.27	0.30
E to ZI	Rise delay	0.27	0.29	0.30	0.32
E to ZO	Fall delay	0.27	0.28	0.29	0.32
E to ZO	Rise delay	1.69	1.77	1.85	2.02

CMOS035 MTC45200	Oscillator 32 khz	OSCI32B

SYMBOL



BEHAVIOUR

A	E	ZI	ZO
1	1	0	
0	1		1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	7.4 SL
E	6.0 SL

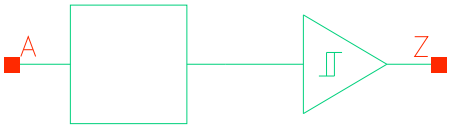
OUTPUT Pin	Max. load
ZI	39 SL
ZO	0.352 pF

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
A to ZI	Fall delay	3.80	4.05	4.29	4.78
A to ZI	Rise delay	36.23	38.81	41.52	46.90
A to ZO	Fall delay	1.24	1.33	1.42	1.61
A to ZO	Rise delay	21.47	23.01	24.62	27.85
E to ZI	Fall delay	0.27	0.32	0.36	0.44
E to ZI	Rise delay	0.27	0.32	0.36	0.43
E to ZO	Fall delay	1.39	1.48	1.58	1.77
E to ZO	Rise delay	21.48	23.02	24.64	27.87

CMOS035 MTC45200	CMOS Schmitt Trigger Input Pad Buffer	SCHMITC

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	2.130 pF

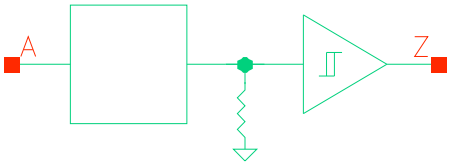
OUTPUT Pin	Max. load
Z	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
A to Z	Fall delay	0.45	0.55	0.63	0.78
A to Z	Rise delay	0.48	0.60	0.71	0.93

CMOS035 MTC45200	CMOS Schmitt Trigger Input Pad Buffer with Active Pull-Down	SCHMITCD

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	2.138 pF

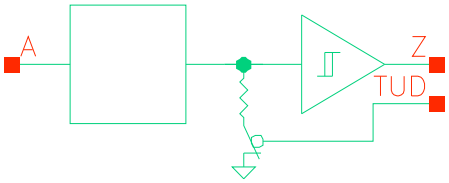
OUTPUT Pin	Max. load
Z	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
A to Z	Fall delay	0.45	0.56	0.64	0.79
A to Z	Rise delay	0.49	0.61	0.72	0.94

CMOS035 MTC45200	CMOS Schmitt Trigger Input Pad Buffer with Active Pull-Down and Test Pin	SCHMITCDQ

SYMBOL



BEHAVIOUR

A	TUD	Z
1	-	1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	2.135 pF
TUD	1.9 SL

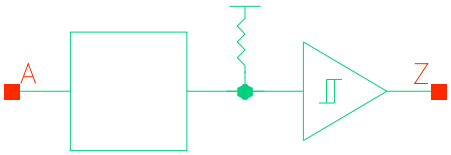
OUTPUT Pin	Max. load
Z	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
A to Z	Fall delay	0.45	0.56	0.64	0.79
A to Z	Rise delay	0.49	0.61	0.72	0.94

CMOS035 MTC45200	CMOS Schmitt Trigger Input Pad Buffer with Active Pull-Up	SCHMITCU

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	2.140 pF

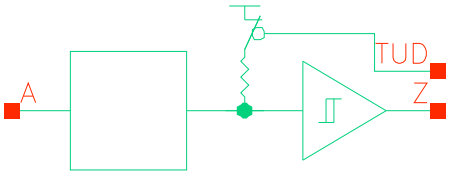
OUTPUT Pin	Max. load
Z	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
A to Z	Fall delay	0.46	0.56	0.65	0.79
A to Z	Rise delay	0.49	0.61	0.72	0.94

CMOS035 MTC45200	CMOS Schmitt Trigger Input Pad Buffer with Active Pull-Up and Test Pin	SCHMITCUQ

SYMBOL



BEHAVIOUR

A	TUD	Z
1	-	1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	2.136 pF
TUD	2.3 SL

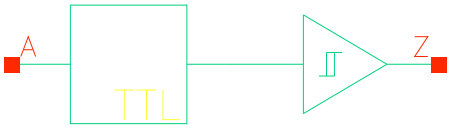
OUTPUT Pin	Max. load
Z	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
A to Z	Fall delay	0.46	0.56	0.65	0.79
A to Z	Rise delay	0.49	0.61	0.72	0.94

CMOS035 MTC45200	TTL Schmitt Trigger Input Pad Buffer	SCHMITT

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	2.152 pF

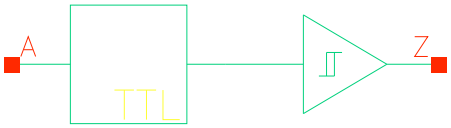
OUTPUT Pin	Max. load
Z	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
A to Z	Fall delay	0.42	0.52	0.61	0.75
A to Z	Rise delay	0.38	0.49	0.60	0.82

CMOS035 MTC45200	TTL Five Volt tolerant Schmitt Trigger Input Pad Buffer	SCHMITT_FT

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	2.146 pF

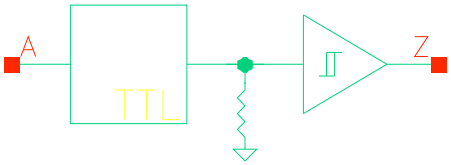
OUTPUT Pin	Max. load
Z	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
A to Z	Fall delay	0.56	0.67	0.77	0.93
A to Z	Rise delay	0.75	0.87	0.98	1.19

CMOS035 MTC45200	TTL Schmitt Trigger Input Pad Buffer with Active Pull-Down	SCHMITTD

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	2.160 pF

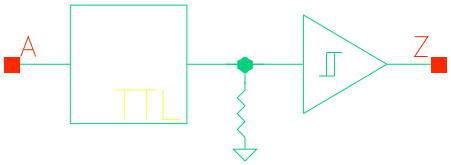
OUTPUT Pin	Max. load
Z	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
A to Z	Fall delay	0.43	0.53	0.61	0.76
A to Z	Rise delay	0.38	0.50	0.61	0.83

CMOS035 MTC45200	TTL Five Volt tolerant Schmitt Trigger Input Pad Buffer with Active Pull-Down	SCHMITTD_FT

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	2.144 pF

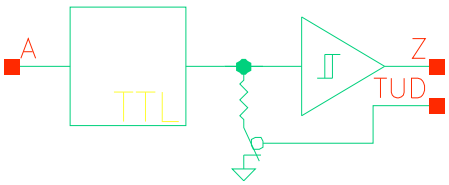
OUTPUT Pin	Max. load
Z	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
A to Z	Fall delay	0.54	0.66	0.75	0.91
A to Z	Rise delay	0.82	0.94	1.05	1.27

CMOS035 MTC45200	TTL Schmitt Trigger Input Pad Buffer with Active Pull-Down and Test Pin	SCHMITTDQ

SYMBOL



BEHAVIOUR

A	TUD	Z
1	-	1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	2.157 pF
TUD	1.9 SL

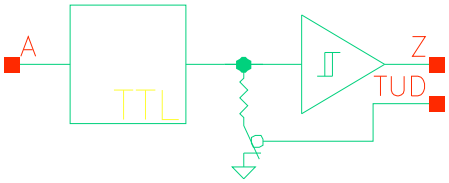
OUTPUT Pin	Max. load
Z	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
A to Z	Fall delay	0.43	0.53	0.61	0.76
A to Z	Rise delay	0.38	0.50	0.61	0.83

CMOS035 MTC45200	TTL Five Volt tolerant Schmitt Trigger Input Pad Buffer with Active Pull-Down and Test Pin	SCHMITTDQ_FT

SYMBOL



BEHAVIOUR

A	TUD	Z
1	-	1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	2.146 pF
TUD	1.9 SL

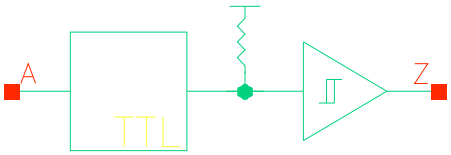
OUTPUT Pin	Max. load
Z	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
A to Z	Fall delay	0.56	0.67	0.77	0.93
A to Z	Rise delay	0.82	0.94	1.05	1.27

CMOS035 MTC45200	TTL Schmitt Trigger Input Pad Buffer with Active Pull-Up	SCHMITTU

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	2.162 pF

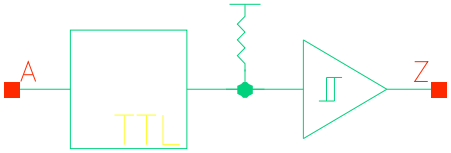
OUTPUT Pin	Max. load
Z	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
A to Z	Fall delay	0.44	0.54	0.62	0.76
A to Z	Rise delay	0.38	0.49	0.60	0.82

CMOS035 MTC45200	TTL Five Volt tolerant Schmitt Trigger Input Pad Buffer with Active Pull-Up	SCHMITTU_FT

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	2.151 pF

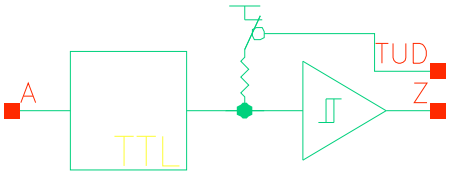
OUTPUT Pin	Max. load
Z	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
A to Z	Fall delay	0.59	0.71	0.80	0.96
A to Z	Rise delay	0.71	0.83	0.94	1.16

CMOS035 MTC45200	TTL Schmitt Trigger Input Pad Buffer with Active Pull-Up and Test Pin	SCHMITTUQ

SYMBOL



BEHAVIOUR

A	TUD	Z
1	-	1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	2.158 pF
TUD	2.3 SL

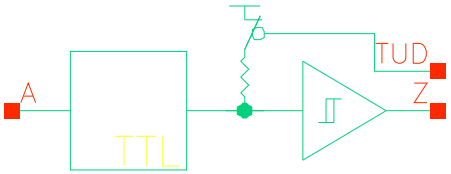
OUTPUT Pin	Max. load
Z	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
A to Z	Fall delay	0.44	0.54	0.62	0.76
A to Z	Rise delay	0.38	0.49	0.60	0.82

CMOS035 MTC45200	TTL Five Volt tolerant Schmitt Trigger Input Pad Buffer with Active Pull-Up and Test Pin	SCHMITTUQ_FT

SYMBOL



BEHAVIOUR

A	TUD	Z
1	-	1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	2.147 pF
TUD	2.3 SL

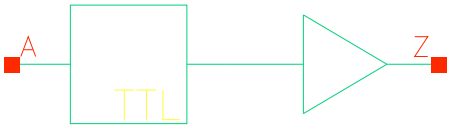
OUTPUT Pin	Max. load
Z	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
A to Z	Fall delay	0.59	0.71	0.80	0.96
A to Z	Rise delay	0.75	0.87	0.98	1.19

CMOS035 MTC45200	TTL Input Pad Buffer	TLCHT

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	2.161 pF

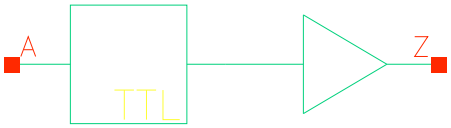
OUTPUT Pin	Max. load
Z	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
A to Z	Fall delay	0.24	0.33	0.41	0.55
A to Z	Rise delay	0.24	0.33	0.41	0.58

CMOS035 MTC45200	TTL Five Volt tolerant Input Pad Buffer	TLCHT_FT

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	2.151 pF

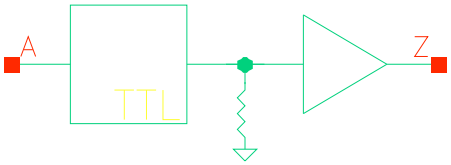
OUTPUT Pin	Max. load
Z	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
A to Z	Fall delay	0.28	0.37	0.45	0.59
A to Z	Rise delay	0.31	0.40	0.49	0.66

CMOS035 MTC45200	TTL Input Pad Buffer with Active Pull-Down	TLCHTD

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	2.169 pF

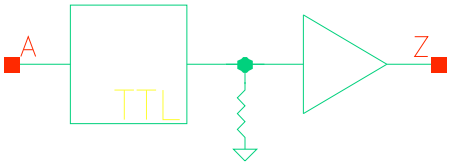
OUTPUT Pin	Max. load
Z	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
A to Z	Fall delay	0.24	0.33	0.41	0.55
A to Z	Rise delay	0.25	0.34	0.42	0.59

CMOS035 MTC45200	TTL Five Volt tolerant Input Pad Buffer with Active Pull-Down	TLCHTD_FT

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	2.149 pF

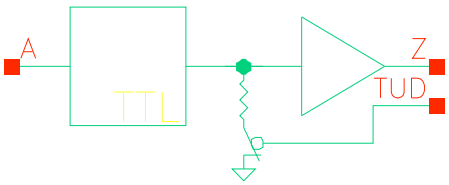
OUTPUT Pin	Max. load
Z	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
A to Z	Fall delay	0.27	0.36	0.44	0.58
A to Z	Rise delay	0.33	0.42	0.50	0.67

CMOS035 MTC45200	TTL Input Pad Buffer with Active Pull-Down and Test Pin	TLCHTDQ

SYMBOL



BEHAVIOUR

A	TUD	Z
1	-	1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	2.166 pF
TUD	1.9 SL

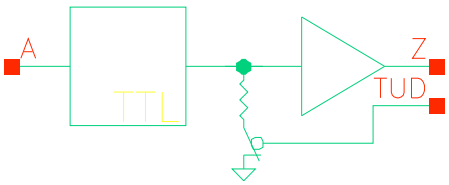
OUTPUT Pin	Max. load
Z	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
A to Z	Fall delay	0.24	0.33	0.41	0.55
A to Z	Rise delay	0.25	0.34	0.42	0.59

CMOS035 MTC45200	TTL Five Volt tolerant Input Pad Buffer with Active Pull-Down and Test Pin	TLCHTDQ_FT

SYMBOL



BEHAVIOUR

A	TUD	Z
1	-	1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	2.151 pF
TUD	1.9 SL

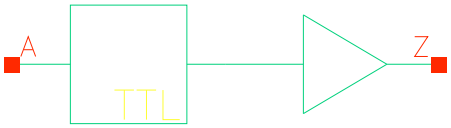
OUTPUT Pin	Max. load
Z	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
A to Z	Fall delay	0.28	0.37	0.45	0.59
A to Z	Rise delay	0.33	0.42	0.50	0.67

CMOS035 MTC45200	TTL Input Pad Buffer	TLCHTH_FT

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	2.148 pF

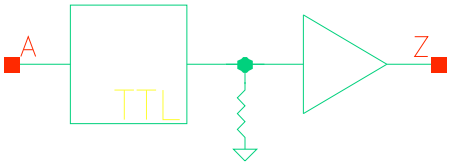
OUTPUT Pin	Max. load
Z	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
A to Z	Fall delay	0.43	0.48	0.51	0.58
A to Z	Rise delay	0.45	0.49	0.52	0.57

CMOS035 MTC45200	TTL Input Pad Buffer	TLCHTHD_FT

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	2.148 pF

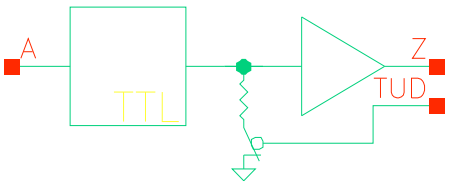
OUTPUT Pin	Max. load
Z	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
A to Z	Fall delay	0.43	0.47	0.51	0.57
A to Z	Rise delay	0.47	0.51	0.54	0.59

CMOS035 MTC45200	TTL Input Pad Buffer	TLCHTHDQ_FT

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	2.148 pF
TUD	2.3 SL

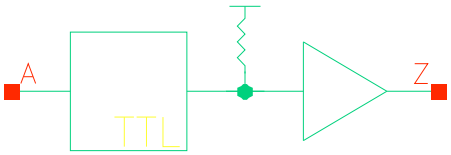
OUTPUT Pin	Max. load
Z	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
A to Z	Fall delay	0.43	0.47	0.51	0.57
A to Z	Rise delay	0.48	0.51	0.54	0.60

CMOS035 MTC45200	TTL Input Pad Buffer	TLCHTHU_FT

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	2.156 pF

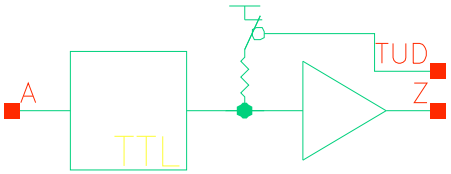
OUTPUT Pin	Max. load
Z	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
A to Z	Fall delay	0.46	0.51	0.54	0.60
A to Z	Rise delay	0.44	0.48	0.51	0.56

CMOS035 MTC45200	TTL Input Pad Buffer	TLCHTHUQ_FT

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	2.155 pF
TUD	2.3 SL

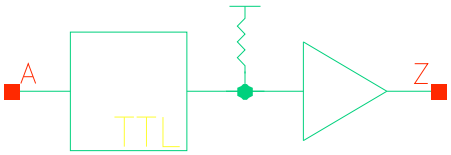
OUTPUT Pin	Max. load
Z	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
A to Z	Fall delay	0.46	0.51	0.54	0.61
A to Z	Rise delay	0.44	0.48	0.51	0.56

CMOS035 MTC45200	TTL Input Pad Buffer with Active Pull-Up	TLCHTU

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	2.171 pF

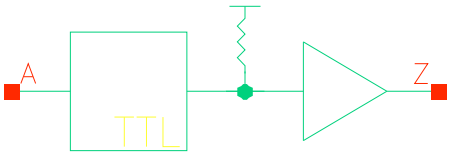
OUTPUT Pin	Max. load
Z	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
A to Z	Fall delay	0.25	0.34	0.42	0.56
A to Z	Rise delay	0.24	0.33	0.41	0.58

CMOS035 MTC45200	TTL Five Volt tolerant Input Pad Buffer with Active Pull-Up	TLCHTU_FT

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	2.156 pF

OUTPUT Pin	Max. load
Z	81 SL

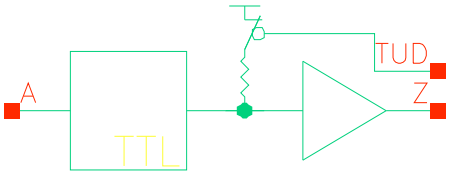
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
A to Z	Fall delay	0.30	0.39	0.47	0.61

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
A to Z	Rise delay	0.31	0.40	0.48	0.65

CMOS035 MTC45200	TTL Input Pad Buffer with Active Pull-Up and Test Pin	TLCHTUQ

SYMBOL



BEHAVIOUR

A	TUD	Z
1	-	1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	2.167 pF
TUD	2.3 SL

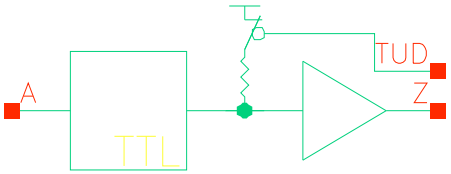
OUTPUT Pin	Max. load
Z	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
A to Z	Fall delay	0.25	0.34	0.42	0.56
A to Z	Rise delay	0.24	0.33	0.42	0.59

CMOS035 MTC45200	TTL Five Volt tolerant Input Pad Buffer with Active Pull-Up and Test Pin	TLCHTUQ_FT

SYMBOL



BEHAVIOUR

A	TUD	Z
1	-	1

ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	2.151 pF
TUD	2.3 SL

OUTPUT Pin	Max. load
Z	81 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
A to Z	Fall delay	0.30	0.39	0.47	0.61

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL
A to Z	Rise delay	0.31	0.40	0.49	0.66

CMOS035 MTC45200	Internal supply for core only power pad	VDD

SYMBOL

ABSTRACT

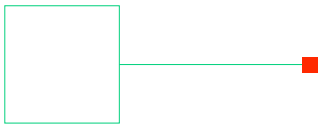
Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

OUTPUT Pin	Max. load
vdd!	39 SL

CMOS035 MTC45200	Internal supply for core only power pad	VDDCO

SYMBOL



ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

OUTPUT Pin	Max. load
VDDCORE	39 SL

CMOS035 MTC45200	Internal ground for core only power pad	VSS

SYMBOL

ABSTRACT

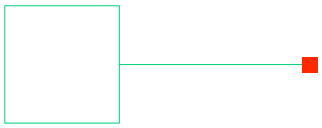
Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

OUTPUT Pin	Max. load
gnd!	39 SL

CMOS035 MTC45200	Internal ground for core only power pad	VSSCO

SYMBOL



ABSTRACT

Cell Length	Cell Height	Cell Area
144.00 um	183.00 um	26352

PIN DESCRIPTIONS

OUTPUT Pin	Max. load
VSSCORE	39 SL