Databook

1 Introduction

1.1 General 3.3V IOLIB specification

1.1.1 DC specifications

Table 1: Absolute Maximum Ratings

Vdd	3.3V Power Supply Voltage	-0.5V to 4V	
	Input or Output Voltage	-0.5V to (Vdd+ 0.5V)	
	Input or Output Voltage	-0.5V to 5.5V	Note 1

Note1: For 5V tolerant inputs and 5V tolerant output buffers in tri-state mode.

Table 2: Recommended DC Operating Conditions

Vdd	Power Supply Voltage	2.7 to 3.6V	Note 1
T_j	Operating Junction temperature	-40^{o}C to 125^{o}C	

All the following specifications are valid only within these recommended operating conditions.

Note1: For low voltage TTL circuits the switching levels are only guaranteed between 3.0V and 3.6V.

Table 3: General Interface Electrical Characteristics

	Parameter	Conditions	Min	Typ	Max	Unit	Note
Iil	Low Level Input Current Without pull-up device	Vi=0V			1	uA	1
Iih	High Level Input Current Without pull-down device	Vi=Vdd			1	uA	1
Ioz	Tri-state Output leakage Without pull up/down device	Vo=0V or Vdd			1	uA	1
Cin	Input capacitance		See data-sheets				
Cout	Output capacitance		See data-sheets				
Cio	I/O capacitance		See data-sheets				
I latchup	I/O Latch-up Current	V<0V, V>Vdd	200			mA	
Vesd	Electrostatic Protection	Leakage < 1uA	4000			V	2

Note1: The leakage currents are generally very small, < 1nA. The value given here, 1uA, is a maximum that can occur after an Electrostatic Stress on the pin.

Note2: Human Body Model.

Table 4: Low Voltage CMOS Interface DC Electrical Characteristics

	Parameter	Conditions	Min	Typ	Max	Unit	Note
Vil	Low level input voltage				0.2*Vdd	V	
Vih	High level input voltage		0.8*Vdd			V	
Vhyst	Schmitt trigger hysteresis		0.8			V	
Vol	Low level output Voltage	Iol=XmA			0.4	V	1, 2
Voh	High level output Voltage	Ioh=-XmA	0.85*Vdd			V	1, 2

Note1: Takes into account 200mV voltage drop in both supply lines.

Note2: X is the source/sink current under worst case conditions and is reflected in the name of the I/O cell according to the drive capability.

Table 5: Low Voltage TTL Interface DC Electrical Characteristics

	Parameter	Conditions	Min	Typ	Max	Unit	Note
Vil	Low level input voltage				0.8	V	1
Vih	High level input voltage		2.0			V	1
Vilhyst	Low level Threshold input falling		0.9		1.35		1
Vihhyst	High level threshold input rising		1.3		1.9		1
Vhyst	Schmitt trigger hysteresis		0.4		0.7	V	1
Vol	Low level output Voltage	Iol=XmA			0.4	V	1, 2,3
Voh	High level output Voltage	Ioh=-XmA	2.4			V	1, 2,3

Note1: TTL specifications only apply to the supply voltage range Vdd = 3.0V to 3.6V

Note2: Takes into account 200mV voltage drop in both supply lines.

Note3: X is the source/sink current under worst case conditions and is reflected in the name of the I/O cell according to the drive capability.

Table 6: Pullup & pulldown Characteristics

	Parameter	Conditions	Min	Typ	Max	Unit	Note
Ipu	Pullup current	Vi = 0V	-25	-66	-125	uA	1
Ipd	Pulldown current	Vi = Vdd	25	66	125	uA	1
Ipd	Pulldown current	Vi = 5V	25	66	125	uA	2
Rup	Equivalent pull-up resistance	Vi = 0V		50		KOhm	
Rpd	Equivalent pull-down resistance	Vi = Vdd		50		KOhm	
Rpd	Equivalent pull-down resistance	Vi = 5V		76		KOhm	2

Note1: Min condition: Vdd=2.7V, 125^{o}C, Min process
Max condition: Vdd-3.6V, -40^{o}C, Max process

Note2: For 5V tolerant buffers.

1.1.2 Naming convention

Inputs	
IBUF	CMOS input buffer.
TLCHT	TTL input buffer.
SCHMIT	Input buffer with hysteresis.
1st suffix	T for TTL levels
	C for CMOS levels
	Not present after IBUF & TLCHT.
2nd suffix	H for High drive input stage.
3rd suffix	U for active pull up
	D for active pull down.
4th suffix	Q for switch on pull-up/down.
5th suffix	_FT for 5V tolerant.

Outputs	
B	Push pull output buffer.
BT	Tri-state output buffer.
1st suffix	Drive capability in mA.
2nd suffix	C for CMOS (Absence of “C” = TTL).
3rd suffix	R for slew rate control.
4th suffix	OD for open drain.
5th suffix	U for pull up.
	D for active pull down.
6th suffix	Q for switch on pull-up/down.
7th suffix	_FT for 5V tolerant.

Bidirectional	
BD	Bidirectional buffer.
1st suffix	Drive capability in mA.
2nd suffix	H for High drive input stage.
3rd suffix	Z for Tri-state input stage.
4th suffix	S for Schmitt trigger on input.
5th suffix	T for TTL levels
	C for CMOS levels.
6th suffix	R for slew rate control.
7th suffix	OD for open drain output.
8th suffix	U for active pull up.
	D for active pull down.
9th suffix	Q for switch on pull-up/down.
10th suffix	_FT for 5V tolerant.

1.2 buffers description (Functionality)

1.2.1 Input stages

Input buffers are available with two possible drives towards the core chip:

- "Normal drive" is equivalent to an X4 drive in the standard digital library. These cells are characterised with internal loads up to 80 Standard Loads, i.e. 0.72pF.
- "High drive" is equivalent to an X16 drive in the standard digital library. They are characterized with loads up to 316 Standard Loads, i.e. 2.84pF.
  The suffix "H" is used in the cell name when high drive is present.
  Note: In this library release, the high drive option is only possible with CMOS input buffers.

Five volt Tolerant inputs:

- Five tolerant inputs are input buffers that can receive 5V signals while being supplied under 3.3V:

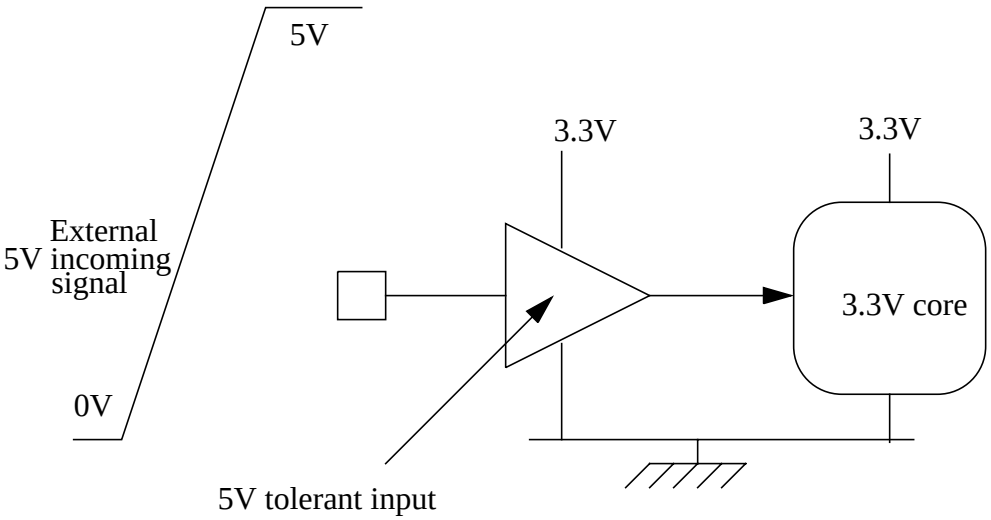

Figure 1: 5V tolerant input principle

- Only TTL buffers (with or without hysteresis) are available with the five volt tolerant option, which means that the minimum supply voltage on-chip is 3.0V.

• Pull down devices are available for 5V tolerant as for normal inputs and sink the same current.

A Pull-up device is also available for 5V tolerant inputs, but it can only ensure an internal logical “1” on a floating input. It can not be used to bias an external node. Indeed, it won’t provide a “1” TTL level outside the chip.

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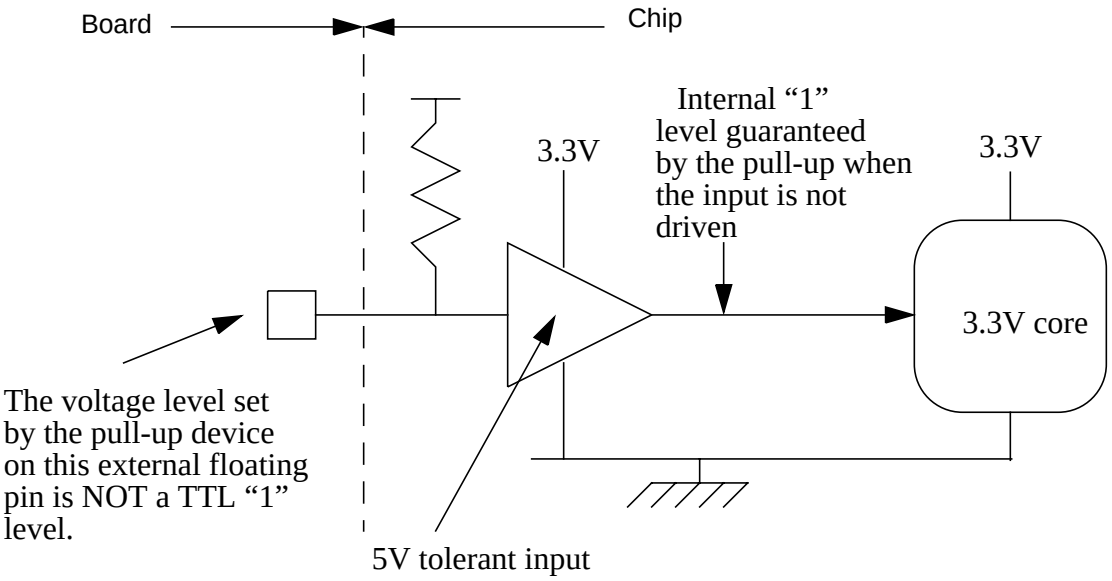

Figure 2: Pull-up device for 5V tolerant inputs

1.2.2 Output buffers

Drive choice:

• The rating of output buffers in mA (2, 4, 8, 3 or 6mA) is a DC specification. This is the current a buffer can source/sink within VOH and VOL specifications, in worst case conditions. The maximum output current, during output switching, is much higher. Please refer to table 7.

• The primary goal of the slew rate control circuitry is to reduce the SLOPE of the CURRENT flowing to/from the load. As the timing degradation is usually not very significant, slew rate controlled buffers should be used as much as possible.

Table 7: Typical current characteristics of output buffers. 25°C, 3.3V, TYP models.

Slew rate control	Current rating	Condition	Typ dI/dT	Typ peak current
YES	2 mA	Cl=35pF	16.5 mA/nS	24 mA
	4 mA	Cl=85pF	20 mA/nS	47 mA
	8 mA	Cl=150pF	23.5 mA/nS	85 mA
	3 mA FT	Cl=60pF	21.5 mA/nS	37 mA
	6 mA FT	Cl=120pF	25 mA/nS	69 mA
NO	2 mA	Cl=35pF	71 mA/nS	25 mA
	4 mA	Cl=85pF	82 mA/nS	50 mA
	8 mA	Cl=150pF	89 mA/nS	100 mA
	3 mA FT	Cl=60pF	122 mA/nS	41 mA
	6 mA FT	Cl=120pF	131 mA/nS	79 mA

The above values are mean values between currents in vdde! and gnde! power lines for one switching buffer.

- In order to reduce the noise on the supplies, it is important to use the smallest buffers compatible with the application timing requirements (refer to timing values in the datasheets) and always prefer buffer with slew rate control.
- For output stages, the difference between TTL and CMOS is only the thresholds at which the timing delays are measured (vdd/2 for CMOS, 1.4V for TLL). The output transistors are the same in both cases.
- In the data-sheets, the slight difference in timing delays between tri-state and non tri-state buffers is due to the extra logic for the tri-state control that adds some delay. The output transistors are the same in both cases.

Five volt Tolerant outputs:

- 5V tolerant output buffers are buffers supplied under 3.3V which can drive external loads from 0 to 3.3V but can sustain 5V signals when in tri-state mode:

:

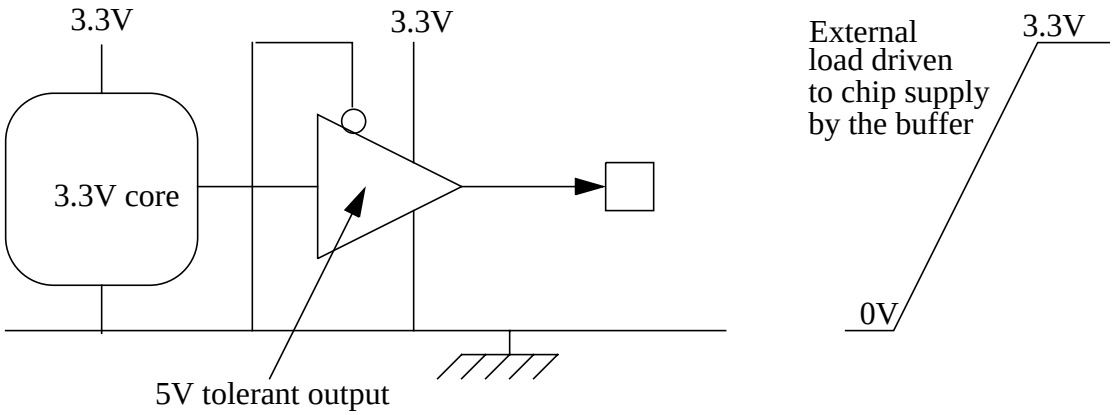

Figure 3: 5V tolerant output buffer in active mode.

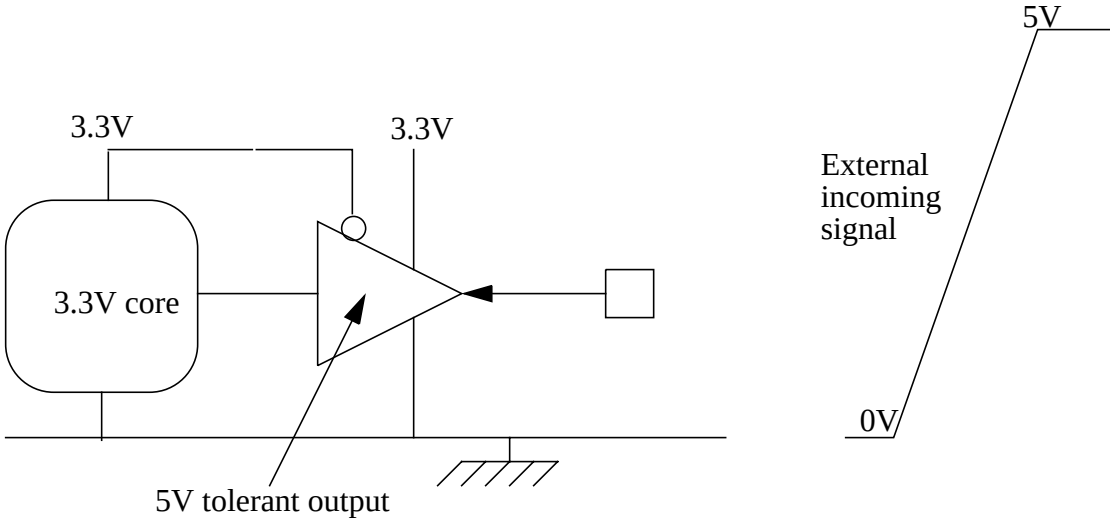

Figure 4: 5V tolerant output buffer in tri-state mode.

- Only TTL buffers are available with the five volt tolerant option, which means that the minimum supply voltage on-chip is 3.0V.
- Only tri-state buffers are available with the five volt tolerant option.
- Five Volt tolerant buffers have a reduced driving capability compared to normal buffers (3 and 6mA instead of 4 an 8mA).

Care must be taken when using 5V tolerant output buffers. Indeed, when they go to tri-state condition (EN goes to “1”) from a 3.3V high state (EN = “0” and A = “1”), they are not quite in a high impedance state. The 5V external chip taking over the bus must be able to:

- source 2.5mA to drive a 3mA 5V tolerant buffer from 3.3V to 5V
- sink 1.1mA to drive a 3mA 5V tolerant buffer from 3.3V to 0V
- source 5mA to drive a 6mA 5V tolerant buffer from 3.3V to 5V
- sink 2.2mA to drive a 6mA 5V tolerant buffer from 3.3V to 0V

These figures are maximum values.
After the buffer has been driven away from 3.3V once, the 5V tolerant buffer is in a true high impedance state.
A design solution to this problem will be implemented in future releases.

1.2.3 Bidirectional buffer

Normal bidirectional buffers are tri-state output buffers associated with an input buffer. All the previous notes on input and output buffers apply to bidirectionals.

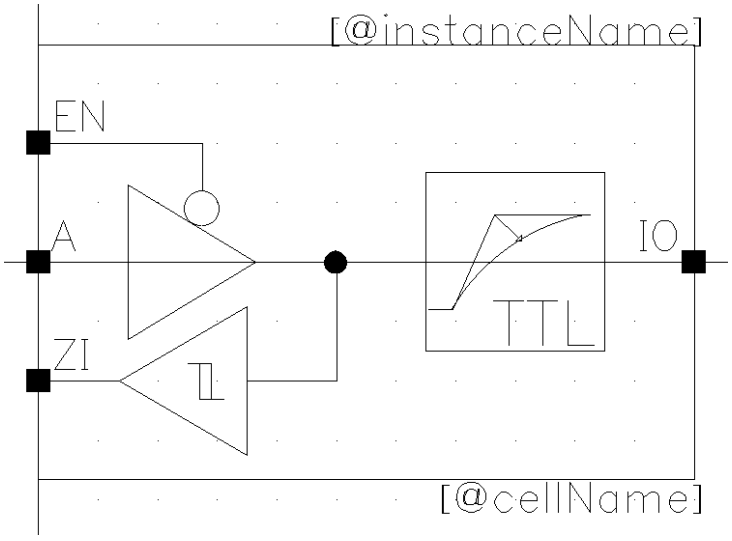

Figure 5: “Normal” bidirectional

Table 8: Modes of operation of a “normal” bidirectional buffer

EN	Function
0	Output buffer. The input signal arrives on A, the cell drives IO (and ZI) with IO = A.
1	Input buffer. The input signal arrives on IO, the cell drives ZI with ZI=IO. A is not used.

Also, tri-state input buffers are available in order to build “true” bidirectional cells to interface external & internal buses:

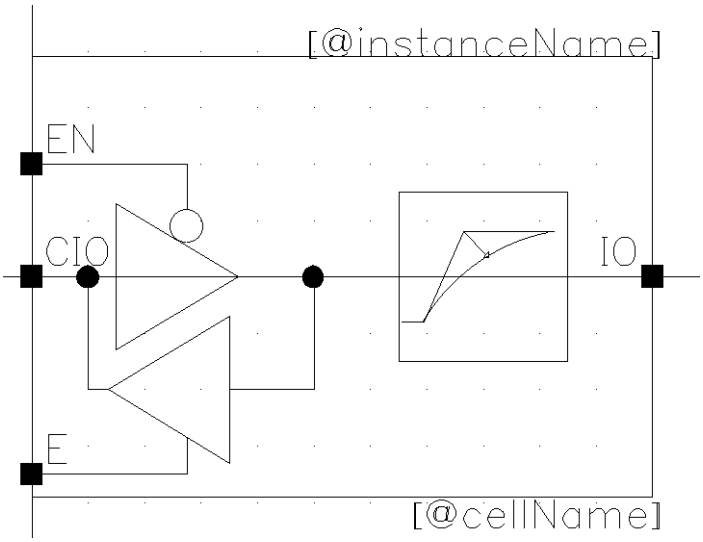

Figure 6: “true” bidirectional

- The suffix “Z” is used in the cell name when the tri-state input option is present.
  Note: Only CMOS input with high drive to core (X16) can be tri-state.

Table 9: Modes of operation of a “true” bidirectional buffer

EN	E	Function
0	0	Output buffer. The input signal arrives on CIO, the cell drives IO with IO = CIO.
0	1	Bus keeper. The cell forces both IO and CIO with IO = CIO.
1	0	Open circuit. Both CIO and IO are in a tri-state mode. The cell doesn’t drive CIO nor IO.
1	1	Input buffer. The input signal arrives on IO, the cell drives CIO with CIO = IO.

The bus keeper configuration of a true bidirectional (EN=0, E=1) must be avoided and is not supported by the library front-end tools.

1.2.4 Pull-up and pull-down active devices - IDDQ compliance

Weak pull-up and pull-down active devices connected to the pad node are available in some of the cells of the library. They fall into two categories: Devices that are always on (U or D suffix in cell names) or devices that can be switched on/off (UQ or DQ suffix in cell names). The switch versions are useful for example when IDDQ testing is required since in this case all IOs can be put in a zero DC power consumption state.

The nominal resistance is typically 50K Ohms (See General specifications).

Table 10: Pull-up and pull-down devices

pull type	pull control pin	Function
Simple pull-up (U)	-	50K Ohm pull-up.
Pull-up with switch (UQ)	T2=0	50K Ohm pull-up.
	T2=vdd	Open circuit, no current.
Simple pull-down (D)	-	50K Ohm pulldown.
Pull-down with switch (DQ)	T3=0	Open circuit, no current.
	T3=vdd	50K Ohm pull-down.

1.2.5 Peripheral buffers

In the “OTHER” category of the MTC45100 library, two peripheral buffers are available: BUF4 and BUF8.

They are identical to B4 and B8 output buffers, but the “Z” output redirected towards the core circuit. They can be used to drive big on-chip loads.

1.2.6 Analog pads

Three analog pads are available in the “OTHER” category.

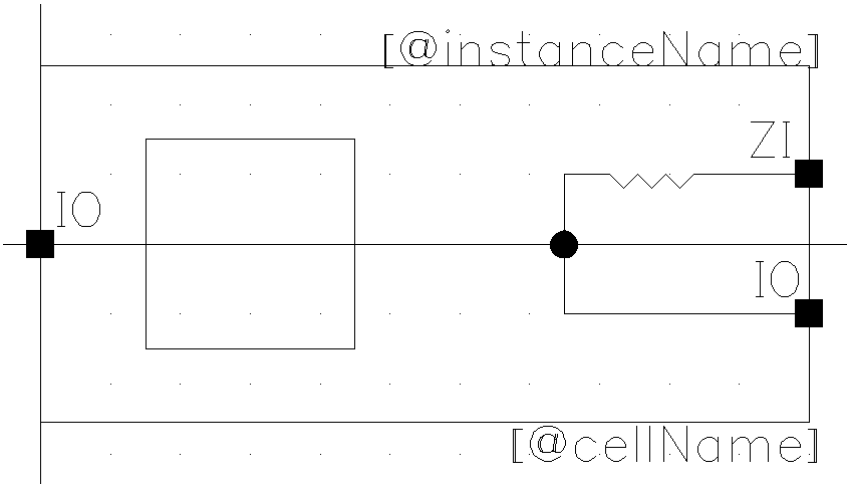

Figure 7: ANA and ANA_OD pads

ANA and ANA_OD are “bidirectional” pads for analog signals. Both contain primary ESD protections in parallel with the pad plus a secondary diode protection after a series resistor. ANA has also protection diodes to vdd. Thus ANA is the best protected cell while ANA_OD can be used when diodes to vdd are not allowed in the application (Signals higher than vdd, for example).

- ZI is the access to core via the series resistor, (440 Ohms). This is the best protected pin against ESD and should be used in particular for input signals.
- IO is a direct access from the pad to the core, bypassing the series resistance. It can be used for output analog signals or any signal when a series resistance cannot be used. The metal2 width is 4um, allowing an equivalent current of 5.7mA in worst case electromigration (T=125°C).

Special care must be taken in the design of the circuit connected to the IO pin of ANA and ANA_OD, in order to guarantee a good ESD performance. Please contact the Unicad support to get design directions.

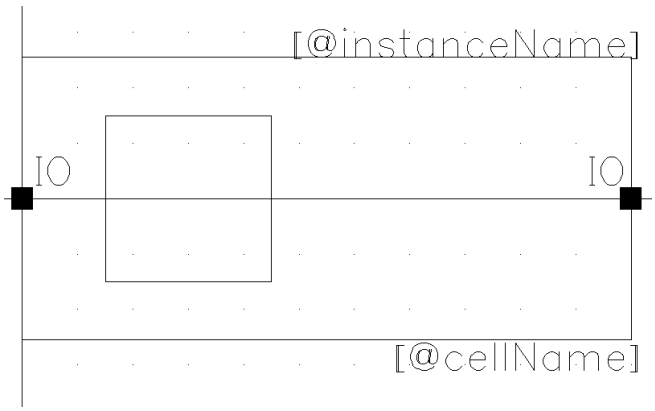

Figure 8: ANA_NOPROT pad

ANA_NOPROT is a simple wire pad, without any protection device.

- The connection width is 15.7um (metal2), allowing an equivalent current of 21mA in worst electromigration case (T=125 ℃).

Use ANA_NOPROT only in extreme cases were NO esd devices can be tolerated and when ESD protection is not an issue (Prototypes, for example). The ESD performance on this kind on pad will probably be very low (depending on the circuit connected to it).

1.2.7 Crystal pad oscillators

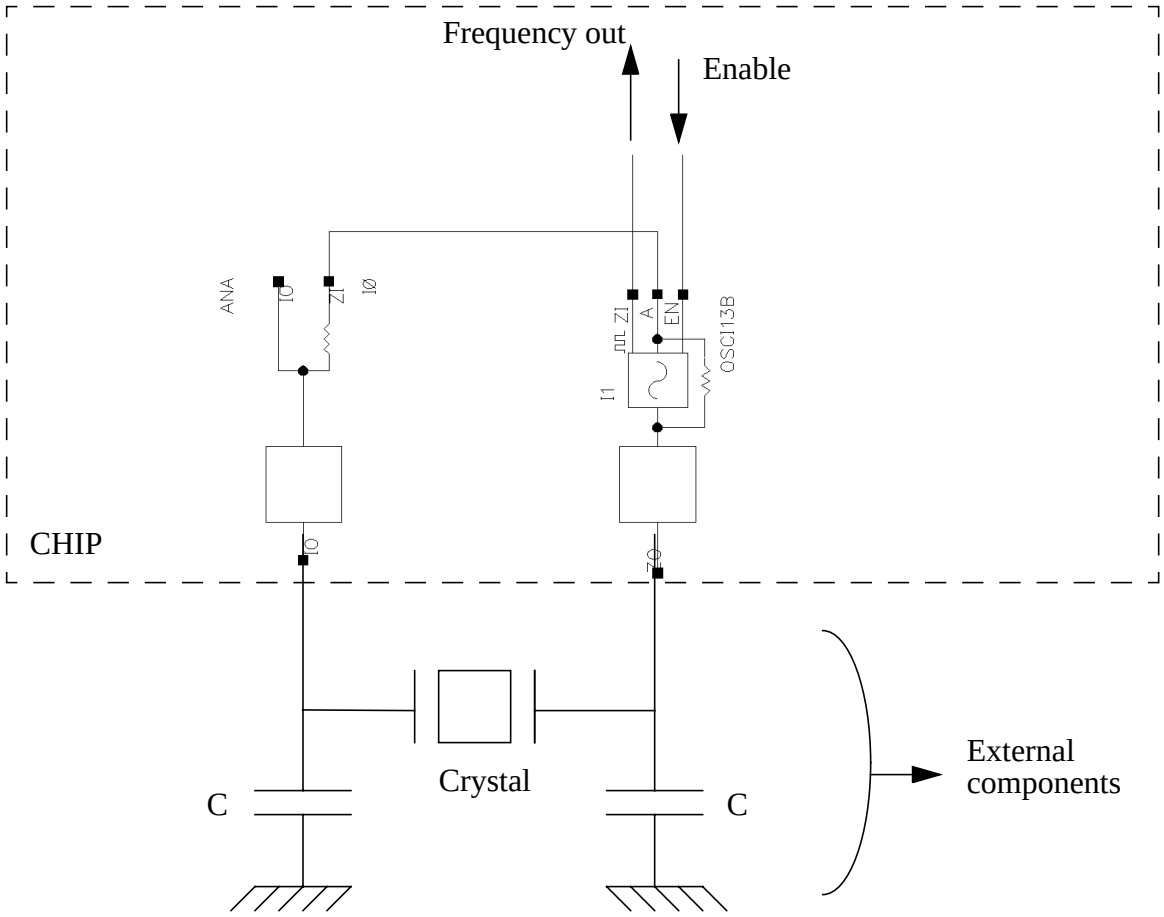

Figure 9: Crystal pad application scheme

The two crystal pad oscillators OSCI13B (13Mhz) and OSCI32B (32Khz) need to be used in conjunction with the ANA pad cell. The full configuration for a crystal oscillator occupies two pads.

Suggested values for C are:

- 27pF for the 32Khz oscillator and
- 16pF for the 13Mhz oscillator.

But other values may be tried depending on the environment (package type...).

- EN = “1” allows oscillations while EN = “0” stops them and the power consumption becomes null.

Table 11: Common crystal pad specifications

	min	typ	max	Note
Power supply	2.7V	3.3V	3.6V	
Temperature	-40 C		+ 125 C	
Static IDD			< 0.1uA	Disabled oscillator. EN= 0

Table 12: 32 Khz crystal pad specifications

	min	typ	max	Note
Frequency		32 Khz		
Start-up time			500mS	
Transconductance	0.29			mA/V

Table 13: 13 Mhz crystal pad specifications

	min	typ	max	Note
Frequency		13 Mhz		
Start-up time			10mS	
Transconductance	0.6			mA/V

1.3 Supplies description

1.3.1 Power distribution in the IOs

There are 6 different metal3 power rails inside the IO cells:
vdd & gnd
vdde & gnde
vddr & gndr

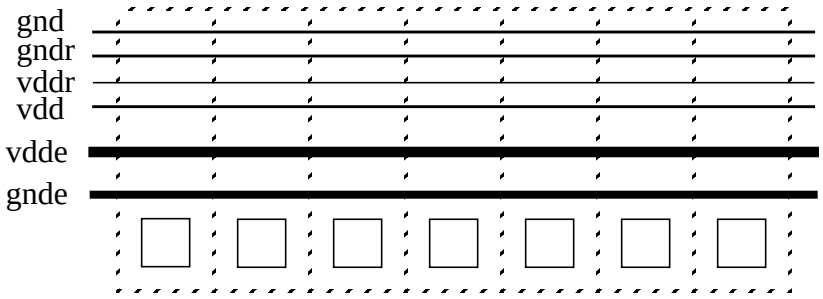

Figure 10: Power rails in IOs

The primary goal of having different rails is to minimize the effect of the noisy output buffers. To do so, the IOs are supplied as follow:

vdde & gnde: External supply, only for output buffers. gnde connects the substrate only next to the pad and output buffers because it is noisy.
vdde & gnde are not available for the core circuitry, they only go through the ring of IO cells.

vdd & gnd: Internal supply: generic digital supply, used for core circuitry as well as pre-drivers in IOs. gnd connects the substrate throughout the chip except near the bonding pads.
This supply is not as noisy as gnde and vdde, but can still have a significant amount of parasitics (especially if highly synchronous logic is present on the chip, for example).

vddr & gndr: This pair is used as a very noise free supply, connecting only front-end receivers of input stages. gndr doesn’ t connect to the substrate at all.
The vddr rail is usually shorted to vdd and gndr to gnd in the power pads.

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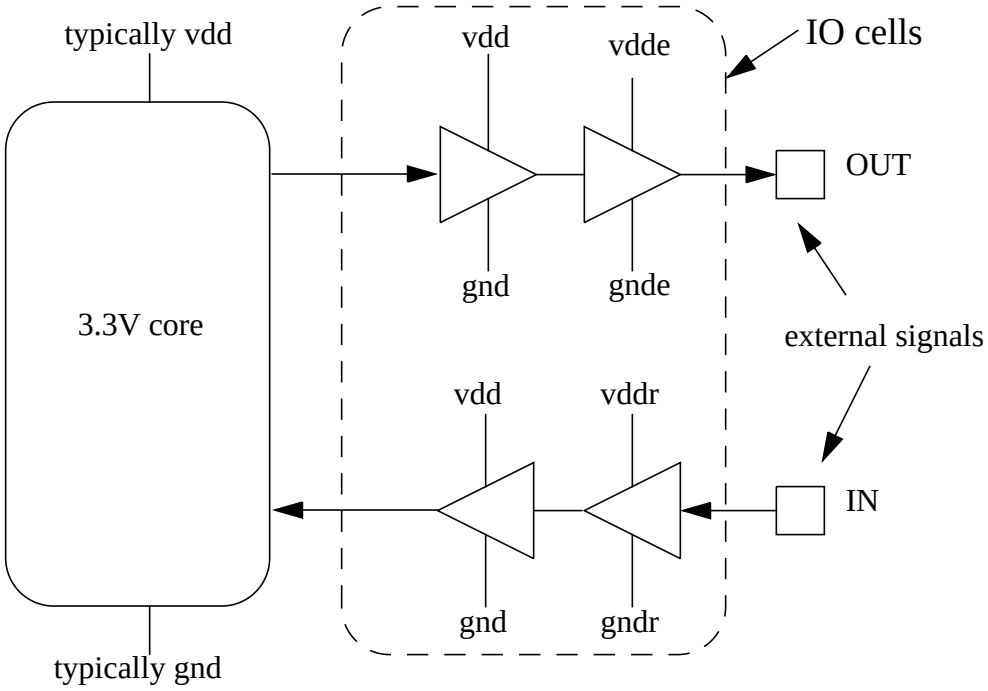


Note: The vddr rail is usually shorted to vdd and gndr to gnd in the power pads.

Figure 11: Power distribution in the IOs

1.3.2 Power pad and corner cell usage

There are a number of power supply pads and corner cells in the “SUPPLY” category of the MTC45100 library.

Usual chip power distribution:

In a “normal” chip, with a unique power for the core & small circuitry in IOs, the following scheme will be used:

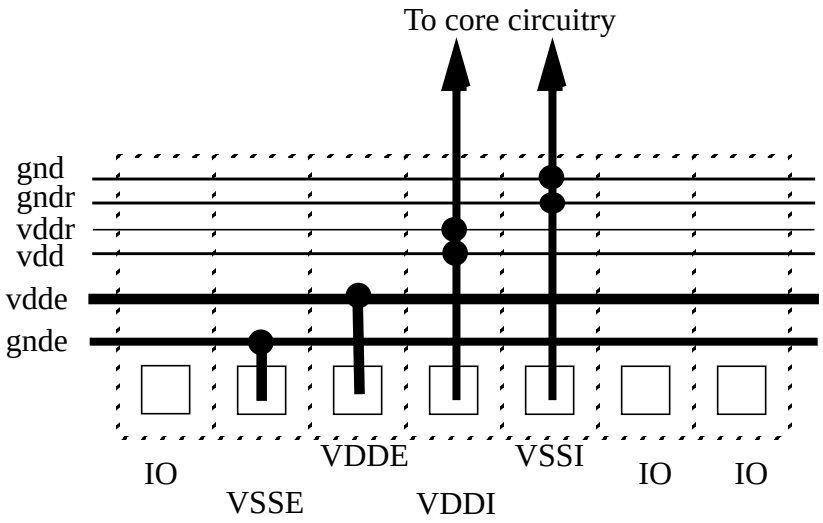


Figure 12: Usual chip power distribution

The following cells are needed:

VDDE	(External supply IO ring only: vdde)
VSSE	(External ground IO ring only: gnde)
VDDI	(Two internal supply IO rings (vdd & vddr) + core)
VSSI	(Two internal ground IO rings (gnd & gndr) + core + substrate biasing)

Note: In that configuration, vddr is shorted to vdd and gndr to gnd.

The VERY MINIMUM power pad set to be used in any chip is:
VDDI + VSSI + VDDE + VSSE power pads.

! If one of them is missing, the IOs will NOT work!

These pads must be placed several times throughout the periphery, depending on the chip:

The number of VDDI/VSSI pairs is a function of the core power consumption: The electromigration rules allow a maximum average current of 125 mA through each VDDI or VSSI pad.
This is an absolute maximum rating.
In practise, the number of VDDI/VSSI pairs must be defined by studies of voltage drops and ground bounce. The type of core circuitry will be critical in this evaluation (frequency, peak currents, etc...).
This calculation is not is the scope of this document.

The number of VDDE/VSSE pairs is primarily a function of the spikes on the on-chip supply rails generated by the switching output buffers. Ideally, many parameters should be taken into account, such as package type, on-chip capacitance between vdde and gnde, IO pad type, presence of analog blocks on chips, etc...
An acceptable compromise is often reached with the following rule: **One VDDE/VSSE pair is necessary for each 100mA of standardized output current**. The standardized output current is given below for the different buffer types:

Table 14: Standardized output currents

Slew rate control	Current rating	Standardized current
YES	2 mA	6
	4 mA	8
	8 mA	16
	3 mA FT	8
	6 mA FT	16
NO	2 mA	28
	4 mA	32
	8 mA	32
	3 mA FT	32
	6 mA FT	32

(Number of VDDE/VSSE pairs) =
(Total standardized output current) / 100.

As an example, 1 VDDE/VSSE pair in needed for three 8mA without slew rate control buffers, while 1 pair is enough for twelve 4mA with slew rate control buffers.
Input stages account for 0mA of standardized current.

Anyway, all unused package pins should be dedicated to extra power pads, even if the above recommendations are already met.

By construction, all the VDDI power pads on a chip are connected together via the IO ring. Same remark for VSSI, VDDE and VSSE.

Chip power distribution with independent core supplies:

In some cases, independent power pads may be needed to supply some parts of the core chip. For example to supply a sensitive analog block with a clean power distribution, or supply parts of the chip that

can be powered down while others are still active, etc...
The following scheme can be used

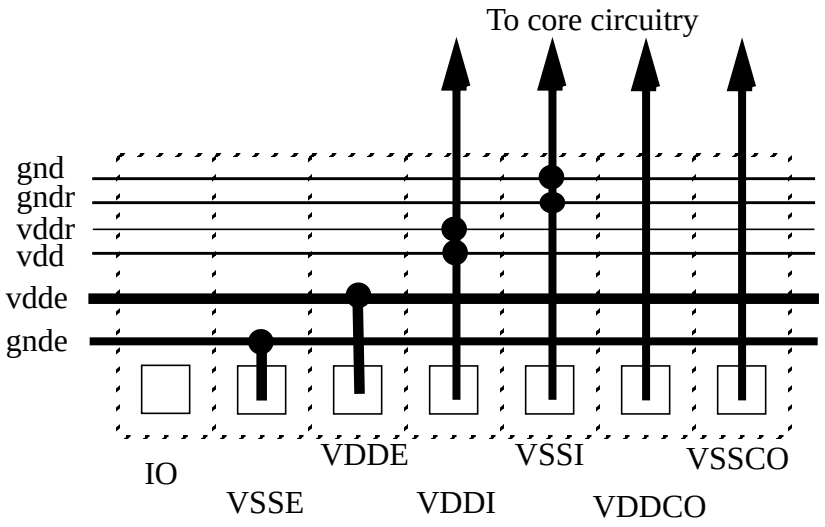


Figure 13: Chip power distribution with independent core supplies

Two cells are available in the MTC45100 library for this purpose:

VDDCO	(Internal supply for core circuitry only)
VSSCO	(Internal ground for core circuitry only)

The number of VDDCO/VSSCO pads is determined as for the VDDI/VSSI pads, depending on the current they are supposed to carry.

Even when the whole core is supplied via VDDCO and VSSCO pads, a number of VDDI and VSSI pads is still required so that the IOs work properly. A minimum of one VDDI/VSSI pair every 30 IO pads is recommended.

1.4 Layout IO structure

1.4.1 Programmability:

An important feature of the CMOS035 IO library is the possibility to program IO buffers at metal level. A unique base is common to all IOs, containing all the devices up to contact level.
Via1, metal1, via2 & metal2 are the programmable layers which connect the base components to build the different IO functions.
Upper levels (from via3 to metal5) are again common to all IOs.

- This feature makes the IO library compatible with an hybrid array chip methodology.

Limitation:

- The power pads have a different base, so they cannot be programmed as IO buffers. However, all power pads have the same base so that any power pad can be replaced by another one by metal fix.
- This particular release has a polysilicon difference between 5V tolerant buffers and 3.3V buffers. This is due to an ESD clamping devices using a polysilicon gate in 3.3V buffers which needs to be further qualified before being used also in the 5V tolerant environment. For the time being, the poly gate has been removed from 5V tolerant buffers.
- The ANA_NOPROT pad is not programmable (simple wire pad).
- The crystal pad oscillators are not programmable.

1.4.2 IO floorplan and cross-section

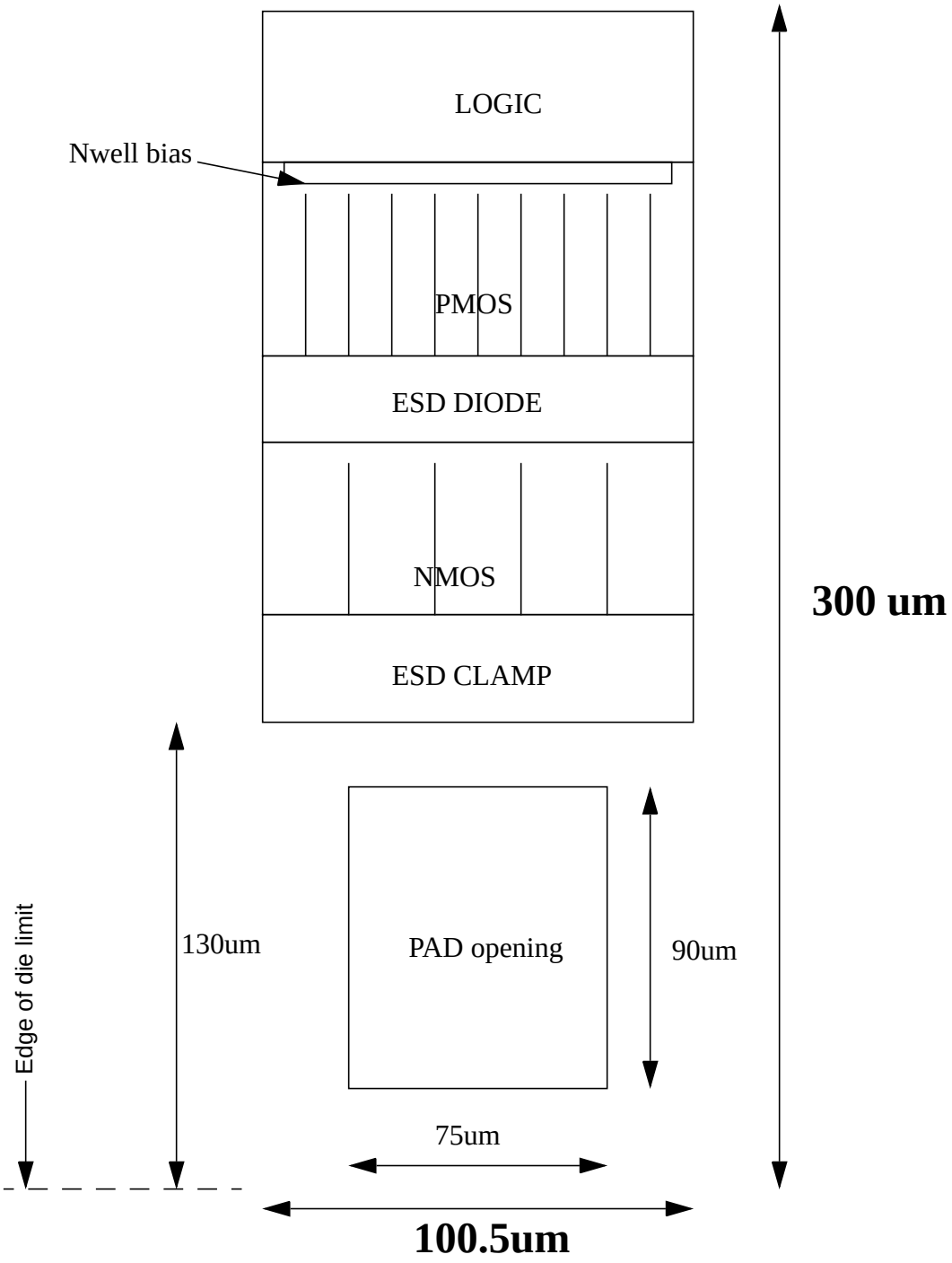


Figure 14: Cell floorplan common to all buffers

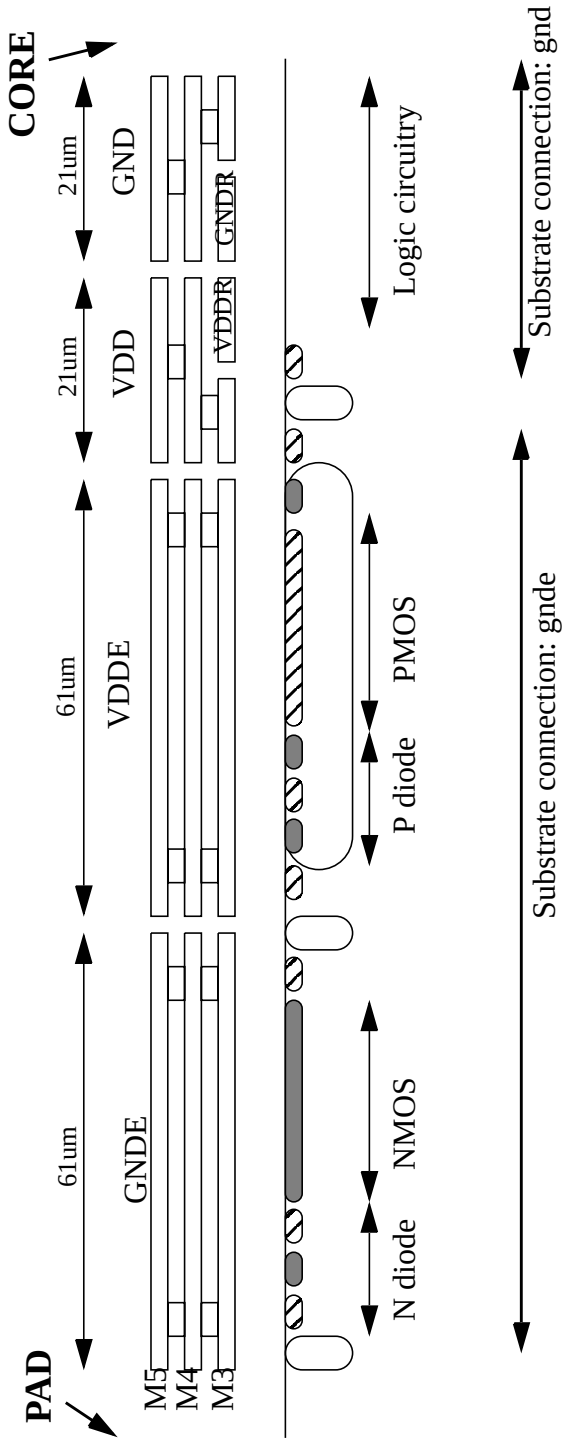


Figure 15: Cross section of IO cells - Bonding pad not shown -

1.5 Placement and routing of IO cells

Some advice on the IO placement is given here for chips ASSEMBLED BY HAND.
For automatic P&R, please refer to the proper cell3Kit documentation.

1.5.1 IO placement - latchup guard band continuity -

In the “P&R” category of the library, you’ll find cells dedicated to the placement and routing of the IOs at top chip level.

The IOs cells must be laterally terminated in order to ensure an optimum latch-up behaviour. This can be achieved by:

Abutment: All cells can be abutted to each other. The metal power ring continuity is automatically ensured by abutment.

If there is free spaces between IOs (core limited chip), filler cells must be used to fill up these empty areas. There are different filler cell widths:

IOFILLER1: 1.5um wide
IOFILLER2: 3.0um wide
IOFILLER4: 6.0um wide
IOFILLER8: 12um wide
IOFILLER16: 24um wide
IOFILLER32: 48um wide
IOFILLER64: 96um wide

It is advised to start the filler cell placement by the widest cell possible and then continue with decreasing sizes until the gaps are completely filled.
(Note: When using the cell3 kit package for automatic P&R, these filler cells are automatically placed).
Filler cells contain latchup guard bands which will provide a good latchup immunity and also metal tracks to ensure the continuity of power metal rails.

It is mandatory and easier to use a 1.5um snap grid when placing and routing IOs by hand. Otherwise filler cells won't fit between IOs.

If, for some reason, the IO ring must be interrupted and filler cells can't be used, the IO ring must be terminated by the IOEND cell.

This can be the case of a chip with digital IOs only on one side, the other part being purely analog; or if an active circuit is inserted between distant IOs beneath the power metal tracks.

Metal tracks (metal 3, 4 and 5) can be continued beyond an IOEND cell using the IOPCELL device. This is a programmable cell with variable width containing only metal rails.

IOEND and IOPCELL are not handled by the cell3 kit. They are provided only to solve specific situations. (Manual placement).

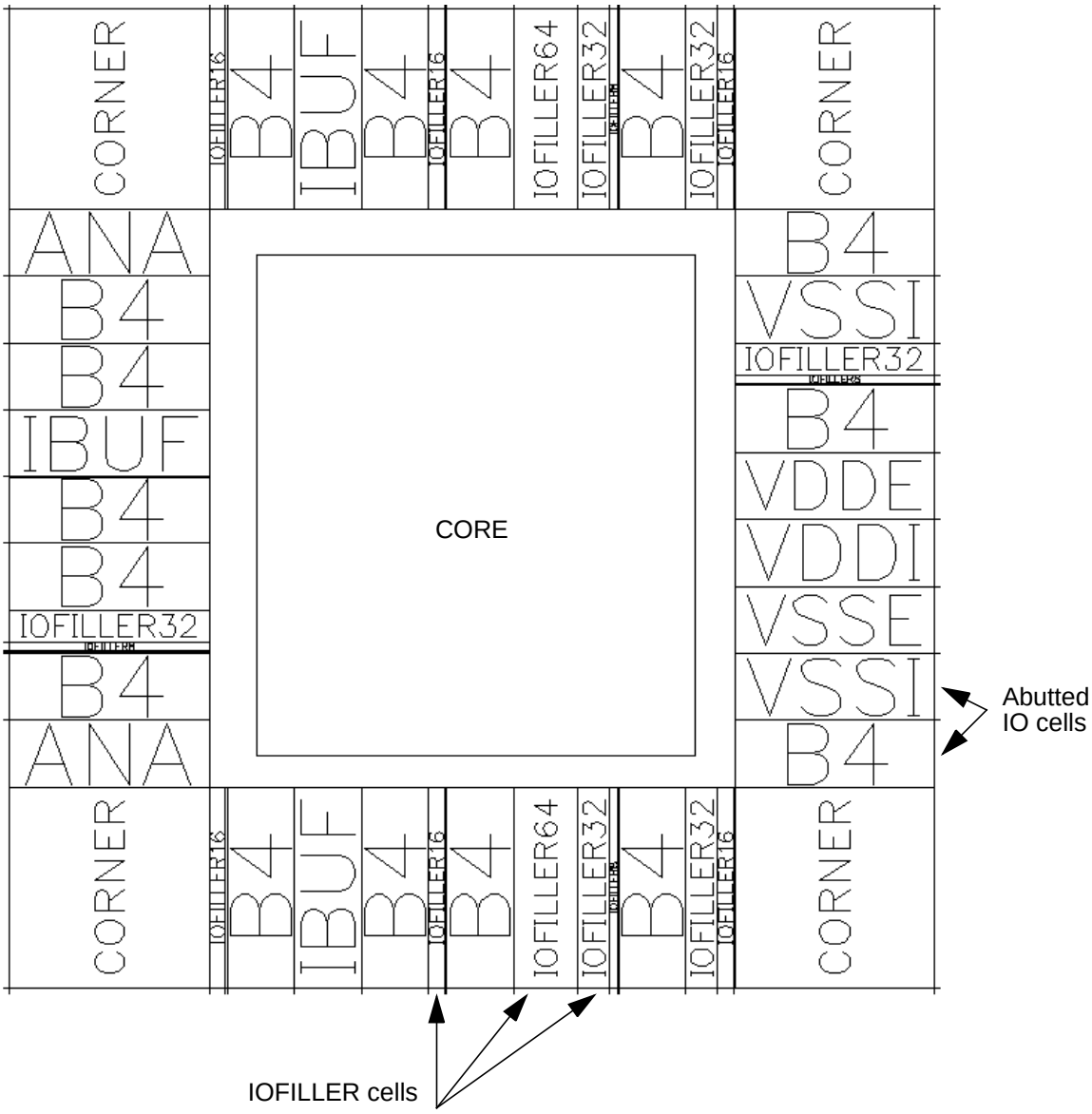


Figure 16: Example of a classical IO ring placement

The example above shows how IOFILLERx and CORNER cells are used to build a “normal”, closed IO ring. All the elements must be abutted and not overlapping.

This kind of IO ring can be assembled by hand (remember: use a 1.5um snap grid) or automatically by the cell3 kit which takes care of IOFILLERx and CORNER cells.

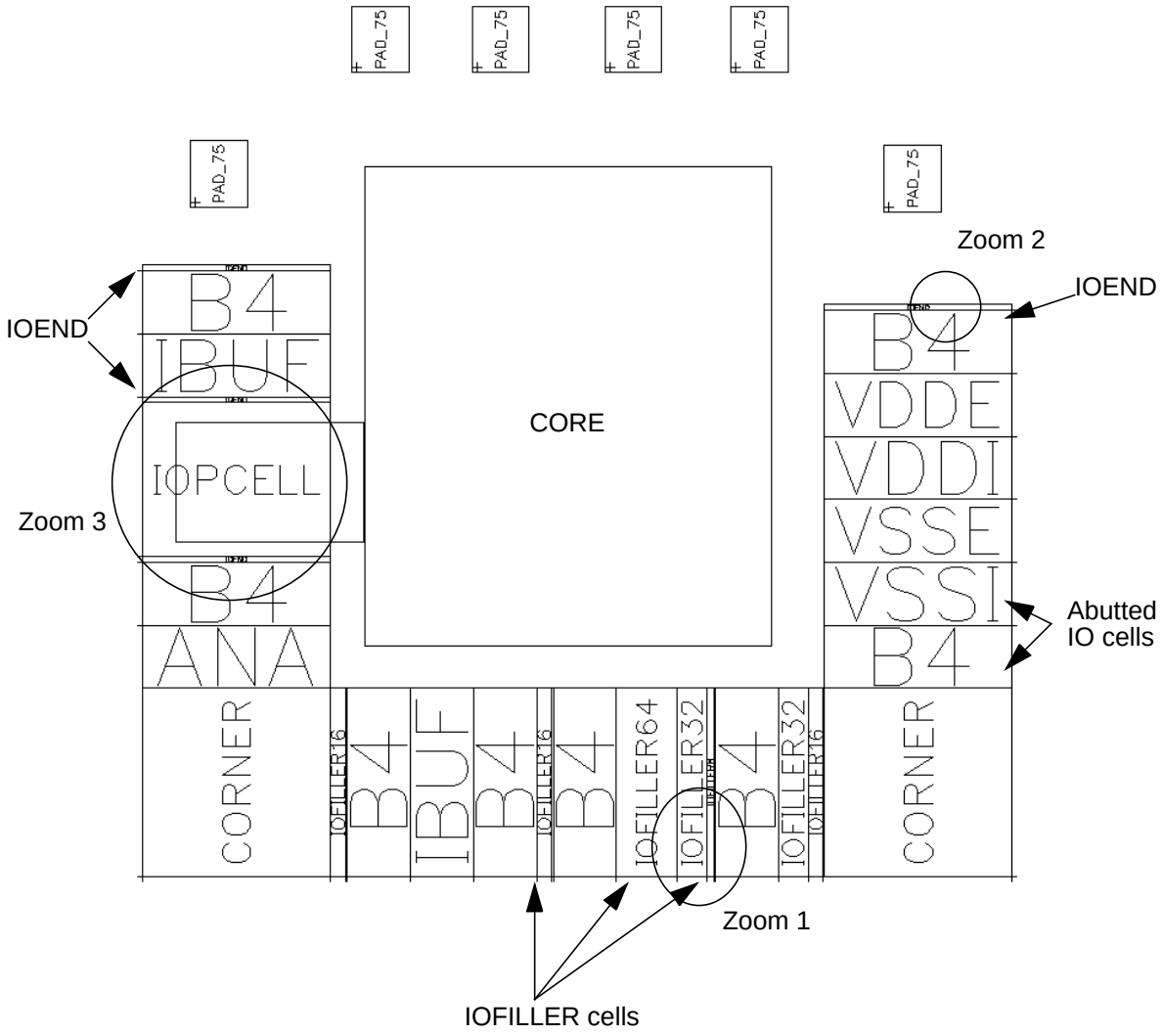


Figure 17: Example of a specific, manually assembled IO ring

The example above shows how to use the IOFILLERx, CORNER, IOEND and IOPCELL cells to build a more complex, interrupted IO ring.

This kind of IO ring is assembled manually (remember: use a 1.5um snap grip).

Please refer to the 3 next figures for more details (Zooms 1, 2 and 3).

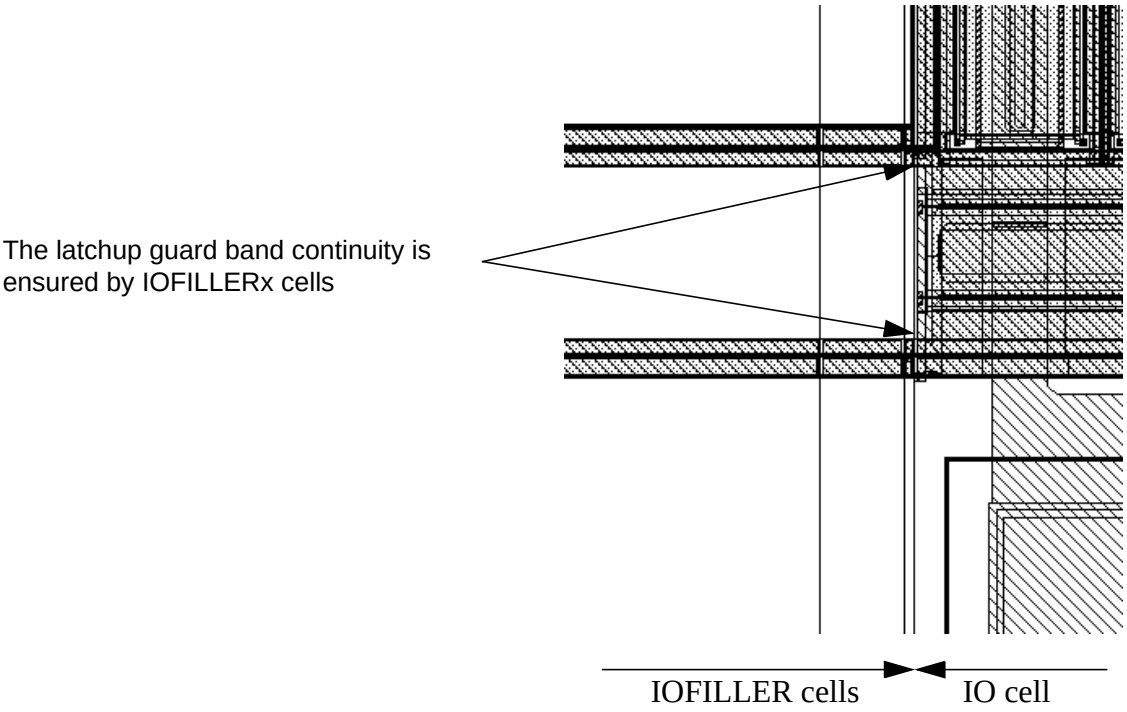


Figure 18: Zoom 1: Latchup guard band continuity with IOFILLERx cells.

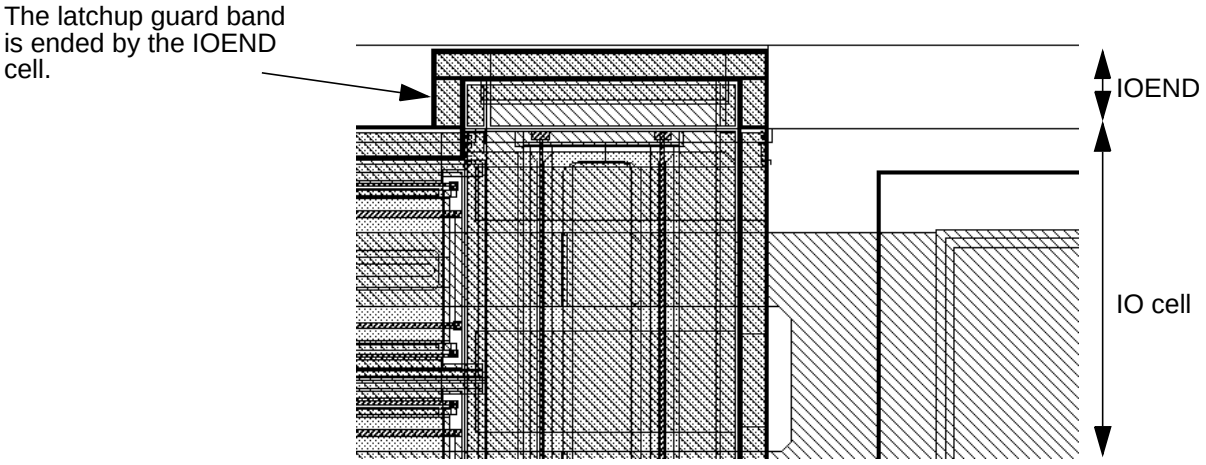


Figure 19: Zoom 2: Latchup guard band termination with IOEND cell.

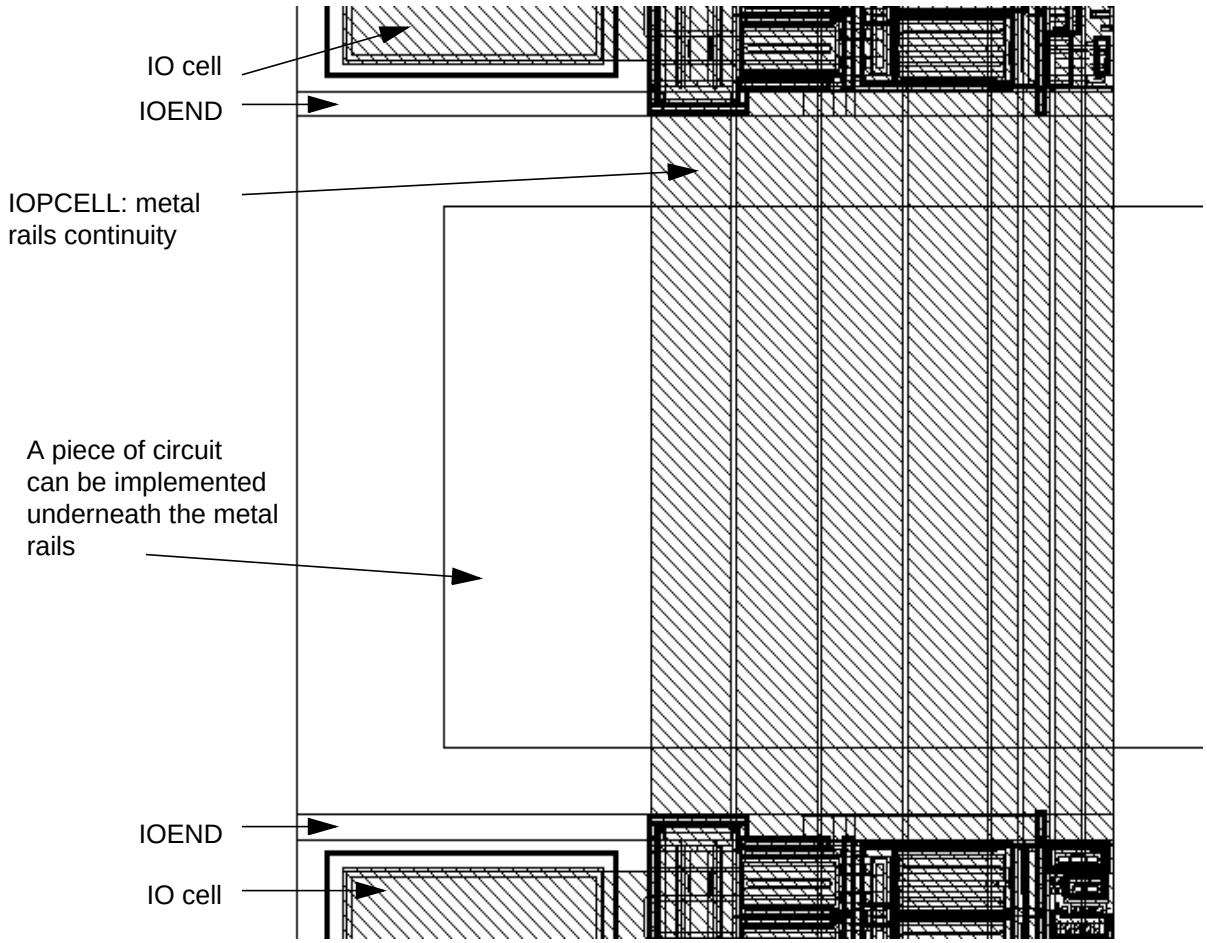


Figure 20: Zoom 3: Latchup guard band interruption, continuity of metal power rails

1.5.2 Power line routing

As shown in the “IO structure” chapter, 3 metal layers are dedicated to power busing (M3, M4 & M5) on top of the IO cells. These rails are only dedicated to supply the IO cells, they are not designed to distribute power and ground to the core circuit.

However, M5 power rings are interrupted in power cells (VDDI, VSSI, VDDCO and VSSCO) to allow a low-resistance supply to core in M5. The maximum current to core is then 125mA for each power pad, and the series resistance is limited to 0.1 Ohm.

A metal 4 access pin is also available at the top of the power pads. This allow a power distribution to core both in metal4 and metal5, making the top chip assembling more flexible.

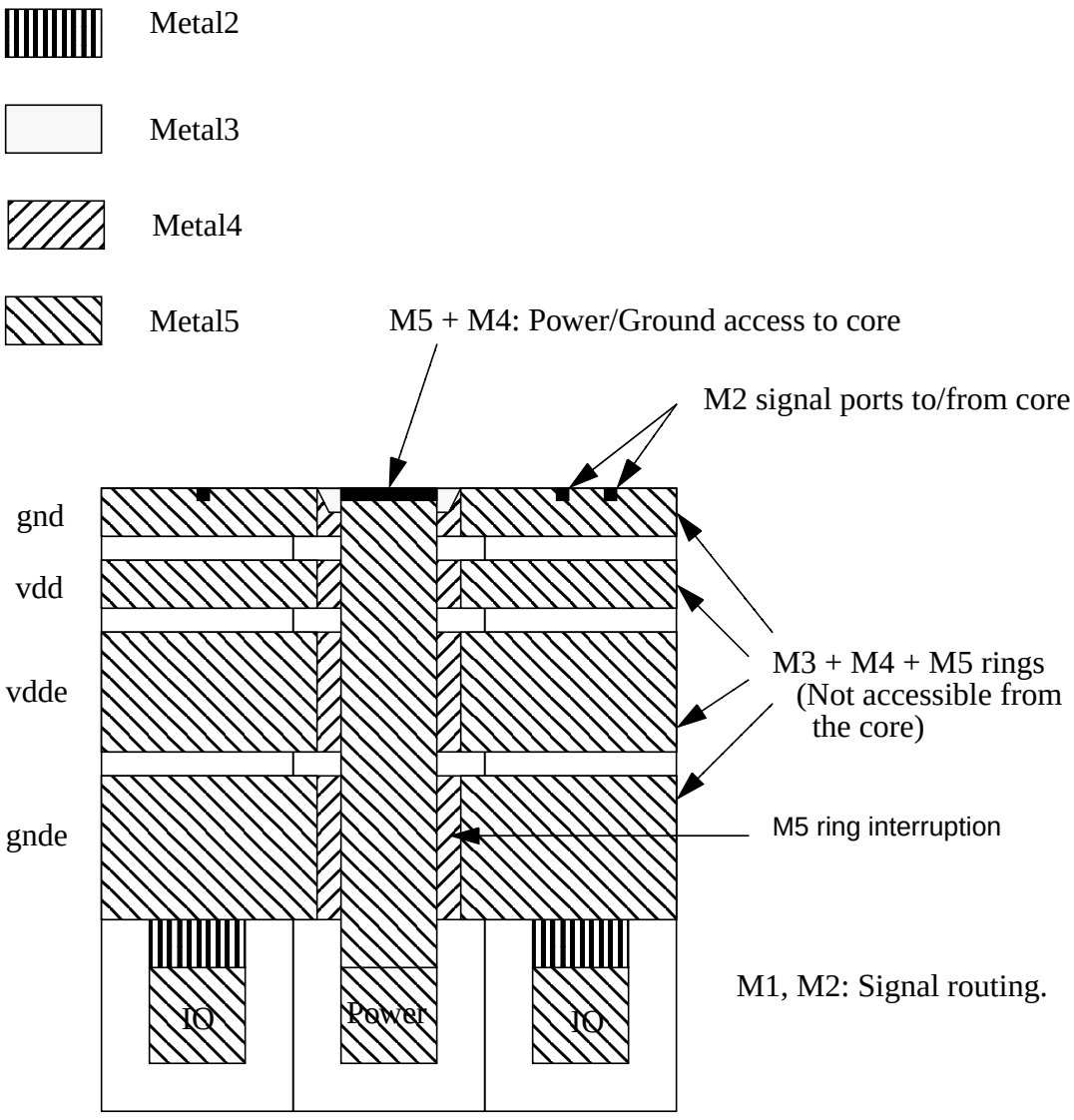


Figure 21: Metal usage in IOs

1.6 Power supply pads in schematics

Power pads have cmos.sch and symbol views. Indeed, there is some ESD circuitry inside each of them which needs to pass the LVS.

EACH power pad used in the layout must also be present in the schematic. VSSI, VSSE, VDDI and VDDE symbols only need to be instantiated. No connections are required (global nets).

VDDCO and VSSCO symbols need to be specifically connected to the core, either directly or via global nets (Please refer to the next figure).

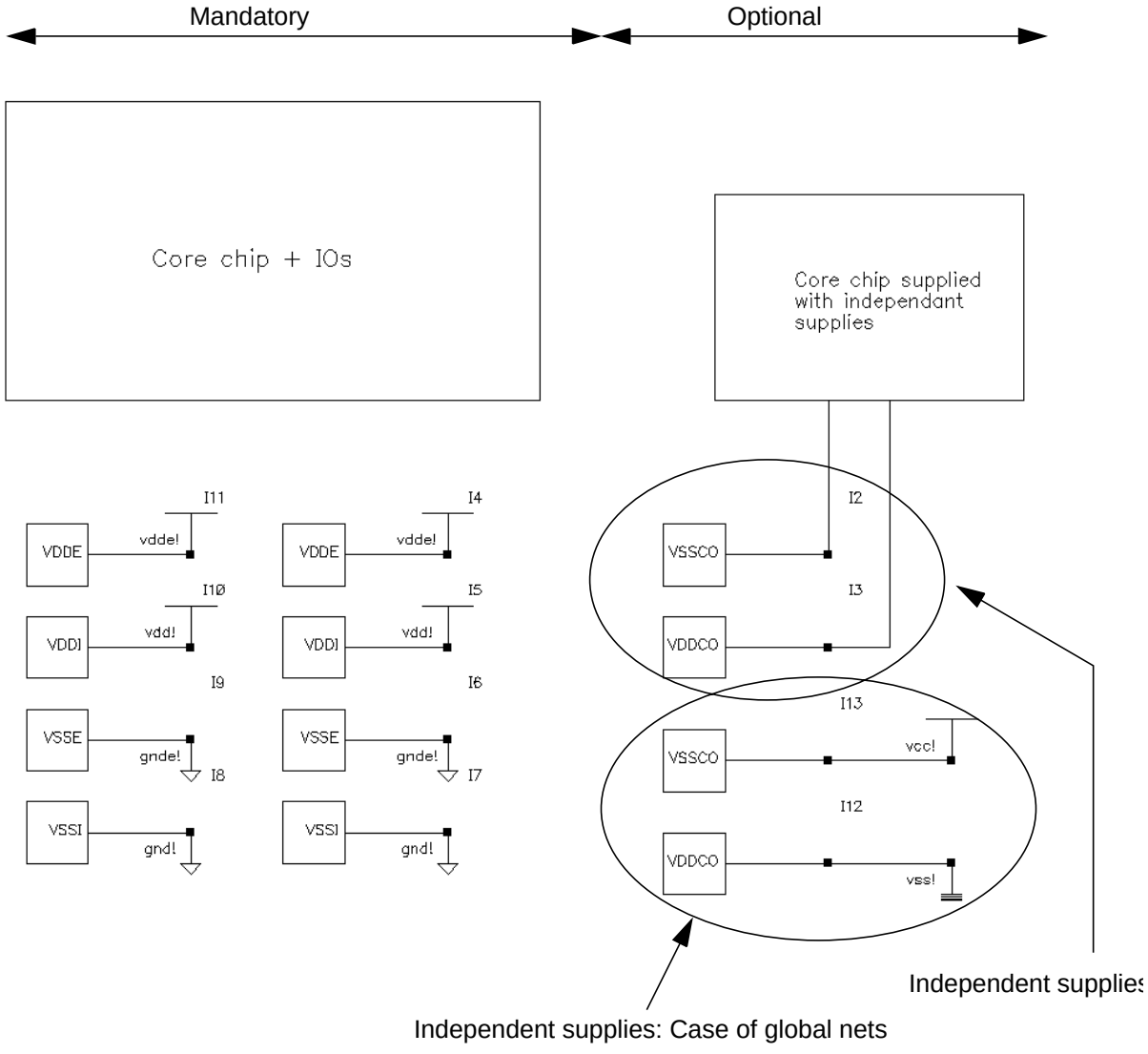


Figure 22: Power pads must be present in the top cell schematic

1.7 Diva & Dracula verifications

1.7.1 General

IO cells should always be checked (DRC or LVS) at chip top level. It is not recommended and useless to check an IO cell alone.
Indeed, the 6 metal power rails present in each cell are properly connected only in power pads at chip level.
Please contact the Unicad support if verifications at cell level are required (In case of specific IO developments, in particular).

DRC

IOs are DRC free both with DIVA and Dracula checks.

The ERC1 and ERC2 switches available in the dracula decks should not be passed on the IOs.

- ERC2 will flag unconnected devices.
- ERC1 will flag all wells because it looks for connections (VSS and VDD) unknown in the IOs where gnd, gnde, vdd and vdde are used:

```
ERC1354     54      11.00   11.00 3190.00 3190.00          2275
LCONNECT   PWELLC             DISC    VSS?    OUTPUT ERC13 54

ERC1454     54      130.00  130.00 3071.00 3071.00         1673
LCONNECT   NWELLC             DISC    VDD?    OUTPUT ERC14 54
```

LVS

The notes on DIVA LVS and DRACULA LVS in this document mainly deal with power supply issues. It is assumed as prerequisite that IO pins (signal pins) are properly labelled. In particular, the “IO label” facility of the Cell3 kit may be used to add Dracula IO labels on the chip layout.

In the cmos.sch views, 4 global nets define the power supply distribution in the IOs: gnd!, vdd!, gnde! and vdde!. This means that on the layout these 4 nets must be identified on power pads at top level.

gnd! must be added on the pad of VSSI
vdd! must be added on the pad of VDDI
gnde! must be added on the pad of VSSE
vdde! must be added on the pad of VDDE

When the VDDE, VSSE, VDDI and VSSI pads are repeated several times around the chip as previously recommended, only one instance of each needs to be labelled.
Indeed, as already mentioned, all the VDDI power pads of a chip are connected together via the IO ring. Same remark for VSSI, VDDE and VSSE.
If independent supplies are present on chip via VDDCO and VSSCO power pads, EVERY VDDCO and VSSCO pad must be labelled with the appropriate labels.

1.7.2 DIVA LVS

Preparation of the layout:

For DIVA, the Cadence global net "!" syntax must be used for power labels. Labels in metal5 purpose pintext layer and/or pins in metal5 purpose pin layer can be used.

If only labels are used, please note that DIVA will not recognize the terminals in the extracted view. For that reason, even though no unmatched terminals are reported in the LVS log file, the total number of terminals in the extracted view and in the schematic view differs:

	layout	schematic
	terminals	
un-matched	0	0
total	0	48

However, this does not prevent the netlists from matching.

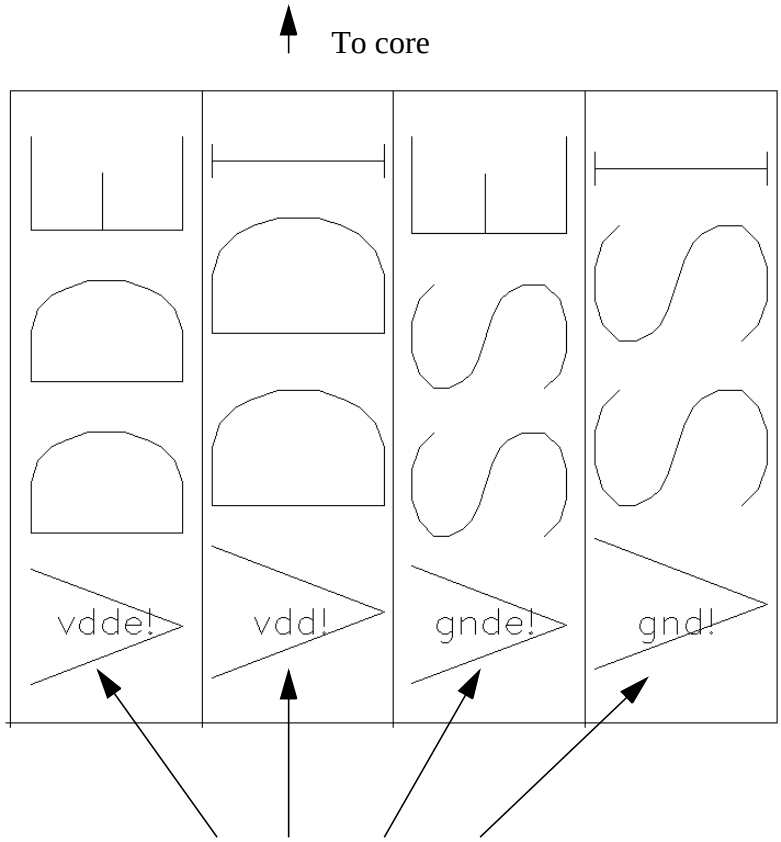


Figure 23: Layout preparation for DIVA LVS

Running DIVA LVS

When using piull-up and pull-down IO cells, the LVS option "Apply device fixing" must be used.

1.7.3 DRACULA LVS

Preparation of the CDL netlist:

The first item to take care of is the declaration of power/ground nodes in the CDL netlist:

Indeed, “vdd” and “gnd” are key words and are always recognized as power and ground nodes, but “gnde” and “vdde” are not. They need to be

specifically declared with ":G" and ":P" suffixes as shown below:

```
*****************************************************************
* Global Net Declarations                                       *
*****************************************************************
*.GLOBAL VDD GND gnde:G vdde:P gnd vdd
```

The addition of ":P" and ":G" must be done manually.

The second concern is the presence of diodes and resistors in IO cells. For this reason, the following lines must appear in the CLD netlist of the circuit:

```
*****************************************************************
* BIPOLAR Declarations                                          *
*****************************************************************
*.BIPOLAR
*.RESVAL
```

These statements can be added by hand or be generated automatically by choosing the following options in the Translators->Netlist->CDL out form:

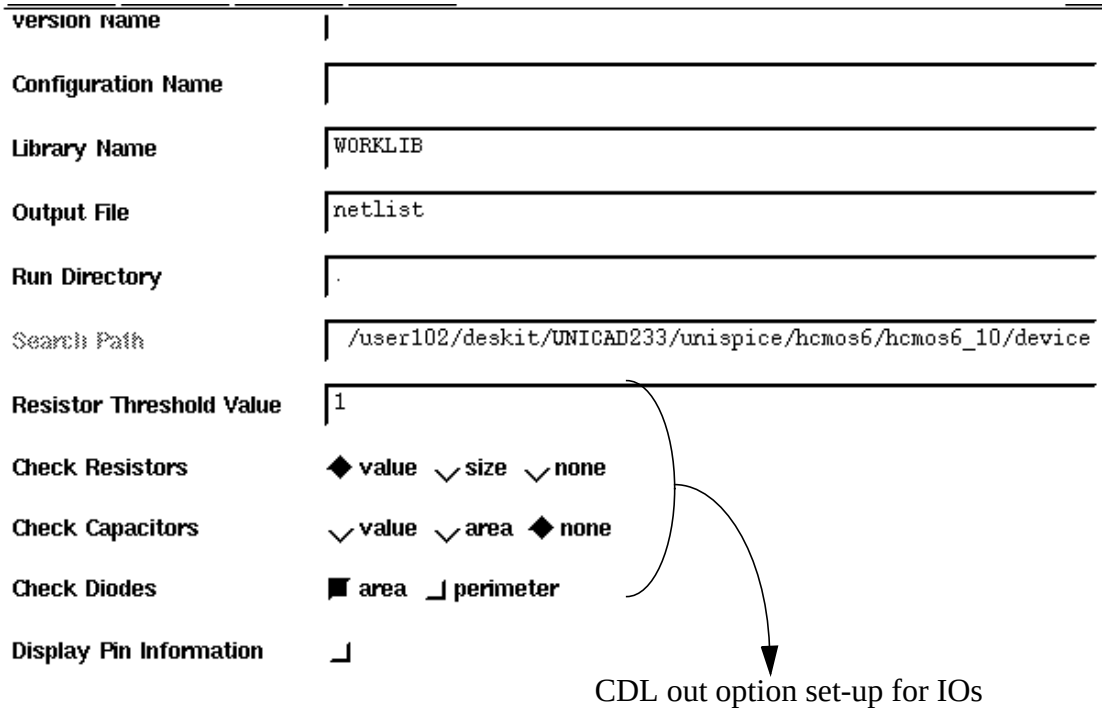


Figure 24: CDL out option form for IOs

Notes:
- it is important to change the default “Resistor Threshold Value” from 2000 to less than 90 which is the value of the resistors in the IOs.

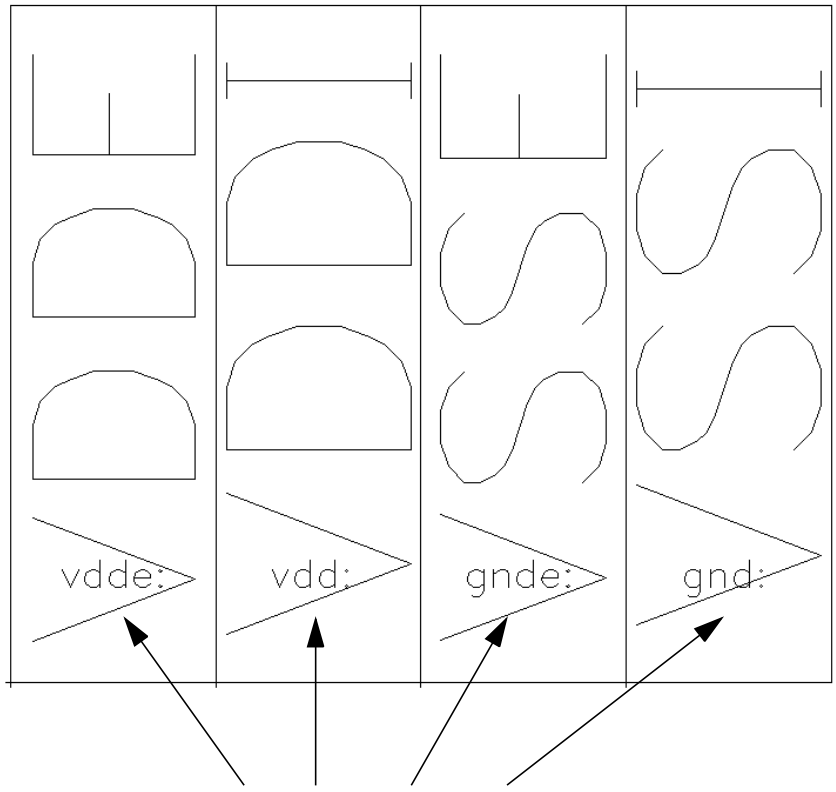
-False discrepancies are reported concerning diodes. These messages can be ignored.

```
**************************************************
********** DISCREPANCY POINTS LISTING **********
**************************************************

** WARNING **      16 SCHEMATIC RES DID NOT SPECIFY WIDTH
** WARNING **      26 SCHEMATIC DIODE DID NOT SPECIFY AREA
** WARNING **  26 SCHEMATIC DIODE DID NOT SPECIFY
PERIPHERY
```

Preparation of the layout

For DRACULA, it is recommended to use the Dracula global net ":" syntax:



labels in metal5 purpose flatext for DRACULA checks

Figure 25: Layout preparation for DRACULA LVS

Case sensitivity

In dracula LVS, the label names can be kept as is or turned to Upper cases. In both situations, you must ensure a good compatibility between the schematic cases and the layout cases.

To keep the case sensitivity:

• The supply names in the CDL netlist are in Lower cases.

• In the LOGLVS program, type the command

:CASE

to keep these lower cases.

• Use lower cases for supply labels in the layout

• By default in the dracula file, the option

CNAMES-CSEN = yes (Keep case sensitivity) is OK.

To turn all cases to Upper:

• Don't use the

:CASE

command in LOGLVS. All the CDL netlist cases will be turned to Upper cases.

• Use only Upper cases for labels in the layout and/or switch the option

CNAMES-CSEN = no (In the dracula file).

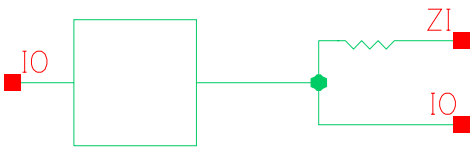
The "Case sensitivity" option that can be set for the GDS2 file generation (Stream out options) concerns only instance names. It doesn't affect cases of labels.

Dracula file preparation:

Add the Z filter option for layout to the default setting:
FILTER-LAY-OPT = BCDEHIJKOZ; layout filtering set
Otherwise, some floating layout resistors are reported as unmatched.

CMOS035 MTC45100	Analog Pad Buffer	ANA

SYMBOL



BEHAVIOUR

IO	ZI	IO
1	1	
1		1

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
IO	1.900 pF

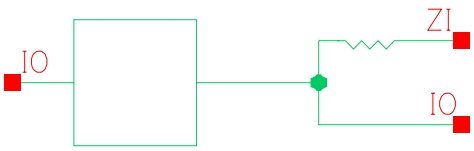
OUTPUT Pin	Max. load
IO	0.352 pF
ZI	38 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	5.0xSL	10.0xSL	20.0xSL	@maxLoad
IO to ZI	Fall delay	0.20	0.20	0.20	0.20	0.20
IO to ZI	Rise delay	0.20	0.20	0.20	0.20	0.20

CMOS035 MTC45100	Analog Pad Buffer	ANA_OD

SYMBOL



BEHAVIOUR

IO	ZI	IO
1	1	
1		1

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
IO	1.900 pF

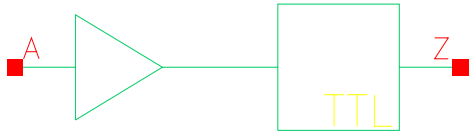
OUTPUT Pin	Max. load
IO	0.352 pF
ZI	38 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	5.0xSL	10.0xSL	20.0xSL	@maxLoad
IO to ZI	Fall delay	0.20	0.20	0.20	0.20	0.20
IO to ZI	Rise delay	0.20	0.20	0.20	0.20	0.20

CMOS035 MTC45100	TTL Output Pad Buffer, 2mA	B2

SYMBOL



BEHAVIOUR

A	Z
11	

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.2 SL

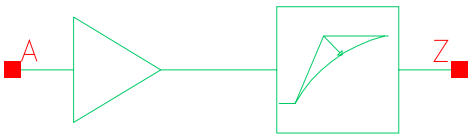
OUTPUT Pin	Max. load
Z	50.000 pF

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		12.50pF	25.00pF	37.50pF	50.00pF	@maxLoad
A to Z	Fall delay	1.84	2.80	3.77	4.73	4.73
A to Z	Rise delay	1.62	2.29	2.97	3.64	3.64

CMOS035 MTC45100	CMOS Output Pad Buffer, 2mA, with Slew Rate Control	B2CR

SYMBOL



BEHAVIOUR

A	Z
11	

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.2 SL

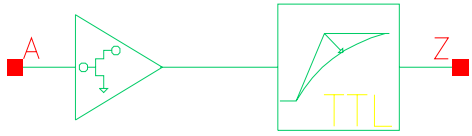
OUTPUT Pin	Max. load
Z	50.000 pF

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		12.50pF	25.00pF	37.50pF	50.00pF	@maxLoad
A to Z	Fall delay	2.27	3.14	3.98	4.81	4.81
A to Z	Rise delay	2.27	3.09	3.90	4.70	4.70

CMOS035 MTC45100	TTL Open Drain Output Pad Buffer, 2mA, with Slew Rate Control	B2ROD

SYMBOL



BEHAVIOUR

A	Z
0	0
1	Z

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.2 SL
Z	1.397 pF

OUTPUT Pin	Max. load
Z	50.000 pF

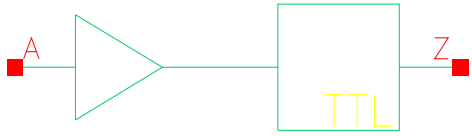
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
A to Z	0Z delay	0.55	0.62	0.87

Timing/Load		12.50pF	25.00pF	37.50pF	50.00pF	@maxLoad
A to Z	Z0 delay	2.24	3.23	4.20	5.17	5.17

CMOS035 MTC45100	TTL Output Pad Buffer, 4mA	B4

SYMBOL



BEHAVIOUR

A	Z
11	

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.2 SL

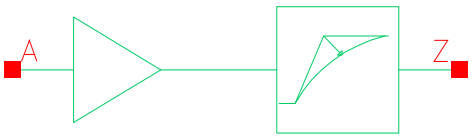
OUTPUT Pin	Max. load
Z	100.000 pF

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF	@maxLoad
A to Z	Fall delay	1.93	2.89	3.86	4.82	4.82
A to Z	Rise delay	1.75	2.43	3.10	3.78	3.78

CMOS035 MTC45100	CMOS Output Pad Buffer, 4mA, with Slew Rate Control	B4CR

SYMBOL



BEHAVIOUR

A	Z
11	

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.2 SL

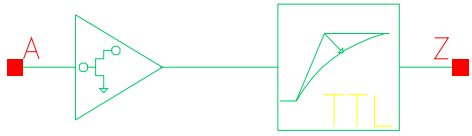
OUTPUT Pin	Max. load
Z	100.000 pF

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF	@maxLoad
A to Z	Fall delay	2.73	3.66	4.53	5.38	5.38
A to Z	Rise delay	2.73	3.61	4.44	5.25	5.25

CMOS035 MTC45100	TTL Open Drain Output Pad Buffer, 4mA, with Slew Rate Control	B4ROD

SYMBOL



BEHAVIOUR

A	Z
0	0
1	Z

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.2 SL
Z	1.651 pF

OUTPUT Pin	Max. load
Z	100.000 pF

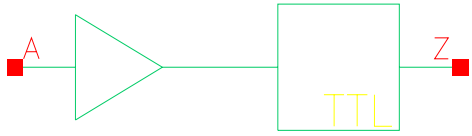
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
A to Z	0Z delay	0.69	0.77	1.02

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF	@maxLoad
A to Z	Z0 delay	2.72	3.79	4.78	5.76	5.76

CMOS035 MTC45100	TTL Output Pad Buffer, 8mA	B8

SYMBOL



BEHAVIOUR

A	Z
11	

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.2 SL

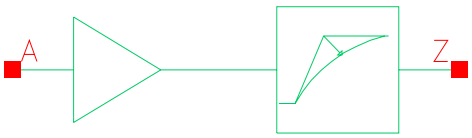
OUTPUT Pin	Max. load
Z	200.000 pF

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF	@maxLoad
A to Z	Fall delay	2.20	3.17	4.13	5.10	5.10
A to Z	Rise delay	2.07	2.76	3.44	4.11	4.11

CMOS035 MTC45100	CMOS Output Pad Buffer, 8mA, with Slew Rate Control	B8CR

SYMBOL



BEHAVIOUR

A	Z
11	

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.2 SL

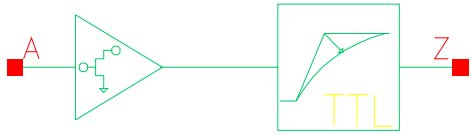
OUTPUT Pin	Max. load
Z	200.000 pF

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF	@maxLoad
A to Z	Fall delay	3.58	4.67	5.62	6.52	6.52
A to Z	Rise delay	3.60	4.63	5.53	6.39	6.39

CMOS035 MTC45100	TTL Open Drain Output Pad Buffer, 8mA, with Slew Rate Control	B8ROD

SYMBOL



BEHAVIOUR

A	Z
0	0
1	Z

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.2 SL
Z	2.161 pF

OUTPUT Pin	Max. load
Z	200.000 pF

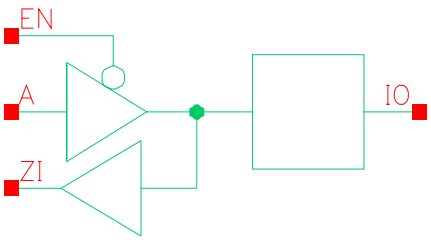
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
A to Z	0Z delay	0.93	1.01	1.26

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF	@maxLoad
A to Z	Z0 delay	3.61	4.83	5.91	6.93	6.93

CMOS035 MTC45100	CMOS Bidir Pad Buffer, 2mA	BD2C

SYMBOL



BEHAVIOUR

A	ENI	OZ	II	O
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	0.9 SL
EN	1.4 SL
IO	2.377 pF

OUTPUT Pin	Max. load
IO	50.000 pF
ZI	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

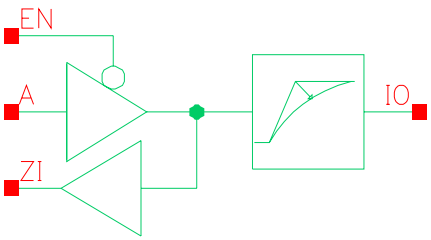
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
IO to ZI	Fall delay	0.23	0.30	0.36	0.47	0.47
IO to ZI	Rise delay	0.27	0.36	0.44	0.61	0.61

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	0.59	0.67	0.93
EN to IO	1Z delay	0.64	0.69	0.87

Timing/Load		12.50pF	25.00pF	37.50pF	50.00pF	@maxLoad
A to IO	Fall delay	2.01	2.85	3.68	4.51	4.51
A to IO	Rise delay	1.88	2.69	3.49	4.30	4.30
EN to IO	Z0 delay	1.66	2.49	3.32	4.15	4.15
EN to IO	Z1 delay	1.86	2.66	3.46	4.27	4.27

CMOS035 MTC45100	CMOS Bidir Pad Buffer, 2mA, with Slew Rate Control	BD2CR

SYMBOL



BEHAVIOUR

A	ENI	OZ	II	O
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	0.9 SL
EN	1.4 SL
IO	2.377 pF

OUTPUT Pin	Max. load
IO	50.000 pF
ZI	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

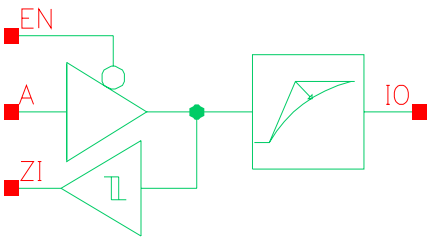
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
IO to ZI	Fall delay	0.23	0.30	0.36	0.47	0.47
IO to ZI	Rise delay	0.27	0.36	0.44	0.61	0.61

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	0.60	0.67	0.93
EN to IO	1Z delay	0.65	0.70	0.88

Timing/Load		12.50pF	25.00pF	37.50pF	50.00pF	@maxLoad
A to IO	Fall delay	2.61	3.47	4.31	5.15	5.15
A to IO	Rise delay	2.38	3.21	4.01	4.82	4.82
EN to IO	Z0 delay	2.25	3.11	3.95	4.79	4.79
EN to IO	Z1 delay	2.35	3.18	3.98	4.79	4.79

CMOS035 MTC45100	CMOS Schmitt Trigger Bidir Pad Buffer, 2mA, with Slew Rate Control	BD2SCR

SYMBOL



BEHAVIOUR

A	ENI	OZ	II	O
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	0.9 SL
EN	1.4 SL
IO	2.381 pF

OUTPUT Pin	Max. load
IO	50.000 pF
ZI	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

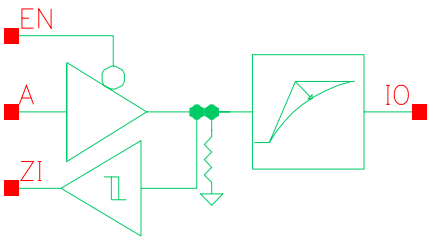
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
IO to ZI	Fall delay	0.56	0.66	0.74	0.87	0.87
IO to ZI	Rise delay	0.52	0.63	0.72	0.89	0.88

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	0.60	0.67	0.93
EN to IO	1Z delay	0.65	0.70	0.88

Timing/Load		12.50pF	25.00pF	37.50pF	50.00pF	@maxLoad
A to IO	Fall delay	2.61	3.48	4.31	5.15	5.15
A to IO	Rise delay	2.38	3.21	4.01	4.82	4.82
EN to IO	Z0 delay	2.25	3.11	3.95	4.79	4.79
EN to IO	Z1 delay	2.35	3.18	3.98	4.79	4.79

CMOS035 MTC45100	CMOS Schmitt Trigger Bidir Pad Buffer with Active Pull-Down, 2mA, with Slew Rate Control	BD2SCRD

SYMBOL



BEHAVIOUR

A	ENI	OZ	II	O
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	0.9 SL
EN	1.4 SL
IO	2.384 pF

OUTPUT Pin	Max. load
IO	50.000 pF
ZI	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

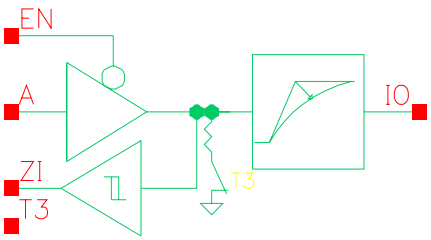
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
IO to ZI	Fall delay	0.57	0.67	0.75	0.88	0.88
IO to ZI	Rise delay	0.53	0.64	0.73	0.90	0.90

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	0.60	0.68	0.94
EN to IO	1Z delay	0.63	0.69	0.87

Timing/Load		12.50pF	25.00pF	37.50pF	50.00pF	@maxLoad
A to IO	Fall delay	2.60	3.46	4.30	5.13	5.13
A to IO	Rise delay	2.39	3.21	4.02	4.83	4.83
EN to IO	Z0 delay	2.23	3.10	3.93	4.76	4.76
EN to IO	Z1 delay	2.36	3.18	3.99	4.80	4.80

CMOS035 MTC45100	CMOS Schmitt Trigger Bidir Pad Buffer with Active Pull-Down, 2mA, with Slew Rate Control	BD2SCRDQ

SYMBOL



BEHAVIOUR

A	ENI	OT	3Z	II	O
-	1	1	-	1	
-	0	-	-	-	
1	0	-	-		1
-	1	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	0.5 SL
EN	1.0 SL
IO	2.392 pF
T3	0.7 SL

OUTPUT Pin	Max. load
IO	50.000 pF
ZI	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

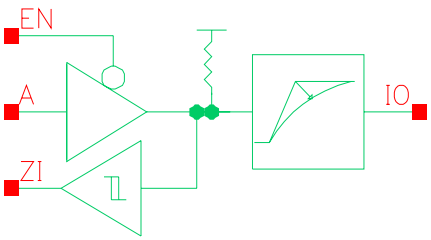
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
IO to ZI	Fall delay	0.56	0.67	0.74	0.87	0.87
IO to ZI	Rise delay	0.53	0.63	0.72	0.89	0.89

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	0.60	0.68	0.94
EN to IO	1Z delay	0.64	0.69	0.87

Timing/Load		12.50pF	25.00pF	37.50pF	50.00pF	@maxLoad
A to IO	Fall delay	2.59	3.46	4.29	5.12	5.12
A to IO	Rise delay	2.39	3.22	4.03	4.83	4.83
EN to IO	Z0 delay	2.23	3.09	3.93	4.76	4.76
EN to IO	Z1 delay	2.38	3.20	4.01	4.82	4.82

CMOS035 MTC45100	CMOS Schmitt Trigger Bidir Pad Buffer with Active Pull-Up, 2mA, with Slew Rate Control	BD2SCRU

SYMBOL



BEHAVIOUR

A	ENI	OZ	II	O
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	0.9 SL
EN	1.4 SL
IO	2.387 pF

OUTPUT Pin	Max. load
IO	50.000 pF
ZI	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

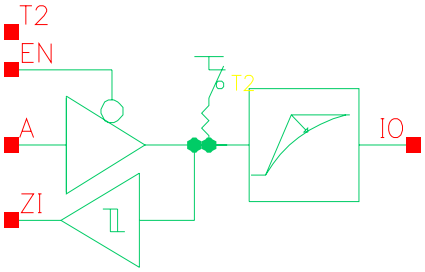
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
IO to ZI	Fall delay	0.58	0.68	0.76	0.89	0.89
IO to ZI	Rise delay	0.54	0.64	0.73	0.90	0.90

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	0.59	0.66	0.93
EN to IO	1Z delay	0.66	0.72	0.90

Timing/Load		12.50pF	25.00pF	37.50pF	50.00pF	@maxLoad
A to IO	Fall delay	2.61	3.48	4.32	5.15	5.15
A to IO	Rise delay	2.38	3.20	4.00	4.80	4.80
EN to IO	Z0 delay	2.25	3.12	3.96	4.79	4.79
EN to IO	Z1 delay	2.34	3.16	3.96	4.77	4.77

CMOS035 MTC45100	CMOS Schmitt Trigger Bidir Pad Buffer with Active Pull-Up, 2mA, with Slew Rate Control	BD2SCRUQ

SYMBOL



BEHAVIOUR

A	ENI	OT	ZZ	II	O
-	1	1	-	1	
-	0	-	-	-	
1	0	-	-		1
-	1	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	0.5 SL
EN	1.0 SL
IO	2.392 pF
T2	0.5 SL

OUTPUT Pin	Max. load
IO	50.000 pF
ZI	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

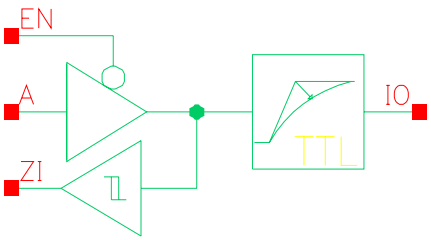
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
IO to ZI	Fall delay	0.56	0.66	0.74	0.87	0.87
IO to ZI	Rise delay	0.52	0.63	0.72	0.88	0.88

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	0.59	0.67	0.93
EN to IO	1Z delay	0.65	0.70	0.88

Timing/Load		12.50pF	25.00pF	37.50pF	50.00pF	@maxLoad
A to IO	Fall delay	2.60	3.47	4.31	5.14	5.14
A to IO	Rise delay	2.39	3.21	4.02	4.83	4.83
EN to IO	Z0 delay	2.24	3.11	3.95	4.78	4.78
EN to IO	Z1 delay	2.38	3.20	4.01	4.82	4.82

CMOS035 MTC45100	TTL Schmitt Trigger Bidir Pad Buffer, 2mA, with Slew Rate Control	BD2STR

SYMBOL



BEHAVIOUR

A	ENI	OZ	II	O
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	0.9 SL
EN	1.4 SL
IO	2.376 pF

OUTPUT Pin	Max. load
IO	50.000 pF
ZI	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

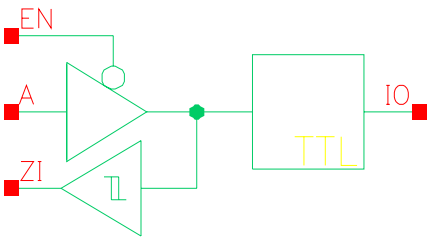
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
IO to ZI	Fall delay	0.50	0.60	0.68	0.81	0.80
IO to ZI	Rise delay	0.44	0.54	0.63	0.80	0.79

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	0.60	0.67	0.94
EN to IO	1Z delay	0.64	0.70	0.88

Timing/Load		12.50pF	25.00pF	37.50pF	50.00pF	@maxLoad
A to IO	Fall delay	2.78	3.77	4.74	5.71	5.71
A to IO	Rise delay	2.22	2.92	3.60	4.27	4.27
EN to IO	Z0 delay	2.42	3.41	4.38	5.35	5.35
EN to IO	Z1 delay	2.19	2.89	3.57	4.24	4.24

CMOS035 MTC45100	TTL Five Volt tolerant Schmitt Trigger Bidir Pad Buffer, 3mA	BD3ST_FT

SYMBOL



BEHAVIOUR

A	ENI	OZ	II	O
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	0.9 SL
EN	1.4 SL
IO	3.224 pF

OUTPUT Pin	Max. load
IO	75.000 pF
ZI	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

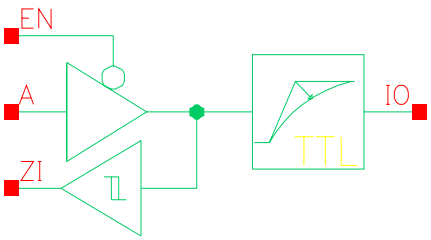
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
IO to ZI	Fall delay	0.90	1.04	1.14	1.31	1.31
IO to ZI	Rise delay	1.05	1.16	1.25	1.42	1.42

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	0.73	0.81	1.07
EN to IO	1Z delay	1.51	1.57	1.75

Timing/Load		18.75pF	37.50pF	56.25pF	75.00pF	@maxLoad
A to IO	Fall delay	2.44	3.53	4.61	5.69	5.69
A to IO	Rise delay	1.94	2.47	2.98	3.50	3.50
EN to IO	Z0 delay	1.98	3.08	4.17	5.26	5.26
EN to IO	Z1 delay	1.94	2.47	2.98	3.50	3.50

CMOS035 MTC45100	TTL Five Volt tolerant Schmitt Trigger Bidir Pad Buffer, 3mA, with Slew Rate Control	BD3STR_FT

SYMBOL



BEHAVIOUR

A	ENI	OZ	II	O
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	0.9 SL
EN	1.4 SL
IO	3.205 pF

OUTPUT Pin	Max. load
IO	75.000 pF
ZI	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

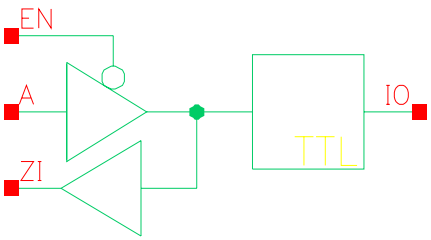
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
IO to ZI	Fall delay	0.90	1.04	1.14	1.31	1.31
IO to ZI	Rise delay	1.05	1.16	1.25	1.42	1.42

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	0.74	0.82	1.08
EN to IO	1Z delay	1.53	1.59	1.77

Timing/Load		18.75pF	37.50pF	56.25pF	75.00pF	@maxLoad
A to IO	Fall delay	3.30	4.44	5.54	6.63	6.63
A to IO	Rise delay	2.77	3.40	3.97	4.51	4.51
EN to IO	Z0 delay	2.90	4.04	5.15	6.25	6.25
EN to IO	Z1 delay	2.77	3.40	3.97	4.51	4.51

CMOS035 MTC45100	TTL Five Volt tolerant Bidir Pad Buffer, 3mA	BD3T_FT

SYMBOL



BEHAVIOUR

A	ENI	OZ	II	O
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	0.9 SL
EN	1.4 SL
IO	3.227 pF

OUTPUT Pin	Max. load
IO	75.000 pF
ZI	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

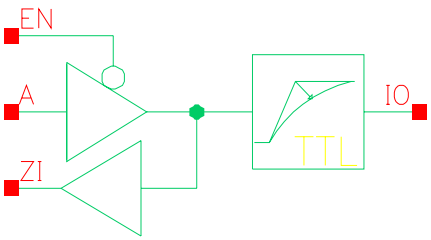
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
IO to ZI	Fall delay	0.39	0.48	0.55	0.67	0.67
IO to ZI	Rise delay	0.47	0.56	0.64	0.81	0.81

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	0.73	0.81	1.07
EN to IO	1Z delay	1.51	1.56	1.75

Timing/Load		18.75pF	37.50pF	56.25pF	75.00pF	@maxLoad
A to IO	Fall delay	2.44	3.53	4.61	5.69	5.69
A to IO	Rise delay	1.94	2.47	2.98	3.50	3.50
EN to IO	Z0 delay	1.98	3.08	4.17	5.27	5.27
EN to IO	Z1 delay	1.94	2.47	2.98	3.50	3.50

CMOS035 MTC45100	TTL Five Volt tolerant Bidir Pad Buffer, 3mA, with Slew Rate Control	BD3TR_FT

SYMBOL



BEHAVIOUR

A	ENI	OZ	II	O
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	0.9 SL
EN	1.4 SL
IO	3.208 pF

OUTPUT Pin	Max. load
IO	75.000 pF
ZI	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

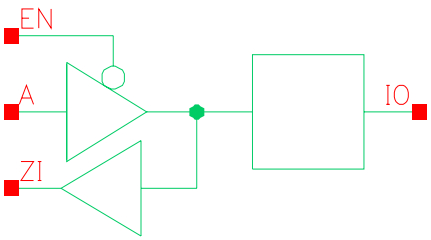
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
IO to ZI	Fall delay	0.39	0.48	0.55	0.67	0.67
IO to ZI	Rise delay	0.47	0.56	0.65	0.81	0.81

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	0.74	0.82	1.08
EN to IO	1Z delay	1.53	1.59	1.77

Timing/Load		18.75pF	37.50pF	56.25pF	75.00pF	@maxLoad
A to IO	Fall delay	3.30	4.44	5.54	6.63	6.63
A to IO	Rise delay	2.77	3.40	3.97	4.51	4.51
EN to IO	Z0 delay	2.90	4.04	5.15	6.25	6.25
EN to IO	Z1 delay	2.77	3.40	3.97	4.51	4.51

CMOS035 MTC45100	CMOS Bidir Pad Buffer, 4mA	BD4C

SYMBOL



BEHAVIOUR

A	ENI	OZ	II	O
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	0.9 SL
EN	1.4 SL
IO	2.924 pF

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

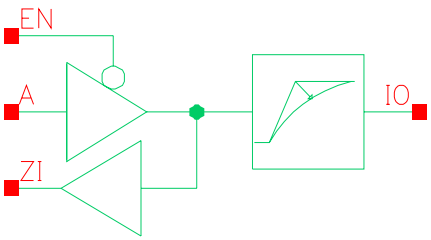
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
IO to ZI	Fall delay	0.23	0.30	0.36	0.47	0.47
IO to ZI	Rise delay	0.27	0.36	0.44	0.61	0.61

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	0.73	0.81	1.07
EN to IO	1Z delay	0.80	0.85	1.04

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF	@maxLoad
A to IO	Fall delay	2.11	2.94	3.77	4.60	4.60
A to IO	Rise delay	2.00	2.81	3.62	4.42	4.42
EN to IO	Z0 delay	1.75	2.58	3.41	4.24	4.24
EN to IO	Z1 delay	1.98	2.78	3.59	4.39	4.39

CMOS035 MTC45100	CMOS Bidir Pad Buffer, 4mA, with Slew Rate Control	BD4CR

SYMBOL



BEHAVIOUR

A	ENI	OZ	II	O
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	0.9 SL
EN	1.4 SL
IO	2.924 pF

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

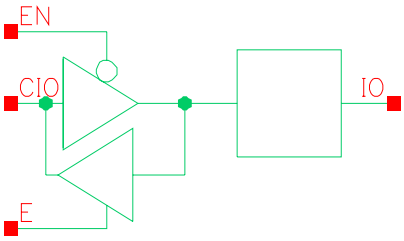
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
IO to ZI	Fall delay	0.23	0.30	0.36	0.47	0.47
IO to ZI	Rise delay	0.27	0.36	0.44	0.61	0.61

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	0.73	0.81	1.07
EN to IO	1Z delay	0.81	0.86	1.05

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF	@maxLoad
A to IO	Fall delay	3.06	3.99	4.86	5.70	5.70
A to IO	Rise delay	2.84	3.72	4.55	5.36	5.36
EN to IO	Z0 delay	2.70	3.64	4.50	5.35	5.35
EN to IO	Z1 delay	2.81	3.69	4.52	5.34	5.34

CMOS035 MTC45100	CMOS Bidir Pad Buffer, 4mA	BD4HZC

SYMBOL



BEHAVIOUR

E	EN	CIO	IO	CIO	IO
1	-	-	1	1	
0	-	-	-	Z	
-	0	1	-		1
-	1	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
CIO	19.4 SL
E	3.9 SL
EN	1.5 SL
IO	2.931 pF

OUTPUT Pin	Max. load
CIO	316 SL
IO	100.000 pF

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

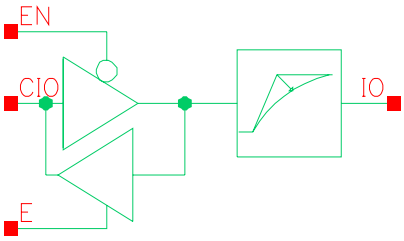
Timing/Load		1.0xSL	80.0xSL	160.0xSL	320.0xSL	@maxLoad
E to CIO	Z0 delay	0.30	0.44	0.52	0.66	0.66
E to CIO	Z1 delay	0.27	0.44	0.55	0.73	0.73
IO to CIO	Fall delay	0.39	0.51	0.59	0.72	0.72
IO to CIO	Rise delay	0.42	0.56	0.67	0.85	0.84

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
E to CIO	0Z delay	0.51	0.56	0.76
E to CIO	1Z delay	0.44	0.50	0.75
EN to IO	0Z delay	0.73	0.81	1.07
EN to IO	1Z delay	0.80	0.86	1.04

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF	@maxLoad
CIO to IO	Fall delay	2.11	2.94	3.77	4.60	4.60
CIO to IO	Rise delay	2.01	2.81	3.62	4.42	4.42
EN to IO	Z0 delay	1.75	2.58	3.41	4.24	4.24
EN to IO	Z1 delay	1.98	2.78	3.59	4.39	4.39

CMOS035 MTC45100	CMOS Bidir Pad Buffer, 4mA, with Slew Rate Control	BD4HZCR

SYMBOL



BEHAVIOUR

E	EN	CIO	IO	CIO	IO
1	-	-	1	1	
0	-	-	-	Z	
-	0	1	-		1
-	1	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
CIO	19.4 SL
E	3.9 SL
EN	1.5 SL
IO	2.931 pF

OUTPUT Pin	Max. load
CIO	316 SL
IO	100.000 pF

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

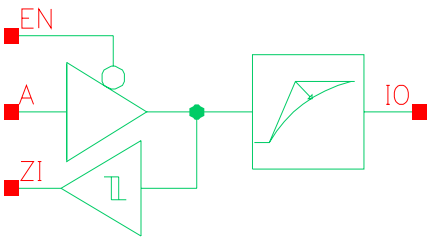
Timing/Load		1.0xSL	80.0xSL	160.0xSL	320.0xSL	@maxLoad
E to CIO	Z0 delay	0.30	0.44	0.52	0.66	0.66
E to CIO	Z1 delay	0.27	0.44	0.55	0.73	0.73
IO to CIO	Fall delay	0.39	0.51	0.59	0.72	0.72
IO to CIO	Rise delay	0.42	0.56	0.67	0.85	0.84

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
E to CIO	0Z delay	0.51	0.56	0.76
E to CIO	1Z delay	0.44	0.50	0.75
EN to IO	0Z delay	0.73	0.81	1.08
EN to IO	1Z delay	0.81	0.87	1.05

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF	@maxLoad
CIO to IO	Fall delay	3.06	4.00	4.86	5.71	5.71
CIO to IO	Rise delay	2.84	3.72	4.55	5.36	5.36
EN to IO	Z0 delay	2.70	3.64	4.51	5.35	5.35
EN to IO	Z1 delay	2.81	3.69	4.52	5.34	5.34

CMOS035 MTC45100	CMOS Schmitt Trigger Bidir Pad Buffer, 4mA, with Slew Rate Control	BD4SCR

SYMBOL



BEHAVIOUR

A	ENI	OZ	II	O
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	0.9 SL
EN	1.4 SL
IO	2.927 pF

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

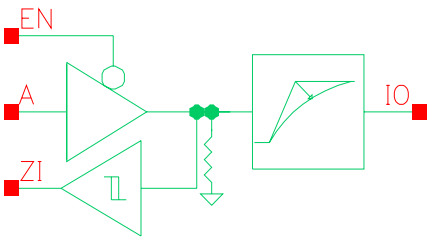
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
IO to ZI	Fall delay	0.56	0.66	0.74	0.87	0.87
IO to ZI	Rise delay	0.52	0.63	0.72	0.89	0.88

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	0.73	0.81	1.07
EN to IO	1Z delay	0.81	0.86	1.05

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF	@maxLoad
A to IO	Fall delay	3.06	3.99	4.86	5.70	5.70
A to IO	Rise delay	2.84	3.72	4.55	5.36	5.36
EN to IO	Z0 delay	2.70	3.64	4.50	5.35	5.35
EN to IO	Z1 delay	2.81	3.69	4.52	5.34	5.34

CMOS035 MTC45100	CMOS Schmitt Trigger Bidir Pad Buffer with Active Pull-Down, 4mA, with Slew Rate Control	BD4SCRD

SYMBOL



BEHAVIOUR

A	ENI	OZ	II	O
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	0.9 SL
EN	1.4 SL
IO	2.931 pF

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

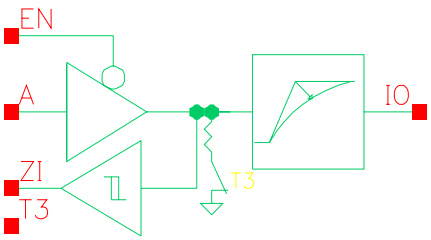
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
IO to ZI	Fall delay	0.57	0.67	0.75	0.88	0.88
IO to ZI	Rise delay	0.53	0.64	0.73	0.90	0.90

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	0.74	0.82	1.08
EN to IO	1Z delay	0.80	0.86	1.04

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF	@maxLoad
A to IO	Fall delay	3.05	3.98	4.85	5.69	5.69
A to IO	Rise delay	2.84	3.72	4.55	5.36	5.36
EN to IO	Z0 delay	2.69	3.63	4.49	5.34	5.34
EN to IO	Z1 delay	2.81	3.70	4.52	5.34	5.34

CMOS035 MTC45100	CMOS Schmitt Trigger Bidir Pad Buffer with Active Pull-Down, 4mA, with Slew Rate Control	BD4SCRDQ

SYMBOL



BEHAVIOUR

A	ENI	OT	3Z	II	O
-	1	1	-	1	
-	0	-	-	-	
1	0	-	-		1
-	1	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	0.5 SL
EN	1.0 SL
IO	2.939 pF
T3	0.7 SL

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

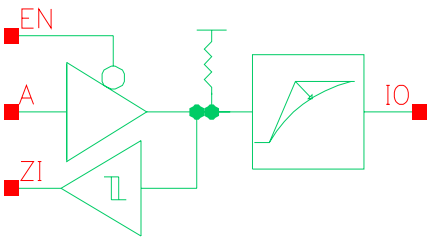
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
IO to ZI	Fall delay	0.56	0.67	0.74	0.87	0.87
IO to ZI	Rise delay	0.53	0.63	0.72	0.89	0.89

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	0.74	0.82	1.08
EN to IO	1Z delay	0.80	0.86	1.04

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF	@maxLoad
A to IO	Fall delay	3.04	3.97	4.84	5.68	5.68
A to IO	Rise delay	2.84	3.72	4.55	5.37	5.37
EN to IO	Z0 delay	2.68	3.62	4.48	5.33	5.33
EN to IO	Z1 delay	2.83	3.71	4.55	5.36	5.36

CMOS035 MTC45100	CMOS Schmitt Trigger Bidir Pad Buffer with Active Pull-Up, 4mA, with Slew Rate Control	BD4SCRU

SYMBOL



BEHAVIOUR

A	ENI	OZ	II	O
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	0.9 SL
EN	1.4 SL
IO	2.934 pF

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

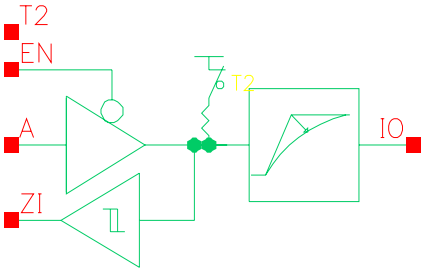
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
IO to ZI	Fall delay	0.58	0.68	0.76	0.89	0.89
IO to ZI	Rise delay	0.54	0.64	0.73	0.90	0.90

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	0.73	0.80	1.07
EN to IO	1Z delay	0.82	0.88	1.06

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF	@maxLoad
A to IO	Fall delay	3.06	3.99	4.86	5.71	5.71
A to IO	Rise delay	2.83	3.71	4.54	5.35	5.35
EN to IO	Z0 delay	2.70	3.64	4.51	5.35	5.35
EN to IO	Z1 delay	2.80	3.68	4.51	5.32	5.32

CMOS035 MTC45100	CMOS Schmitt Trigger Bidir Pad Buffer with Active Pull-Up, 4mA, with Slew Rate Control	BD4SCRUQ

SYMBOL



BEHAVIOUR

A	ENI	OT	ZZ	II	O
-	1	1	-	1	
-	0	-	-	-	
1	0	-	-		1
-	1	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	0.5 SL
EN	1.0 SL
IO	2.939 pF
T2	0.5 SL

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

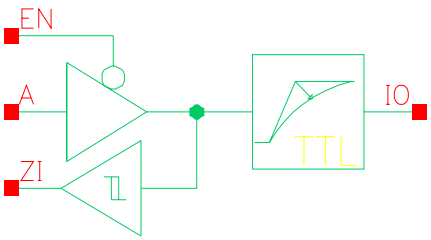
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
IO to ZI	Fall delay	0.56	0.66	0.74	0.87	0.87
IO to ZI	Rise delay	0.52	0.63	0.72	0.88	0.88

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	0.73	0.81	1.07
EN to IO	1Z delay	0.81	0.87	1.05

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF	@maxLoad
A to IO	Fall delay	3.04	3.98	4.84	5.69	5.69
A to IO	Rise delay	2.84	3.72	4.55	5.37	5.37
EN to IO	Z0 delay	2.69	3.63	4.50	5.34	5.34
EN to IO	Z1 delay	2.83	3.71	4.54	5.36	5.36

CMOS035 MTC45100	TTL Schmitt Trigger Bidir Pad Buffer, 4mA, with Slew Rate Control	BD4STR

SYMBOL



BEHAVIOUR

A	ENI	OZ	II	O
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	0.9 SL
EN	1.4 SL
IO	2.912 pF

OUTPUT Pin	Max. load
IO	100.000 pF
ZI	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

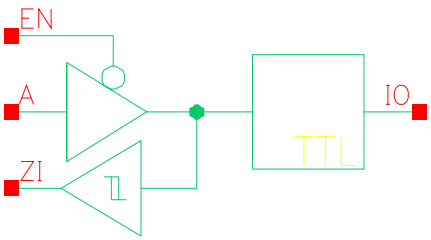
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
IO to ZI	Fall delay	0.50	0.60	0.68	0.81	0.80
IO to ZI	Rise delay	0.44	0.54	0.63	0.80	0.79

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	0.74	0.82	1.08
EN to IO	1Z delay	0.80	0.86	1.04

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF	@maxLoad
A to IO	Fall delay	3.23	4.29	5.29	6.26	6.26
A to IO	Rise delay	2.66	3.43	4.13	4.82	4.82
EN to IO	Z0 delay	2.88	3.94	4.93	5.91	5.91
EN to IO	Z1 delay	2.64	3.40	4.10	4.79	4.79

CMOS035 MTC45100	TTL Five Volt tolerant Schmitt Trigger Bidir Pad Buffer, 6mA	BD6ST_FT

SYMBOL



BEHAVIOUR

A	ENI	OZ	II	O
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	0.9 SL
EN	1.4 SL
IO	4.699 pF

OUTPUT Pin	Max. load
IO	150.000 pF
ZI	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

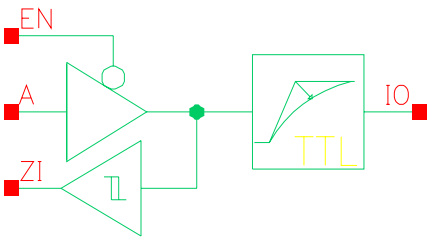
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
IO to ZI	Fall delay	0.90	1.03	1.14	1.31	1.31
IO to ZI	Rise delay	1.05	1.16	1.25	1.42	1.41

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	0.96	1.03	1.30
EN to IO	1Z delay	2.38	2.43	2.61

Timing/Load		37.50pF	75.00pF	112.50pF	150.00pF	@maxLoad
A to IO	Fall delay	2.65	3.77	4.87	5.95	5.95
A to IO	Rise delay	2.29	2.86	3.39	3.91	3.91
EN to IO	Z0 delay	2.09	3.22	4.33	5.43	5.43
EN to IO	Z1 delay	2.29	2.86	3.39	3.91	3.91

CMOS035 MTC45100	TTL Five Volt tolerant Schmitt Trigger Bidir Pad Buffer, 6mA, with Slew Rate Control	BD6STR_FT

SYMBOL



BEHAVIOUR

A	ENI	OZ	II	O
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	0.9 SL
EN	1.4 SL
IO	4.682 pF

OUTPUT Pin	Max. load
IO	150.000 pF
ZI	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

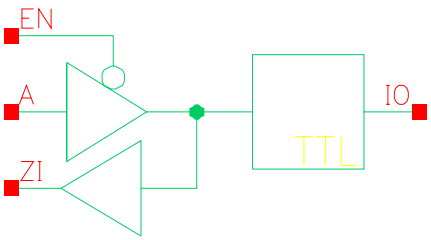
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
IO to ZI	Fall delay	0.90	1.04	1.14	1.31	1.31
IO to ZI	Rise delay	1.05	1.16	1.25	1.42	1.42

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	0.96	1.04	1.30
EN to IO	1Z delay	2.40	2.46	2.64

Timing/Load		37.50pF	75.00pF	112.50pF	150.00pF	@maxLoad
A to IO	Fall delay	4.24	5.46	6.62	7.73	7.73
A to IO	Rise delay	3.48	4.26	4.91	5.51	5.51
EN to IO	Z0 delay	3.80	5.04	6.20	7.32	7.32
EN to IO	Z1 delay	3.49	4.26	4.91	5.51	5.51

CMOS035 MTC45100	TTL Five Volt tolerant Bidir Pad Buffer, 6mA	BD6T_FT

SYMBOL



BEHAVIOUR

A	ENI	OZ	II	O
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	0.9 SL
EN	1.4 SL
IO	4.703 pF

OUTPUT Pin	Max. load
IO	150.000 pF
ZI	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

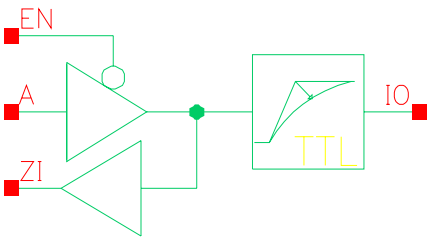
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
IO to ZI	Fall delay	0.39	0.48	0.55	0.67	0.67
IO to ZI	Rise delay	0.46	0.56	0.64	0.81	0.81

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	0.96	1.03	1.30
EN to IO	1Z delay	2.38	2.43	2.61

Timing/Load		37.50pF	75.00pF	112.50pF	150.00pF	@maxLoad
A to IO	Fall delay	2.65	3.77	4.87	5.95	5.95
A to IO	Rise delay	2.29	2.86	3.39	3.91	3.91
EN to IO	Z0 delay	2.09	3.22	4.33	5.43	5.43
EN to IO	Z1 delay	2.29	2.86	3.39	3.91	3.91

CMOS035 MTC45100	TTL Five Volt tolerant Bidir Pad Buffer, 6mA, with Slew Rate Control	BD6TR_FT

SYMBOL



BEHAVIOUR

A	ENI	OZ	II	O
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	0.9 SL
EN	1.4 SL
IO	4.686 pF

OUTPUT Pin	Max. load
IO	150.000 pF
ZI	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

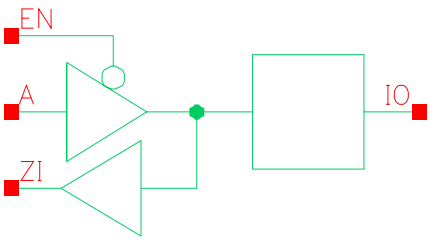
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
IO to ZI	Fall delay	0.39	0.48	0.55	0.67	0.67
IO to ZI	Rise delay	0.46	0.56	0.64	0.81	0.81

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	0.96	1.04	1.30
EN to IO	1Z delay	2.40	2.46	2.64

Timing/Load		37.50pF	75.00pF	112.50pF	150.00pF	@maxLoad
A to IO	Fall delay	4.24	5.46	6.62	7.73	7.73
A to IO	Rise delay	3.48	4.26	4.91	5.51	5.51
EN to IO	Z0 delay	3.80	5.04	6.20	7.32	7.32
EN to IO	Z1 delay	3.49	4.26	4.91	5.51	5.51

CMOS035 MTC45100	CMOS Bidir Pad Buffer, 8mA	BD8C

SYMBOL



BEHAVIOUR

A	ENI	OZ	II	O
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	0.9 SL
EN	1.4 SL
IO	3.991 pF

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

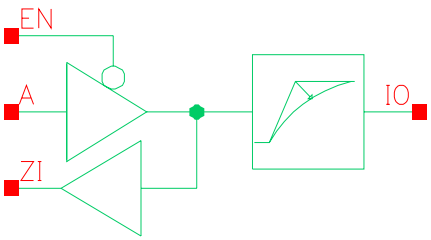
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
IO to ZI	Fall delay	0.23	0.30	0.36	0.47	0.47
IO to ZI	Rise delay	0.27	0.36	0.44	0.61	0.61

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	0.96	1.04	1.30
EN to IO	1Z delay	1.08	1.14	1.32

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF	@maxLoad
A to IO	Fall delay	2.37	3.21	4.04	4.87	4.87
A to IO	Rise delay	2.32	3.14	3.95	4.75	4.75
EN to IO	Z0 delay	2.01	2.85	3.68	4.51	4.51
EN to IO	Z1 delay	2.30	3.11	3.92	4.73	4.73

CMOS035 MTC45100	CMOS Bidir Pad Buffer, 8mA, with Slew Rate Control	BD8CR

SYMBOL



BEHAVIOUR

A	ENI	OZ	II	O
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	0.9 SL
EN	1.4 SL
IO	3.991 pF

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

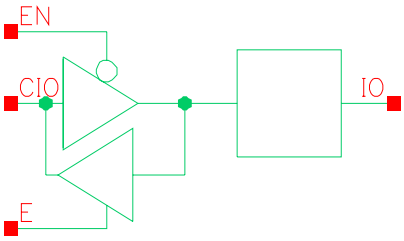
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
IO to ZI	Fall delay	0.23	0.30	0.36	0.47	0.47
IO to ZI	Rise delay	0.27	0.36	0.44	0.61	0.61

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	0.97	1.04	1.31
EN to IO	1Z delay	1.09	1.15	1.33

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF	@maxLoad
A to IO	Fall delay	3.90	4.99	5.94	6.83	6.83
A to IO	Rise delay	3.70	4.73	5.64	6.50	6.50
EN to IO	Z0 delay	3.55	4.64	5.59	6.49	6.49
EN to IO	Z1 delay	3.68	4.71	5.62	6.47	6.47

CMOS035 MTC45100	CMOS Bidir Pad Buffer, 8mA	BD8HZC

SYMBOL



BEHAVIOUR

E	EN	CIO	IO	CIO	IO
1	-	-	1	1	
0	-	-	-	Z	
-	0	1	-		1
-	1	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
CIO	19.4 SL
E	3.9 SL
EN	1.5 SL
IO	3.998 pF

OUTPUT Pin	Max. load
CIO	316 SL
IO	200.000 pF

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

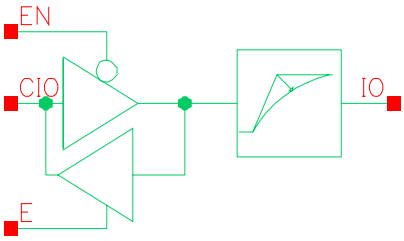
Timing/Load		1.0xSL	80.0xSL	160.0xSL	320.0xSL	@maxLoad
E to CIO	Z0 delay	0.30	0.44	0.52	0.66	0.66
E to CIO	Z1 delay	0.27	0.44	0.55	0.73	0.73
IO to CIO	Fall delay	0.39	0.51	0.59	0.72	0.72
IO to CIO	Rise delay	0.42	0.56	0.67	0.85	0.84

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
E to CIO	0Z delay	0.51	0.56	0.76
E to CIO	1Z delay	0.44	0.50	0.75
EN to IO	0Z delay	0.96	1.04	1.30
EN to IO	1Z delay	1.08	1.14	1.32

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF	@maxLoad
CIO to IO	Fall delay	2.37	3.21	4.05	4.88	4.88
CIO to IO	Rise delay	2.33	3.14	3.95	4.76	4.76
EN to IO	Z0 delay	2.01	2.85	3.68	4.51	4.51
EN to IO	Z1 delay	2.30	3.12	3.92	4.73	4.73

CMOS035 MTC45100	CMOS Bidir Pad Buffer, 8mA, with Slew Rate Control	BD8HZCR

SYMBOL



BEHAVIOUR

E	EN	CIO	IO	CIO	IO
1	-	-	1	1	
0	-	-	-	Z	
-	0	1	-		1
-	1	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
CIO	19.4 SL
E	3.9 SL
EN	1.5 SL
IO	3.998 pF

OUTPUT Pin	Max. load
CIO	316 SL
IO	200.000 pF

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

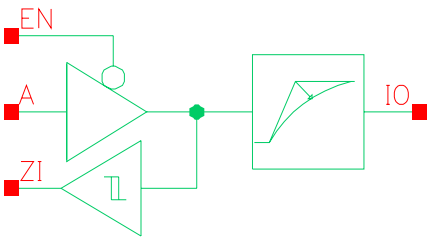
Timing/Load		1.0xSL	80.0xSL	160.0xSL	320.0xSL	@maxLoad
E to CIO	Z0 delay	0.30	0.44	0.52	0.66	0.66
E to CIO	Z1 delay	0.27	0.44	0.55	0.73	0.73
IO to CIO	Fall delay	0.39	0.51	0.59	0.72	0.72
IO to CIO	Rise delay	0.42	0.56	0.67	0.85	0.84

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
E to CIO	0Z delay	0.51	0.56	0.76
E to CIO	1Z delay	0.44	0.50	0.75
EN to IO	0Z delay	0.97	1.04	1.31
EN to IO	1Z delay	1.09	1.15	1.33

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF	@maxLoad
CIO to IO	Fall delay	3.90	4.99	5.94	6.84	6.84
CIO to IO	Rise delay	3.71	4.74	5.64	6.50	6.50
EN to IO	Z0 delay	3.55	4.64	5.59	6.49	6.49
EN to IO	Z1 delay	3.68	4.71	5.62	6.47	6.47

CMOS035 MTC45100	CMOS Schmitt Trigger Bidir Pad Buffer, 8mA, with Slew Rate Control	BD8SCR

SYMBOL



BEHAVIOUR

A	ENI	OZ	II	O
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	0.9 SL
EN	1.4 SL
IO	3.994 pF

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

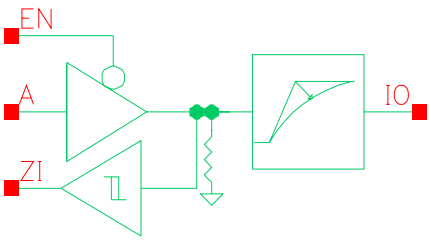
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
IO to ZI	Fall delay	0.56	0.66	0.74	0.87	0.87
IO to ZI	Rise delay	0.52	0.63	0.72	0.89	0.88

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	0.97	1.04	1.31
EN to IO	1Z delay	1.09	1.15	1.33

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF	@maxLoad
A to IO	Fall delay	3.90	4.99	5.94	6.83	6.83
A to IO	Rise delay	3.70	4.73	5.64	6.50	6.50
EN to IO	Z0 delay	3.55	4.64	5.59	6.49	6.49
EN to IO	Z1 delay	3.68	4.71	5.62	6.47	6.47

CMOS035 MTC45100	CMOS Schmitt Trigger Bidir Pad Buffer with Active Pull-Down, 8mA, with Slew Rate Control	BD8SCRD

SYMBOL



BEHAVIOUR

A	ENI	OZ	II	O
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	0.9 SL
EN	1.4 SL
IO	3.998 pF

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

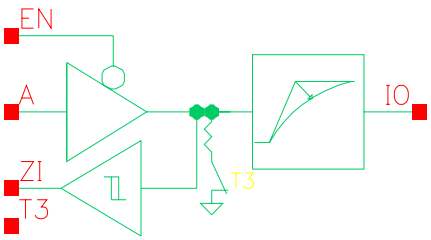
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
IO to ZI	Fall delay	0.57	0.67	0.75	0.88	0.88
IO to ZI	Rise delay	0.53	0.64	0.73	0.90	0.90

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	0.98	1.05	1.32
EN to IO	1Z delay	1.08	1.13	1.31

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF	@maxLoad
A to IO	Fall delay	3.89	4.98	5.93	6.83	6.83
A to IO	Rise delay	3.71	4.74	5.64	6.50	6.50
EN to IO	Z0 delay	3.54	4.63	5.58	6.48	6.48
EN to IO	Z1 delay	3.68	4.71	5.62	6.47	6.47

CMOS035 MTC45100	CMOS Schmitt Trigger Bidir Pad Buffer with Active Pull-Down, 8mA, with Slew Rate Control	BD8SCRDQ

SYMBOL



BEHAVIOUR

A	ENI	OT	3Z	II	O
-	1	1	-	1	
-	0	-	-	-	
1	0	-	-		1
-	1	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	0.5 SL
EN	1.0 SL
IO	4.007 pF
T3	0.7 SL

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

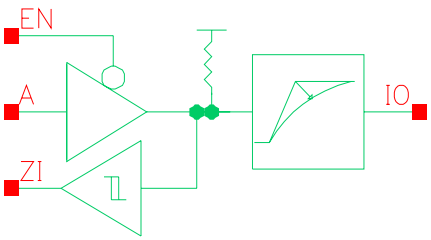
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
IO to ZI	Fall delay	0.56	0.67	0.74	0.87	0.87
IO to ZI	Rise delay	0.53	0.63	0.72	0.89	0.89

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	0.97	1.05	1.31
EN to IO	1Z delay	1.08	1.13	1.31

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF	@maxLoad
A to IO	Fall delay	3.87	4.96	5.91	6.81	6.81
A to IO	Rise delay	3.70	4.73	5.64	6.50	6.50
EN to IO	Z0 delay	3.52	4.61	5.57	6.46	6.46
EN to IO	Z1 delay	3.69	4.72	5.63	6.49	6.49

CMOS035 MTC45100	CMOS Schmitt Trigger Bidir Pad Buffer with Active Pull-Up, 8mA, with Slew Rate Control	BD8SCRU

SYMBOL



BEHAVIOUR

A	ENI	OZ	II	O
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	0.9 SL
EN	1.4 SL
IO	4.001 pF

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

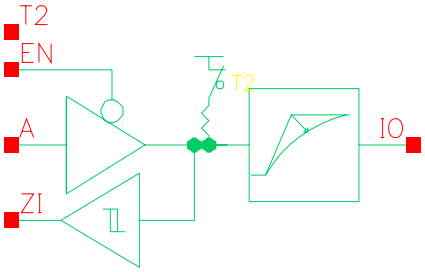
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
IO to ZI	Fall delay	0.58	0.68	0.76	0.89	0.89
IO to ZI	Rise delay	0.54	0.64	0.73	0.90	0.90

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	0.96	1.04	1.30
EN to IO	1Z delay	1.10	1.16	1.34

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF	@maxLoad
A to IO	Fall delay	3.90	4.99	5.94	6.84	6.84
A to IO	Rise delay	3.70	4.73	5.64	6.49	6.49
EN to IO	Z0 delay	3.55	4.64	5.59	6.49	6.49
EN to IO	Z1 delay	3.67	4.70	5.61	6.47	6.47

CMOS035 MTC45100	CMOS Schmitt Trigger Bidir Pad Buffer with Active Pull-Up, 8mA, with Slew Rate Control	BD8SCRUQ

SYMBOL



BEHAVIOUR

A	ENI	OT	ZZ	II	O
-	1	1	-	1	
-	0	-	-	-	
1	0	-	-		1
-	1	-	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	0.5 SL
EN	1.0 SL
IO	4.007 pF
T2	0.5 SL

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

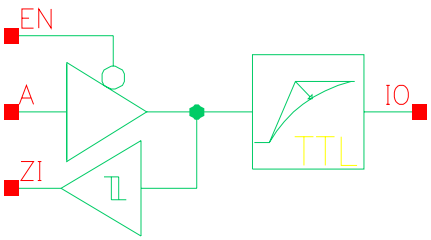
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
IO to ZI	Fall delay	0.56	0.66	0.74	0.87	0.87
IO to ZI	Rise delay	0.52	0.63	0.72	0.88	0.88

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	0.96	1.04	1.30
EN to IO	1Z delay	1.09	1.15	1.32

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF	@maxLoad
A to IO	Fall delay	3.88	4.97	5.92	6.81	6.81
A to IO	Rise delay	3.70	4.73	5.63	6.49	6.49
EN to IO	Z0 delay	3.53	4.62	5.57	6.47	6.47
EN to IO	Z1 delay	3.69	4.72	5.63	6.49	6.49

CMOS035 MTC45100	TTL Schmitt Trigger Bidir Pad Buffer, 8mA, with Slew Rate Control	BD8STR

SYMBOL



BEHAVIOUR

A	ENI	OZ	II	O
-	1	1	1	
-	0	-	-	
1	0	-		1
-	1	-		Z

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	0.9 SL
EN	1.4 SL
IO	3.958 pF

OUTPUT Pin	Max. load
IO	200.000 pF
ZI	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

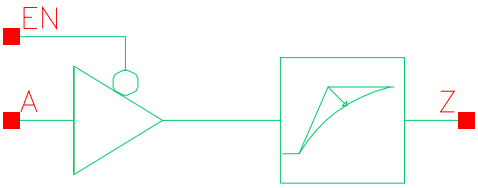
Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
IO to ZI	Fall delay	0.50	0.60	0.68	0.81	0.80
IO to ZI	Rise delay	0.44	0.54	0.63	0.80	0.79

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to IO	0Z delay	0.98	1.05	1.32
EN to IO	1Z delay	1.07	1.13	1.31

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF	@maxLoad
A to IO	Fall delay	4.10	5.32	6.39	7.41	7.41
A to IO	Rise delay	3.49	4.41	5.19	5.93	5.93
EN to IO	Z0 delay	3.75	4.97	6.04	7.06	7.06
EN to IO	Z1 delay	3.47	4.38	5.17	5.91	5.91

CMOS035 MTC45100	CMOS Tristate Output Pad Buffer, 2mA, with Slew Rate Control	BT2CR

SYMBOL



BEHAVIOUR

EN	A	Z
1	-	Z
0	1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	0.9 SL
EN	1.4 SL
Z	2.249 pF

OUTPUT Pin	Max. load
Z	50.000 pF

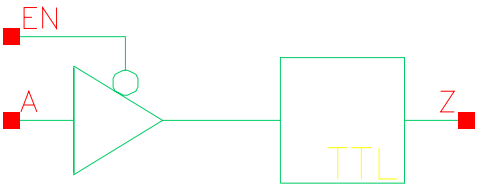
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to Z	0Z delay	0.60	0.67	0.93
EN to Z	1Z delay	0.65	0.70	0.88

Timing/Load		12.50pF	25.00pF	37.50pF	50.00pF	@maxLoad
A to Z	Fall delay	2.60	3.47	4.30	5.14	5.14
A to Z	Rise delay	2.38	3.20	4.01	4.81	4.81
EN to Z	Z0 delay	2.24	3.11	3.94	4.78	4.78
EN to Z	Z1 delay	2.35	3.17	3.98	4.78	4.78

CMOS035 MTC45100	TTL Five Volt tolerant Tristate Output Pad Buffer, 3mA	BT3_FT

SYMBOL



BEHAVIOUR

EN	A	Z
1	-	Z
0	1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	0.9 SL
EN	1.4 SL
Z	3.197 pF

OUTPUT Pin	Max. load
Z	75.000 pF

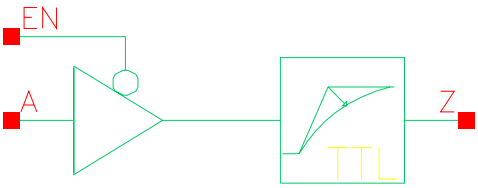
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to Z	0Z delay	0.73	0.81	1.07
EN to Z	1Z delay	1.51	1.57	1.75

Timing/Load		18.75pF	37.50pF	56.25pF	75.00pF	@maxLoad
A to Z	Fall delay	2.43	3.52	4.60	5.69	5.69
A to Z	Rise delay	1.93	2.46	2.98	3.49	3.49
EN to Z	Z0 delay	1.97	3.08	4.17	5.26	5.26
EN to Z	Z1 delay	1.94	2.46	2.98	3.49	3.49

CMOS035 MTC45100	TTL Five Volt tolerant Tristate Output Pad Buffer, 3mA, with Slew Rate Control	BT3R_FT

SYMBOL



BEHAVIOUR

EN	A	Z
1	-	Z
0	1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	0.9 SL
EN	1.4 SL
Z	3.178 pF

OUTPUT Pin	Max. load
Z	75.000 pF

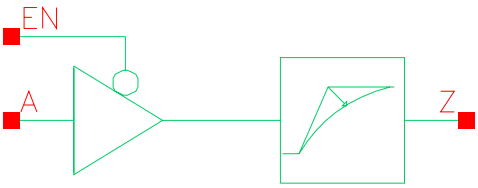
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to Z	0Z delay	0.74	0.82	1.08
EN to Z	1Z delay	1.53	1.58	1.77

Timing/Load		18.75pF	37.50pF	56.25pF	75.00pF	@maxLoad
A to Z	Fall delay	3.29	4.43	5.53	6.63	6.63
A to Z	Rise delay	2.76	3.40	3.97	4.51	4.51
EN to Z	Z0 delay	2.89	4.04	5.14	6.24	6.24
EN to Z	Z1 delay	2.77	3.40	3.97	4.51	4.51

CMOS035 MTC45100	CMOS Tristate Output Pad Buffer, 4mA, with Slew Rate Control	BT4CR

SYMBOL



BEHAVIOUR

EN	A	Z
1	-	Z
0	1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	0.9 SL
EN	1.4 SL
Z	2.796 pF

OUTPUT Pin	Max. load
Z	100.000 pF

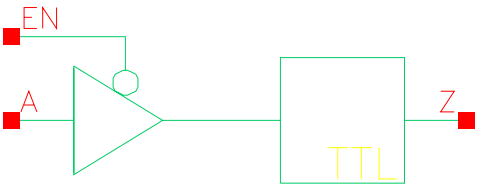
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to Z	0Z delay	0.73	0.81	1.07
EN to Z	1Z delay	0.81	0.86	1.05

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF	@maxLoad
A to Z	Fall delay	3.05	3.99	4.85	5.70	5.70
A to Z	Rise delay	2.83	3.72	4.54	5.36	5.36
EN to Z	Z0 delay	2.70	3.63	4.50	5.34	5.34
EN to Z	Z1 delay	2.81	3.69	4.52	5.33	5.33

CMOS035 MTC45100	TTL Five Volt tolerant Tristate Output Pad Buffer, 6mA	BT6_FT

SYMBOL



BEHAVIOUR

EN	A	Z
1	-	Z
0	1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	0.9 SL
EN	1.4 SL
Z	4.672 pF

OUTPUT Pin	Max. load
Z	150.000 pF

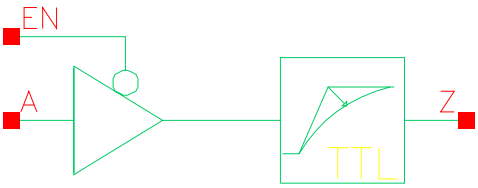
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to Z	0Z delay	0.96	1.03	1.30
EN to Z	1Z delay	2.38	2.43	2.61

Timing/Load		37.50pF	75.00pF	112.50pF	150.00pF	@maxLoad
A to Z	Fall delay	2.65	3.77	4.86	5.95	5.95
A to Z	Rise delay	2.29	2.86	3.39	3.91	3.91
EN to Z	Z0 delay	2.09	3.22	4.32	5.42	5.42
EN to Z	Z1 delay	2.29	2.86	3.39	3.91	3.91

CMOS035 MTC45100	TTL Five Volt tolerant Tristate Output Pad Buffer, 6mA, with Slew Rate Control	BT6R_FT

SYMBOL



BEHAVIOUR

EN	A	Z
1	-	Z
0	1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	0.9 SL
EN	1.4 SL
Z	4.655 pF

OUTPUT Pin	Max. load
Z	150.000 pF

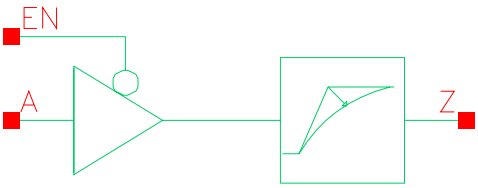
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to Z	0Z delay	0.96	1.04	1.30
EN to Z	1Z delay	2.40	2.46	2.64

Timing/Load		37.50pF	75.00pF	112.50pF	150.00pF	@maxLoad
A to Z	Fall delay	4.23	5.46	6.61	7.72	7.72
A to Z	Rise delay	3.48	4.26	4.91	5.51	5.51
EN to Z	Z0 delay	3.80	5.03	6.19	7.31	7.31
EN to Z	Z1 delay	3.49	4.26	4.91	5.51	5.51

CMOS035 MTC45100	CMOS Tristate Output Pad Buffer, 8mA, with Slew Rate Control	BT8CR

SYMBOL



BEHAVIOUR

EN	A	Z
1	-	Z
0	1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	0.9 SL
EN	1.4 SL
Z	3.886 pF

OUTPUT Pin	Max. load
Z	200.000 pF

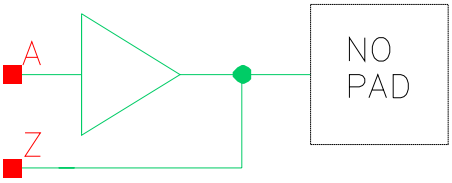
TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Slope		0.4xSS	1.0xSS	4.0xSS
EN to Z	0Z delay	0.97	1.04	1.31
EN to Z	1Z delay	1.09	1.15	1.33

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF	@maxLoad
A to Z	Fall delay	3.89	4.99	5.94	6.83	6.83
A to Z	Rise delay	3.70	4.73	5.64	6.49	6.49
EN to Z	Z0 delay	3.54	4.64	5.59	6.48	6.48
EN to Z	Z1 delay	3.68	4.71	5.61	6.47	6.47

CMOS035 MTC45100	Peripheral Buffer, 4mA	BUF4

SYMBOL



BEHAVIOUR

A	Z
11	

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.2 SL

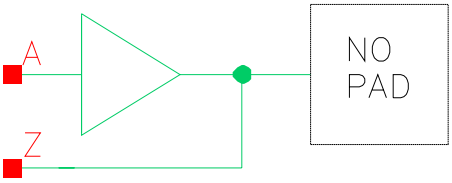
OUTPUT Pin	Max. load
Z	100.000 pF

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		25.00pF	50.00pF	75.00pF	100.00pF	@maxLoad
A to Z	Fall delay	1.54	2.20	2.86	3.53	3.53
A to Z	Rise delay	1.65	2.29	2.92	3.56	3.56

CMOS035 MTC45100	Peripheral Buffer, 8mA	BUF8

SYMBOL



BEHAVIOUR

A	Z
11	

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.2 SL

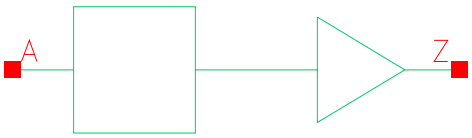
OUTPUT Pin	Max. load
Z	200.000 pF

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		50.00pF	100.00pF	150.00pF	200.00pF	@maxLoad
A to Z	Fall delay	1.81	2.48	3.15	3.81	3.81
A to Z	Rise delay	1.97	2.63	3.26	3.90	3.90

CMOS035 MTC45100	CMOS Input Pad Buffer	IBUF

SYMBOL



BEHAVIOUR

A	Z
11	

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.816 pF

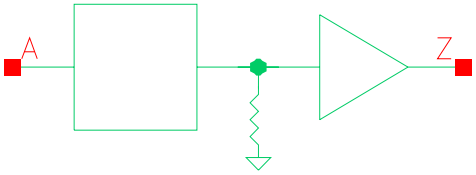
OUTPUT Pin	Max. load
Z	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
A to Z	Fall delay	0.23	0.30	0.36	0.47	0.47
A to Z	Rise delay	0.27	0.36	0.44	0.61	0.61

CMOS035 MTC45100	CMOS Input Pad Buffer with Active Pull-Down	IBUFD

SYMBOL



BEHAVIOUR

A	Z
11	

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.820 pF

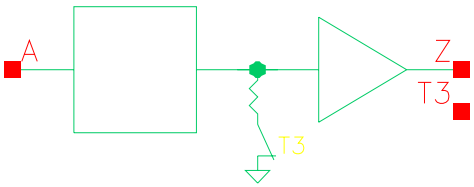
OUTPUT Pin	Max. load
Z	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
A to Z	Fall delay	0.23	0.30	0.36	0.47	0.47
A to Z	Rise delay	0.28	0.37	0.45	0.62	0.61

CMOS035 MTC45100	CMOS Input Pad Buffer with Active Pull-Down	IBUFDQ

SYMBOL



BEHAVIOUR

A	T3Z	
1	-	1

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.828 pF
T3	0.7 SL

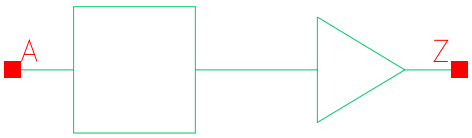
OUTPUT Pin	Max. load
Z	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
A to Z	Fall delay	0.23	0.30	0.36	0.47	0.47
A to Z	Rise delay	0.28	0.36	0.45	0.61	0.61

CMOS035 MTC45100	CMOS Input Pad Buffer	IBUFH

SYMBOL



BEHAVIOUR

A	Z
11	

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.815 pF

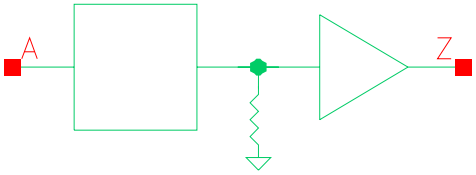
OUTPUT Pin	Max. load
Z	316 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	80.0xSL	160.0xSL	320.0xSL	@maxLoad
A to Z	Fall delay	0.39	0.49	0.56	0.69	0.69
A to Z	Rise delay	0.48	0.60	0.69	0.86	0.86

CMOS035 MTC45100	CMOS Input Pad Buffer with Active Pull-Down	IBUFHD

SYMBOL



BEHAVIOUR

A	Z
11	

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.819 pF

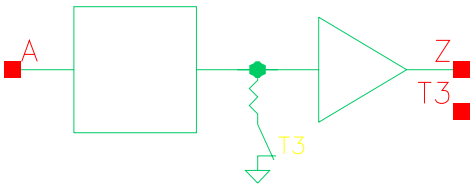
OUTPUT Pin	Max. load
Z	316 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	80.0xSL	160.0xSL	320.0xSL	@maxLoad
A to Z	Fall delay	0.39	0.49	0.57	0.69	0.69
A to Z	Rise delay	0.49	0.61	0.70	0.87	0.87

CMOS035 MTC45100	CMOS Input Pad Buffer with Active Pull-Down	IBUFHDQ

SYMBOL



BEHAVIOUR

A	T3Z	
1	-	1

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.827 pF
T3	0.7 SL

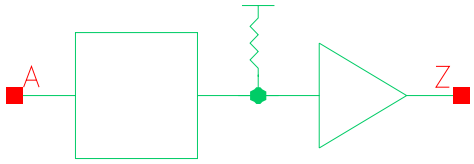
OUTPUT Pin	Max. load
Z	316 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	80.0xSL	160.0xSL	320.0xSL	@maxLoad
A to Z	Fall delay	0.38	0.49	0.56	0.69	0.68
A to Z	Rise delay	0.49	0.60	0.69	0.87	0.86

CMOS035 MTC45100	CMOS Input Pad Buffer with Active Pull-Up	IBUFHU

SYMBOL



BEHAVIOUR

A	Z
11	

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.822 pF

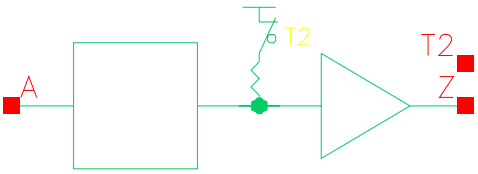
OUTPUT Pin	Max. load
Z	316 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	80.0xSL	160.0xSL	320.0xSL	@maxLoad
A to Z	Fall delay	0.40	0.50	0.58	0.71	0.70
A to Z	Rise delay	0.49	0.61	0.70	0.87	0.86

CMOS035 MTC45100	CMOS Input Pad Buffer with Active Pull-Up	IBUFHUQ

SYMBOL



BEHAVIOUR

A	T2	Z
1	-	1

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.827 pF
T2	0.5 SL

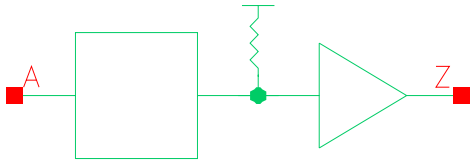
OUTPUT Pin	Max. load
Z	316 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	80.0xSL	160.0xSL	320.0xSL	@maxLoad
A to Z	Fall delay	0.38	0.49	0.56	0.69	0.68
A to Z	Rise delay	0.48	0.60	0.69	0.86	0.85

CMOS035 MTC45100	CMOS Input Pad Buffer with Active Pull-Up	IBUFU

SYMBOL



BEHAVIOUR

A	Z
11	

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.823 pF

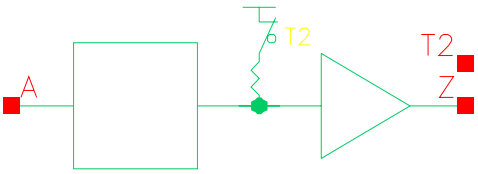
OUTPUT Pin	Max. load
Z	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
A to Z	Fall delay	0.24	0.32	0.38	0.49	0.49
A to Z	Rise delay	0.27	0.36	0.45	0.61	0.61

CMOS035 MTC45100	CMOS Input Pad Buffer with Active Pull-Up	IBUFUQ

SYMBOL



BEHAVIOUR

A	T2	Z
1	-	1

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.828 pF
T2	0.5 SL

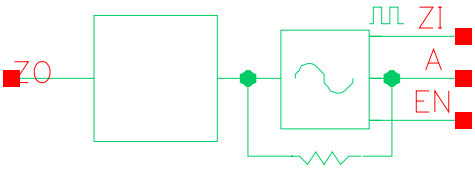
OUTPUT Pin	Max. load
Z	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
A to Z	Fall delay	0.23	0.30	0.36	0.47	0.47
A to Z	Rise delay	0.27	0.36	0.44	0.61	0.61

CMOS035 MTC45100	Oscillator 13 Mhz	OSCI13B

SYMBOL



BEHAVIOUR

A	ENZ	IZ	O
1	1	0	
0	1		1

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	11.7 SL
EN	8.0 SL

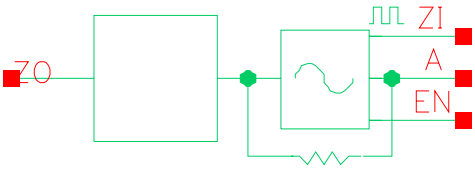
OUTPUT Pin	Max. load
ZI	38 SL
ZO	0.352 pF

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
A to ZI	Fall delay	1.63	1.75	1.88	2.12	1.87
A to ZI	Rise delay	9.61	10.35	11.12	12.65	11.06
A to ZO	Fall delay	0.77	0.83	0.88	1.00	0.88
A to ZO	Rise delay	7.31	7.89	8.49	9.69	8.44
EN to ZI	Fall delay	0.27	0.31	0.35	0.41	0.34
EN to ZI	Rise delay	0.24	0.28	0.32	0.39	0.32
EN to ZO	Fall delay	0.99	1.05	1.11	1.22	1.10
EN to ZO	Rise delay	7.36	7.94	8.54	9.74	8.49

CMOS035 MTC45100	Oscillator 32 khz	OSCI32B

SYMBOL



BEHAVIOUR

A	ENZ	IZ	O
1	1	0	
0	1		1

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	8.6 SL
EN	5.9 SL

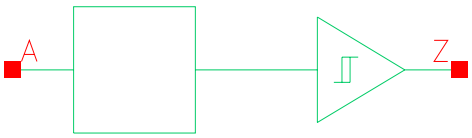
OUTPUT Pin	Max. load
ZI	38 SL
ZO	0.352 pF

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
A to ZI	Fall delay	3.53	3.77	4.00	4.46	3.98
A to ZI	Rise delay	29.16	31.47	33.89	38.71	33.70
A to ZO	Fall delay	1.14	1.23	1.32	1.51	1.32
A to ZO	Rise delay	17.04	18.43	19.88	22.79	19.77
EN to ZI	Fall delay	0.28	0.33	0.37	0.43	0.36
EN to ZI	Rise delay	0.29	0.33	0.37	0.44	0.37
EN to ZO	Fall delay	1.29	1.38	1.47	1.66	1.46
EN to ZO	Rise delay	17.01	18.40	19.85	22.76	19.74

CMOS035 MTC45100	CMOS Schmitt Trigger Input Pad Buffer	SCHMITC

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.820 pF

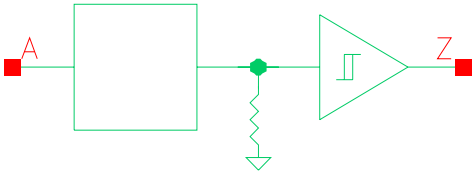
OUTPUT Pin	Max. load
Z	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
A to Z	Fall delay	0.63	0.74	0.83	0.99	0.99
A to Z	Rise delay	0.58	0.71	0.82	1.03	1.03

CMOS035 MTC45100	CMOS Schmitt Trigger Input Pad Buffer with Active Pull-Down	SCHMITCD

SYMBOL



BEHAVIOUR

A	Z
11	

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.823 pF

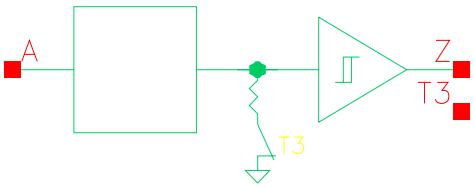
OUTPUT Pin	Max. load
Z	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
A to Z	Fall delay	0.63	0.75	0.84	0.99	0.99
A to Z	Rise delay	0.59	0.72	0.83	1.04	1.04

CMOS035 MTC45100	CMOS Schmitt Trigger Input Pad Buffer with Active Pull-Down	SCHMITCDQ

SYMBOL



BEHAVIOUR

A	T3Z	
1	-	1

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.831 pF
T3	0.7 SL

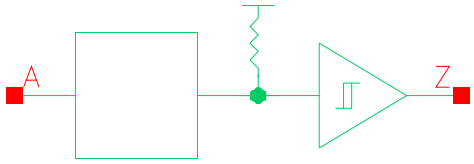
OUTPUT Pin	Max. load
Z	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
A to Z	Fall delay	0.56	0.66	0.74	0.87	0.87
A to Z	Rise delay	0.53	0.63	0.72	0.89	0.89

CMOS035 MTC45100	CMOS Schmitt Trigger Input Pad Buffer with Active Pull-Up	SCHMITCU

SYMBOL



BEHAVIOUR

A	Z
11	

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.826 pF

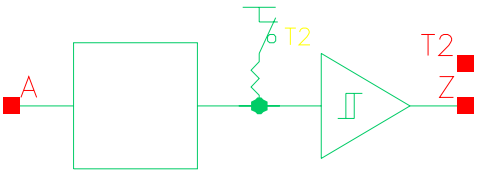
OUTPUT Pin	Max. load
Z	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
A to Z	Fall delay	0.64	0.76	0.85	1.01	1.01
A to Z	Rise delay	0.60	0.72	0.83	1.04	1.04

CMOS035 MTC45100	CMOS Schmitt Trigger Input Pad Buffer with Active Pull-Up	SCHMITCUQ

SYMBOL



BEHAVIOUR

A	T2	Z
1	-	1

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.831 pF
T2	0.5 SL

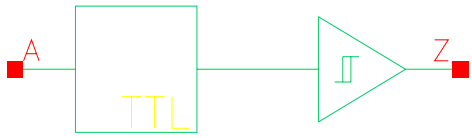
OUTPUT Pin	Max. load
Z	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
A to Z	Fall delay	0.56	0.66	0.74	0.87	0.87
A to Z	Rise delay	0.52	0.62	0.71	0.88	0.88

CMOS035 MTC45100	TTL Schmitt Trigger Input Pad Buffer	SCHMITT

SYMBOL



BEHAVIOUR

A	Z
11	

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.825 pF

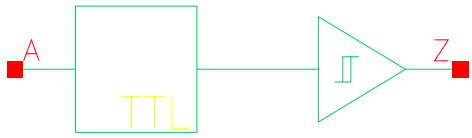
OUTPUT Pin	Max. load
Z	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
A to Z	Fall delay	0.60	0.72	0.80	0.96	0.96
A to Z	Rise delay	0.46	0.58	0.69	0.90	0.90

CMOS035 MTC45100	TTL Five Volt tolerant Schmitt Trigger Input Pad Buffer	SCHMITT_FT

SYMBOL



BEHAVIOUR

A	Z
11	

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.518 pF

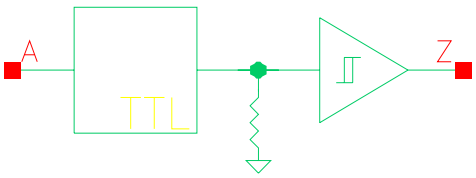
OUTPUT Pin	Max. load
Z	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
A to Z	Fall delay	0.82	0.95	1.06	1.23	1.22
A to Z	Rise delay	1.01	1.12	1.21	1.37	1.37

CMOS035 MTC45100	TTL Schmitt Trigger Input Pad Buffer with Active Pull-Down	SCHMITTD

SYMBOL



BEHAVIOUR

A	Z
11	

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.828 pF

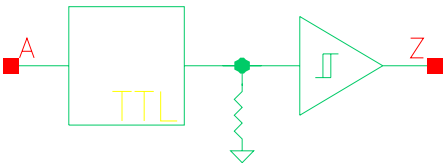
OUTPUT Pin	Max. load
Z	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
A to Z	Fall delay	0.61	0.72	0.81	0.96	0.96
A to Z	Rise delay	0.47	0.59	0.70	0.91	0.91

CMOS035 MTC45100	TTL Five Volt tolerant Schmitt Trigger Input Pad Buffer with Active Pull-Down	SCHMITTD_FT

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.518 pF

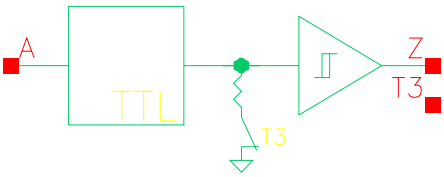
OUTPUT Pin	Max. load
Z	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
A to Z	Fall delay	0.82	0.96	1.06	1.23	1.23
A to Z	Rise delay	1.22	1.33	1.42	1.59	1.58

CMOS035 MTC45100	TTL Schmitt Trigger Input Pad Buffer with Active Pull-Down	SCHMITTDQ

SYMBOL



BEHAVIOUR

A	T3	Z
1	-	1

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.836 pF
T3	0.7 SL

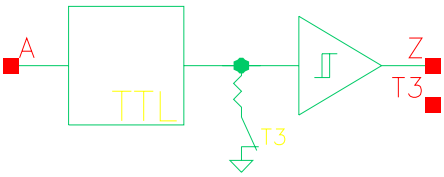
OUTPUT Pin	Max. load
Z	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
A to Z	Fall delay	0.50	0.60	0.68	0.80	0.80
A to Z	Rise delay	0.45	0.55	0.63	0.80	0.80

CMOS035 MTC45100	TTL Five Volt tolerant Schmitt Trigger Input Pad Buffer with Active Pull-Down	SCHMITTDQ_ FT

SYMBOL



BEHAVIOUR

A	T3	Z
1	-	1

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.494 pF
T3	0.7 SL

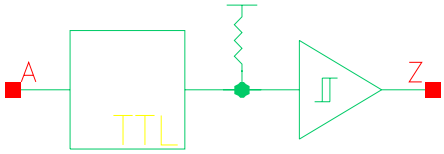
OUTPUT Pin	Max. load
Z	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
A to Z	Fall delay	0.85	0.98	1.08	1.25	1.25
A to Z	Rise delay	1.21	1.32	1.41	1.58	1.58

CMOS035 MTC45100	TTL Schmitt Trigger Input Pad Buffer with Active Pull-Up	SCHMITTU

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.832 pF

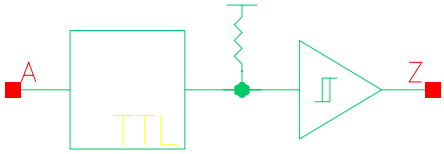
OUTPUT Pin	Max. load
Z	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
A to Z	Fall delay	0.62	0.73	0.82	0.98	0.98
A to Z	Rise delay	0.47	0.59	0.70	0.91	0.91

CMOS035 MTC45100	TTL Five Volt tolerant Schmitt Trigger Input Pad Buffer with Active Pull-Up	SCHMITTU_FT

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.518 pF

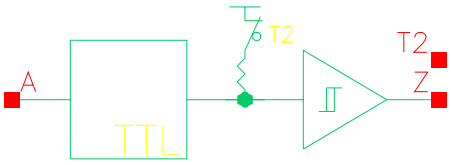
OUTPUT Pin	Max. load
Z	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
A to Z	Fall delay	0.90	1.04	1.14	1.31	1.31
A to Z	Rise delay	0.94	1.05	1.14	1.31	1.31

CMOS035 MTC45100	TTL Schmitt Trigger Input Pad Buffer with Active Pull-Up	SCHMITTUQ

SYMBOL



BEHAVIOUR

A	T2	Z
1	-	1

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.837 pF
T2	0.5 SL

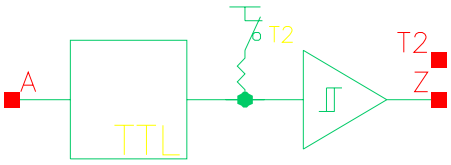
OUTPUT Pin	Max. load
Z	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
A to Z	Fall delay	0.50	0.60	0.67	0.80	0.80
A to Z	Rise delay	0.44	0.54	0.63	0.79	0.79

CMOS035 MTC45100	TTL Five Volt tolerant Schmitt Trigger Input Pad Buffer with Active Pull-Up	SCHMITTUQ_FT

SYMBOL



BEHAVIOUR

A	T2	Z
1	-	1

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.495 pF
T2	0.7 SL

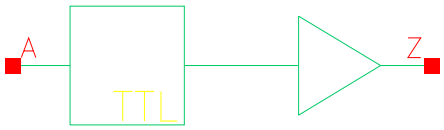
OUTPUT Pin	Max. load
Z	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
A to Z	Fall delay	0.88	1.01	1.11	1.28	1.28
A to Z	Rise delay	1.02	1.13	1.22	1.39	1.39

CMOS035 MTC45100	TTL Input Pad Buffer	TLCHT

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.824 pF

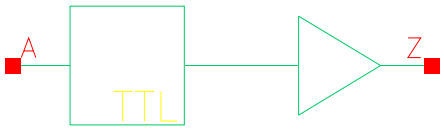
OUTPUT Pin	Max. load
Z	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
A to Z	Fall delay	0.30	0.39	0.46	0.58	0.58
A to Z	Rise delay	0.31	0.40	0.48	0.65	0.64

CMOS035 MTC45100	TTL Five Volt tolerant Input Pad Buffer	TLCHT_FT

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.523 pF

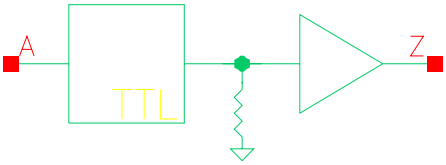
OUTPUT Pin	Max. load
Z	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
A to Z	Fall delay	0.33	0.42	0.49	0.61	0.61
A to Z	Rise delay	0.43	0.52	0.61	0.77	0.77

CMOS035 MTC45100	TTL Input Pad Buffer with Active Pull-Down	TLCHTD

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.827 pF

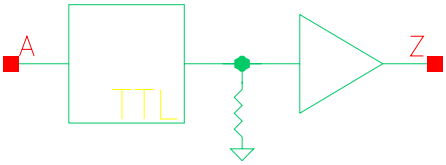
OUTPUT Pin	Max. load
Z	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
A to Z	Fall delay	0.30	0.39	0.46	0.58	0.58
A to Z	Rise delay	0.32	0.41	0.49	0.65	0.65

CMOS035 MTC45100	TTL Five Volt tolerant Input Pad Buffer with Active Pull-Down	TLCHTD_FT

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.523 pF

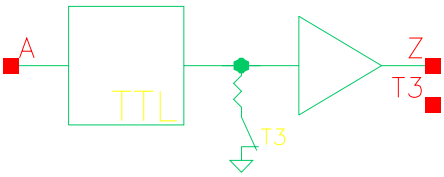
OUTPUT Pin	Max. load
Z	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
A to Z	Fall delay	0.33	0.42	0.49	0.61	0.61
A to Z	Rise delay	0.46	0.56	0.64	0.81	0.81

CMOS035 MTC45100	TTL Input Pad Buffer with Active Pull-Down	TLCHTDQ

SYMBOL



BEHAVIOUR

A	T3	Z
1	-	1

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.836 pF
T3	0.7 SL

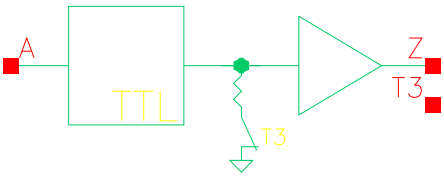
OUTPUT Pin	Max. load
Z	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
A to Z	Fall delay	0.30	0.39	0.45	0.57	0.57
A to Z	Rise delay	0.31	0.40	0.49	0.65	0.65

CMOS035 MTC45100	TTL Five Volt tolerant Input Pad Buffer with Active Pull-Down	TLCHTDQ_FT

SYMBOL



BEHAVIOUR

A	T3	Z
1	-	1

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.498 pF
T3	0.7 SL

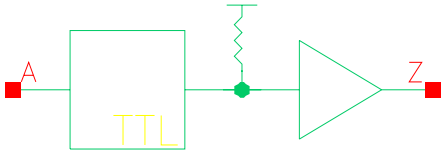
OUTPUT Pin	Max. load
Z	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
A to Z	Fall delay	0.35	0.43	0.50	0.62	0.62
A to Z	Rise delay	0.46	0.56	0.64	0.80	0.80

CMOS035 MTC45100	TTL Input Pad Buffer with Active Pull-Up	TLCHTU

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.831 pF

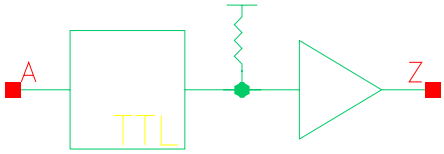
OUTPUT Pin	Max. load
Z	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
A to Z	Fall delay	0.31	0.40	0.47	0.59	0.59
A to Z	Rise delay	0.31	0.40	0.48	0.65	0.65

CMOS035 MTC45100	TTL Five Volt tolerant Input Pad Buffer with Active Pull-Up	TLCHTU_FT

SYMBOL



BEHAVIOUR

A	Z
1	1

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.523 pF

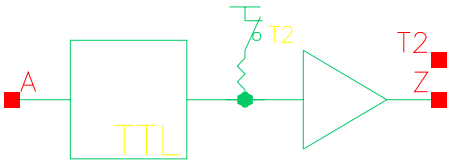
OUTPUT Pin	Max. load
Z	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
A to Z	Fall delay	0.38	0.47	0.54	0.66	0.66
A to Z	Rise delay	0.43	0.52	0.60	0.77	0.77

CMOS035 MTC45100	TTL Input Pad Buffer with Active Pull-Up	TLCHTUQ

SYMBOL



BEHAVIOUR

A	T2	Z
1	-	1

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.836 pF
T2	0.5 SL

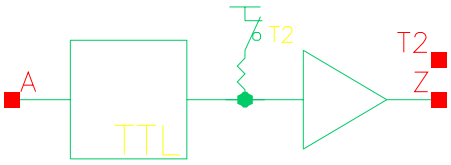
OUTPUT Pin	Max. load
Z	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
A to Z	Fall delay	0.30	0.39	0.45	0.58	0.57
A to Z	Rise delay	0.31	0.40	0.48	0.65	0.64

CMOS035 MTC45100	TTL Five Volt tolerant Input Pad Buffer with Active Pull-Up	TLCHTUQ_FT

SYMBOL



BEHAVIOUR

A	T2	Z
1	-	1

ABSTRACT

Cell Length	Cell Height	Cell Area
100.50 um	300.00 um	30150.00 um2

PIN DESCRIPTIONS

INPUT Pin	Capacitance
A	1.500 pF
T2	0.7 SL

OUTPUT Pin	Max. load
Z	80 SL

TIMINGS nS @typical P, 3.30v, 25.0C, 0.009pF SL (output load), 0.500nS SS (input slope)

Timing/Load		1.0xSL	20.0xSL	40.0xSL	80.0xSL	@maxLoad
A to Z	Fall delay	0.36	0.45	0.51	0.63	0.63
A to Z	Rise delay	0.43	0.53	0.61	0.78	0.77