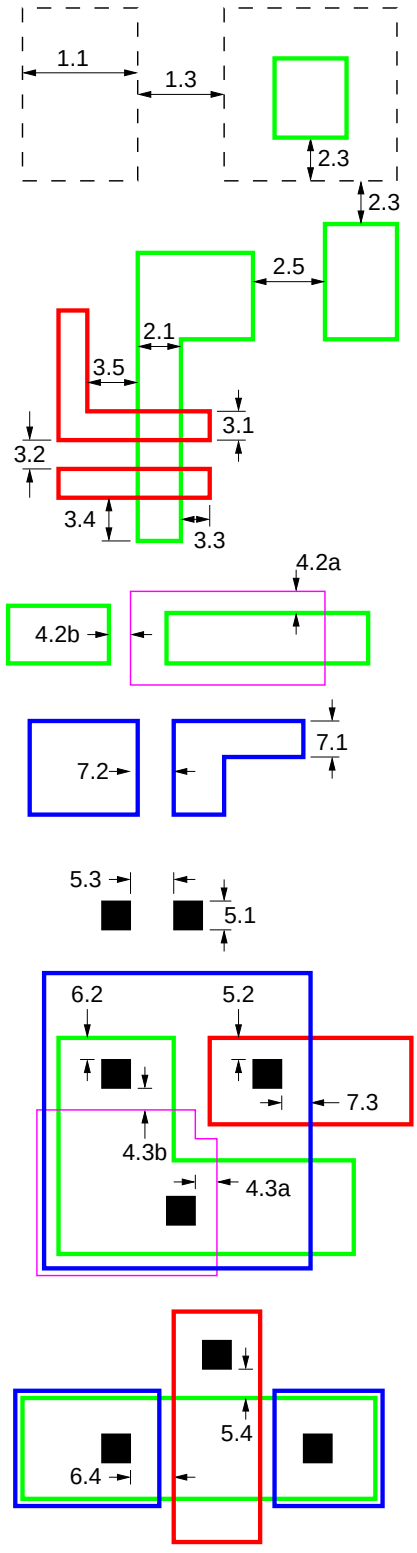
ELEC3025 Sample Design Rules

Simplified Design Rules for a 0.2um CMOS process



	Design Rule	Distance (microns)
	N−well	
1.1	Minimum n−well width	1.2
1.3	Minimum n−well spacing	0.6
	Active Area	
2.1	Minimum active area width	0.3
2.3	Minimum well edge to active area	0.6
2.5	Minimum active area spacing	0.4
	Polysilicon	
3.1	Minimum polysilicon width	0.2
3.2	Minimum polysilicon spacing	0.4
3.3	Minimum polysilicon extension beyond gate	0.25
3.4	Minimum source/drain length	0.4
3.5	Minimum polysilicon spacing to active area	0.1
	P implant	
4.2a	Minimum p implant enclosure of active area	0.2
4.2b	Minimum p implant spacing to active area	0.2
	Metal 1	
7.1	Minimum metal 1 width	0.3
7.2	Minimum metal 1 spacing	0.3
	Contact Window	
5.1	Minimum/maximum contact dimension	0.2
5.3	Minimum contact spacing	0.4
4.3a	Minimum p implant enclosure of contact	0.15
4.3b	Minimum p implant spacing to contact	0.15
5.2	Minimum polysilicon enclosure of contact	0.15
6.2	Minimum active area enclosure of contact	0.15
7.3	Minimum metal 1 enclosure of contact	0.1
5.4	Minimum polysilicon contact spacing to active area	0.2
6.4	Minimum active area contact spacing to polysilicon gate	0.2

* This is not a complete set of design rules but is sufficient for most simple cell designs *