UNIVERSITY OF SOUTHAMPTON ELEC3025W1

SEMESTER 1 EXAMINATIONS 2013/14

INTEGRATED CIRCUIT DESIGN

Duration: 120 min

Section A
Answer question A1 (15 marks) AND
EITHER question A2 (30 marks) OR question A3 (30 marks)

Section B
Answer question B1 (15 marks) AND
EITHER question B2 (30 marks) OR question B3 (30 marks)

Each section will be marked out of 45 giving a maximum of 90 marks.
The remaining marks will be awarded for coursework already submitted.

University approved calculators MAY be used.

Coloured pens/pencils will be required.

Design rules for a sample CMOS process will be provided.

Graph paper will be available.

There are two handout pages (printed in colour on plain paper) to go with this exam.

Number of Pages: 9+2

Section A

Answer question A1 and either question A2 or question A3

A1.

In order to answer this question you will have to consult the two colour handout pages supplied with this exam paper: one of which shows figure A1 while the other provides a set of sample design rules and acts as a key to the masks used in figure A1.

(a) Based on the circuit elements in figure A1, calculate
   (i) the resistance between A and A'
   (ii) the resistance between B and B'
   (iii) the approximate resistance between C and C'

given:
the sheet resistance of polysilicon is 5Ω/□ (5 ohms per square)
the sheet resistance of metal 1 is 0.1Ω/□

(5 marks)

(b) Give values in microns for the width, W, and length, L, of the NMOS transistor shown in figure A1.

(3 marks)

(c) Draw a cross section through the transistor along the line between X and X' and clearly identify its constituent parts.

Explain the term self-aligned as it applies to the gate of this transistor.

(6 marks)

A2.

(a) Derive a transistor level circuit diagram for each of the Boolean functions as a compound gate using the specified logic family:

(i) CMOS logic: $Y = \overline{A.(B+C)}$
(ii) CMOS logic: $Y = \overline{A.(B+C) + D.E}$
(iii) NMOS logic: $Y = \overline{A.(B+C) + D.(E+F)}$

In each diagram you should ensure that the type of each transistor (N-channel/P-channel Enhancement/Depletion) is clearly shown (either with the aid of a key or otherwise).

(10 marks)

(b) Derive a stick diagram for the efficient layout of each of the following Boolean functions for use as a standard cell in a CMOS process that supports just one metal layer:

i) $Y = \overline{A.(B+C)}$
ii) $Y = \overline{A.(B+C) + D.E}$

(12 marks)

(c) Show how the stick diagram for $Y = \overline{A.(B+C)}$ can be adapted for use as a standard cell in a CMOS process that supports:

(i) 2 metal layers
(ii) 3 metal layers

In each case you should show clearly on your diagram the position of the ports and you should briefly describe the inter-cell wiring that would be used to connect the gate to others in a standard cell design.

(8 marks)

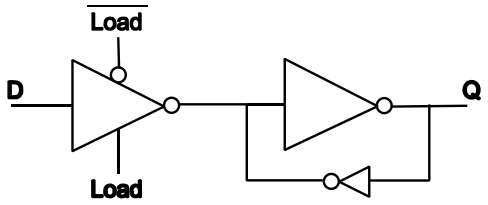
TURN OVER

Section A *(continued)*

Answer question A1 and either question A2 or question A3

A3.

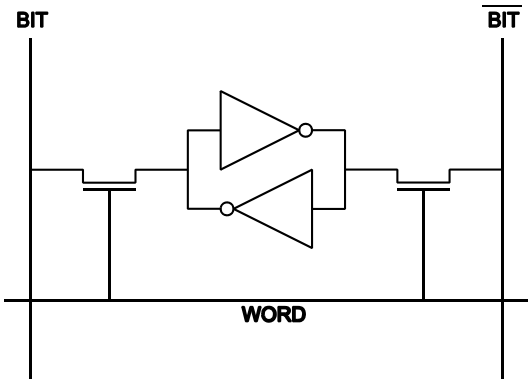
(a) The following is a circuit diagram a CMOS jamb latch:



Draw a transistor level diagram of the jamb latch and explain its operation. In your explanation, you should discuss the sizes of the different transistors where this affects functionality.

(8 marks)

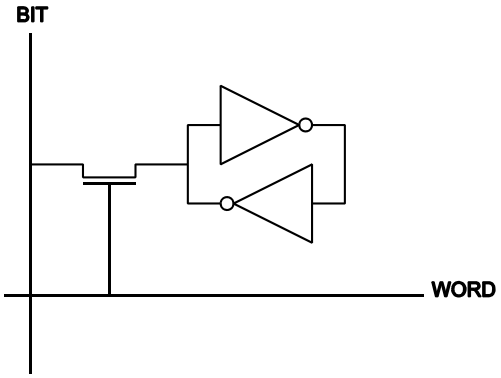
(b) The following is a circuit diagram for a CMOS 6 transistor static RAM cell:



Draw a diagram showing the read and write circuitry required to support this RAM cell and briefly explain the operation of the cell for both read and write operations. Be sure to mention any conflict that may occur during read and write and explain how the sizes of the different transistors affect the resolution of such conflict.

(15 marks)

(c) An alternative static RAM cell uses just 5 transistors:



Discuss the problems associated with using this 5 transistor cell when compared to the 6 transistor version. You should consider the resolution of conflicts during operation, the sizing of transistors, and the design of associated read and write circuitry.

(7 marks)

Section B

Answer question B1 and either question B2 or question B3

B1.

(a) Realise the following logic functions using CPL logic
(i) AND/NAND
(ii) OR/NOR
(iii) XOR/XNOR

(5 marks)

(b) You have 12 transmission gates connected in series. If each of the transmission gates has an "ON" resistance = 20 Ω and output capacitance = 4 pF then what will be the rise time of entire arrangement when all the transmission gates are "ON"?

(5 marks)

(c) If you insert buffer at every 3rd position of the transmission gate chain in B1(b) and if each buffer has a delay of 100 ps then what will be rise time of this arrangement?

(5 marks)

B2.

(a) Derive the expression for the average dynamic power dissipation for a square wave input in a symmetric inverter by clearly stating all the assumptions you are making.

(6 marks)

(b) Calculate the output switching activities (i. e. Y1, Y2 and Y3 respectively) for the following functions

(i) Y1 = a XOR b XOR c
(ii) Y2 = (a AND b) XOR (c OR d)
(iii) Y3 = a OR b AND c

Where a, b, c and d are the primary inputs with equal probability of occurrence of logic 1 and 0.

(18 marks)

(c) What are the two major components for leakage power dissipation and what are their origins? Name the three most effective circuit level design techniques for reduction of leakage current?

(6 marks)

Section B *(continued)*

Answer question B1 and either question B2 or question B3

B3.

(a) (i) Using a table clearly show the states of the PMOS and NMOS transistors for each of the following regions of the CMOS inverter characteristics.
Consider V_{in} = input voltage, V_{tn} = threshold voltage of the NMOS, V_{DD} = supply voltage and V_{tp} = threshold voltage of the PMOS.

Region A: $0 \leq V_{in} < V_{tn}$,
Region B: $V_{tn} \leq V_{in} < V_{DD}/2$,
Region C: $V_{in} = V_{DD}/2$,
Region D: $V_{DD}/2 < V_{in} \leq V_{DD} - |V_{tp}|$, and
Region E: $V_{in} > V_{DD} - |V_{tp}|$.

(8 marks)

(ii) For Region B, C and D draw the equivalent circuit model for the CMOS inverter and clearly show the direction of currents in each case.

(6 marks)

(b) For an NMOS transistor having width (W) = 4.8 μm, channel length (L) = 1.2 μm, derive the value of transconductance (g_m) when it operates in the linear region and the saturation region of its DC characteristic (whichever applicable) using the following parameters:

Carrier mobility (μ) = 500 cm^2/V-sec
Permittivity of silicon dioxide (ε) = 30.975×10^{-14} F/cm
Oxide thickness (t_{ox}) = 100×10^{-8} cm
Drain voltage (V_D) = 5 V
Gate voltage (V_G) = 4 V
Threshold voltage = 0.8 V
Source voltage (V_S) = 0 V

(6 marks)

(c) Through appropriate circuit diagram and mathematical analysis show that for a step input to a CMOS inverter the fall time (t_f) can be given by the following expression

$$t_f = 2\frac{C_L}{\beta_n V_{DD}(1-n)}\left[\frac{(n-0.1)}{1-n} + \frac{1}{2}\ln(19-20n)\right] \approx k\frac{C_L}{\beta_n V_{DD}}$$

where, C_L is the load capacitance, $n = V_{tn}/V_{DD}$, V_{tn} is the threshold voltage of the NMOS transistor and β_n is the process gain factor for the NMOS.

(7 marks)

(d) Considering the carrier mobility for PMOS is three times lower than the carrier mobility in NMOS show that the rise and fall time of a 3-input NAND gate is approximately equal when using transistors of equal size (i. e., both PMOS and NMOS has equal width and length.

(3 marks)

END OF PAPER