ELEC3025W1

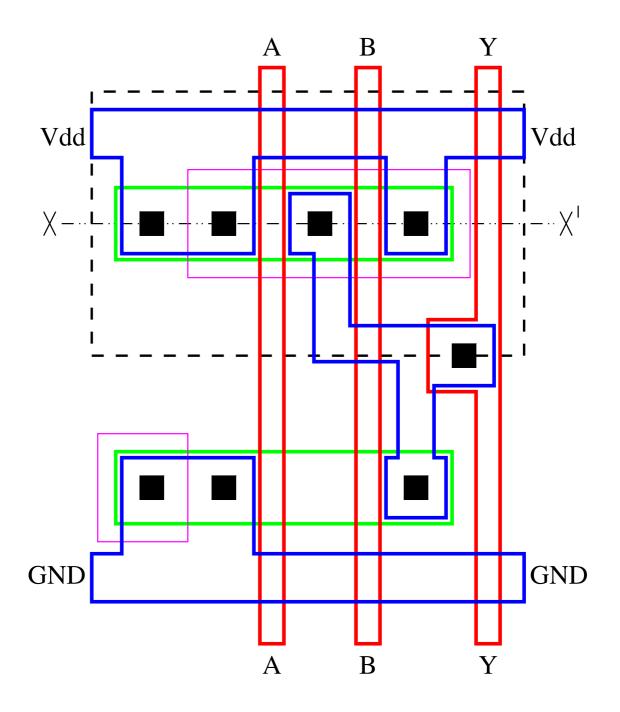


Figure A1: Mask level layout of a two-input CMOS NAND gate

