UNIVERSITY OF SOUTHAMPTON ELEC3025W1

SEMESTER 1 EXAMINATIONS 2012/13

INTEGRATED CIRCUIT DESIGN

Duration: 120 min

Section A
Answer question A1 (15 marks) AND
EITHER question A2 (30 marks) OR question A3 (30 marks)

Section B
Answer question B1 (15 marks) AND
EITHER question B2 (30 marks) OR question B3 (30 marks)

Each section will be marked out of 45 giving a maximum of 90 marks.
The remaining marks will be awarded for coursework already submitted.

University approved calculators MAY be used.

Coloured pens/pencils will be required.

Design rules for a sample CMOS process will be provided.

Graph paper will be available.

Number of Pages: 8+2

Section A

Answer question A1 and either question A2 or question A3

A1.

In order to answer this question you will have to consult the two colour handout pages supplied with this exam paper: one of which shows figure A1 while the other provides a set of sample design rules and acts as a key to the masks used in figure A1.

Figure A1 shows the mask level layout of a two-input CMOS NAND gate.

(a) The line between X and X' on figure A1 cuts through two transistors. Draw a cross-sectional diagram of the gate along this line and identify the doping regions according to their type (p+, p, n, n+) and their function (wafer substrate, well, tap, source, drain).

(9 marks)

(b) In the sample design rules, rule 19.5 determines how close a poly gate contact may be to the channel of a transistor. Explain the implications of ignoring this rule and placing the contact over channel. What factors related to processing might affect the numeric value of this design rule?

(6 marks)

A2.

(a) Any Boolean function may be expressed in *Sum Of Products* (SOP) form and hence implemented using only two levels of logic (a first level using AND gates and a second level using OR gates) provided that inverted and non-inverted inputs are available.

Derive an implementation for each of the Boolean functions:

$$X = A.\overline{C} + B.C.D + \overline{B}$$
$$Y = (\overline{A} + B.D).C$$
$$Z = A \oplus C$$

using two levels of logic (AND and OR gates).

You may assume the availability of inverted inputs.

(10 marks)

(b) A CMOS PLA employs *Pseudo-NMOS* NOR gates and inverters in order to implement sets of SOP expressions.

(i) Draw a transistor level schematic diagram of a *Pseudo-NMOS* NOR gate and briefly describe its operation.

(ii) Explain how *Pseudo-NMOS* NOR gates are used in the AND and OR planes of a PLA. Illustrate your answer with a gate level schematic diagram of a PLA to implement the Boolean functions:

$$X = A.\overline{C} + B.C.D + \overline{B}$$
$$Y = (\overline{A} + B.D).C$$
$$Z = A \oplus C$$

(iii) Draw a stick diagram layout of the AND plane of the PLA described in part (ii).

You may assume the availability of inverted inputs.

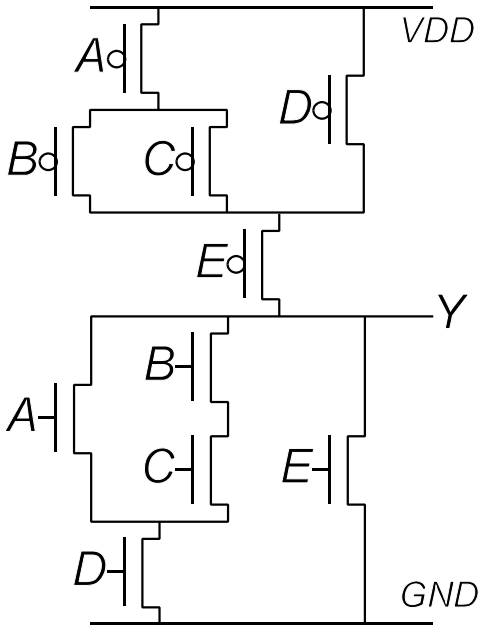
(20 marks)

Section A *(continued)*

Answer question A1 and either question A2 or question A3

A3.

(a) The following circuit diagram is for a CMOS compound gate:



(i) Derive a Boolean expression for this compound gate.

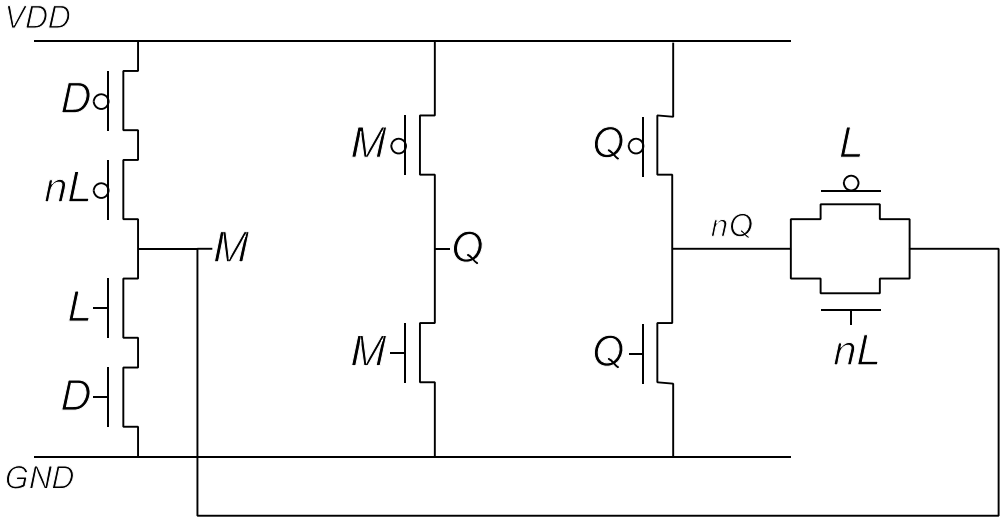
(ii) If one exists, identify an Euler path that passes through all of the PMOS transistors exactly once and a matching Euler path that passes through all of the NMOS transistors exactly once.

Copy the circuit diagram into your answer book and mark the Euler paths on your copy of the diagram.

(iii) Based on your Euler path analysis, derive a suitable stick diagram for efficient layout of this compound gate.

(14 marks)

(b) The following circuit diagram is for a transparent latch with Q and nQ outputs:



(i) If one exists, identify an Euler path that passes through all of the PMOS transistors exactly once.

If one exists, identify an Euler path that passes through all of the NMOS transistors exactly once.

Copy the circuit diagram into your answer book and mark the Euler paths on your copy of the diagram.

(ii) Based on your Euler path analysis, derive a suitable stick diagram for the efficient layout of this transparent latch. Your diagram should clearly show the Q and nQ outputs.

(16 marks)

SectionB

Answer question B1 and either question B2 or question B3

B1.

(a) Explain with a diagram why a PMOS transistor cannot pass a logic 0 efficiently while the NMOS transistor cannot pass logic 1 efficiently?

(5 marks)

(b) Explain with a proper diagram how the differential logic structure may be used for restoring the level of a weak logic 1.

(5 marks)

(c) Realise the dynamic logic circuit for a 2-input NOR gate.

(*5 marks*)

B2.

(a) List the problems of low-power design through voltage scaling.

(4 marks)

(b) Fig. B2(b1) and Fig. B2(b2) show two possible implementations of the function w = ABCD. Analysing switching activity at each of the nodes shown in the Fig. B2(b1) and B2(b2) determine which one of these results in lower power consumption. Assume the following in your analysis:

One AND gate has 1nF capacitance associated with each of its input and output.
Both the circuits run at an arbitrary supply voltage VDD and frequency f
Probability of having a logic 1 at A = 0.5
Probability of having a logic 1 at B = 0.2
Probability of having a logic 1 at C = 0.1
Probability of having a logic 1 at D = 0.5
Ignore the effect of any capacitance associated with the primary inputs (i. e., associated with A, B, C and D) of the AND gates.

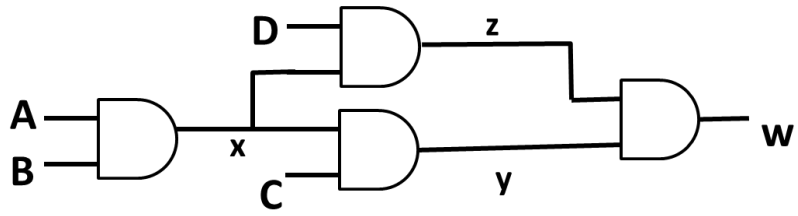


Fig. B2(b1)

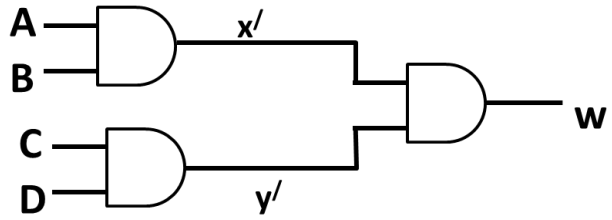


Fig. B2(b2)

(20 marks)

(c) What is the origin of dynamic power dissipation in a circuit? List the capacitances which contribute to the overall load capacitance of a circuit.

(6 marks)

SectionB *(continued)*

Answer question B1 and either question B2 or question B3

B3.

(a) Using proper derivation of related equations find the drain current (I_{ds}) for an NMOS transistor under the following conditions

(i) V_G = 3.3 V, V_S = 0 V, V_T = 0.2 V, V_D = 0.2 V
(ii) V_G = 3.3 V, V_S = 0 V, V_T = 0.2 V, V_D = 2.5 V
(iii) V_G = 3.3 V, V_S = 0 V, V_T = 0.2 V, V_D = 3.3 V

where V_G, V_S and V_D are the voltages at the gate, source and drain respectively and V_T is the threshold voltage of the NMOS transistor. Use the following data for your analysis:

Width of the transistor (W) = 3.6 μm
Channel length (L) = 1.2 μm
Carrier mobility (μ) = 500 cm^2/V-sec
Permittivity of silicon dioxide (ε) = 30.975 × 10^{-14} F/cm
Oxide thickness (t_{ox}) = 200 × 10^{-8} cm

(16 marks)

(b) For an inverter the rise time and fall time are given by the following sets of equations:

$T_r = k (C_L/\beta_p V_{DD})$
$T_f = k (C_L/\beta_n V_{DD})$

Where T_r and T_f are the rise and fall times respectively, C_L is the load capacitance, V_{DD} is the supply voltage and β_p and β_n are the gains for the PMOS and NMOS transistors respectively. Using these and giving proper explanations find the ratio of rise and fall times of a 2-input NOR gate. Assume carrier mobility for NMOS is 3 times that of PMOS and equal width for NMOS and PMOS transistors.

(6 marks)

(c) Draw the small signal AC model of a MOSFET explaining the origin of each component of the model.

(*8 marks*)

END OF PAPER