UNIVERSITY OF SOUTHAMPTON ELEC3025W1

SEMESTER 1 EXAMINATIONS 2011/12

INTEGRATED CIRCUIT DESIGN

Duration: 120 min

Answer question A1
and ONE question from section B
and ONE question from section C

Each question will be marked out of 30 giving a maximum of 90 marks.
The remaining marks will be awarded for coursework already submitted.

University approved calculators MAY be used.

Coloured pens/pencils will be required.

Design rules for a sample CMOS process will be provided.

Graph paper will be available.

Number of Pages: 8

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Section A

Answer question A1
(there are no other questions in section A)

A1.

(a) State Moore's Law.

What factors might cause Moore's law to fail in future?

(5 marks)

(b) Explain the principle of two conductor routing and discuss the benefits of a three metal process rather than a two metal process in supporting two conductor routing.

How might an automatic routing tool make use of a process supporting five metal layers?

(5 marks)

(c) Draw a gate level circuit diagram of a master slave D-type flip flop which uses tristate inverters for multiplexing and briefly describe its operation.

(5 marks)

(d) Explain the general principle of operation of a dynamic logic inverter designed in pull-down topology.

(4 marks)

(e) What are the advantages and disadvantages of a dynamic logic circuit?

Explain with circuit diagrams (wherever appropriate) how the disadvantages can be handled.

(6 marks)

(f) Realize the dynamic logic circuit for the following logic function:

$$Y = \overline{(A.B + C.D).E}$$

where A, B, C, D and E are the inputs to the circuit.

(5 marks)

Section B

Answer either question B1 or question B2

B1.

In order to answer this question you will have to consult the two colour handout pages supplied with this exam paper: one of which shows figure B1 while the other provides a set of sample design rules and acts as a key to the masks used in figure B1.

Figure B1 shows the mask level layout of a two-input CMOS gate which uses pass transistor and transmission gate techniques.

(a) The line between X and X' on figure B1 cuts through three transistors. Draw a cross-sectional diagram of the gate along this line and identify the doping regions according to their type (p or n) and their function (wafer substrate, well, tap or source/drain).

(10 marks)

(b) With reference to the masks in figure B1 and your cross sectional diagram, explain the term ***self-aligned*** as it applies to MOS transistor construction.

(5 marks)

(c) Draw a transistor level circuit diagram of the gate and identify any transmission gate and pass transistor structures within it.

(8 marks)

(d) By examining the various input combinations or otherwise, identify the function of the gate.

(7 marks)

Section B *(continued)*

Answer either question B1 or question B2

B2.

(a) The boolean expression:

$$Y = (A + B).C$$

is to be realized on integrated circuits supporting each of the following technologies:

(i) RTL
(ii) NMOS
(iii) CMOS

For each of the technologies derive a gate level circuit diagram for an efficient implementation. You should use only the gates native to the technology (including compound gates in technologies that support such gates).

(8 marks)

(b) For each of the circuits in part (a) calculate the number and type of components that will be needed on the integrated circuit. Please show clearly how you have calculated your answers.

(6 marks)

(c) The following boolean expressions are to be realized as static CMOS complementary gates:

$$Y = \overline{A} + \overline{B}$$
$$Y = \overline{A} + (\overline{B + C}) + \overline{D}$$

(i) For each of the these gates derive a transistor level circuit diagram.

(iii) For each of the these gates derive a stick diagram based on an investigation of possible Euler paths. Your design should be targeted at a CMOS process supporting only one metal layer.

(16 marks)

Section C

Answer either question C1 or question C2

C1.

(a) (i) Using a table clearly show the states of the PMOS and NMOS transistors for each of the following regions of the CMOS inverter characteristics. Consider V_{in} = input voltage, V_{tn} = threshold voltage of the NMOS, V_{DD} = supply voltage and V_{tp} = threshold voltage of the PMOS.

Region A: $0 \leq V_{in} < V_{tn}$,
Region B: $V_{tn} \leq V_{in} < V_{DD}/2$,
Region C: $V_{in} = V_{DD}/2$,
Region D: $V_{DD}/2 < V_{in} \leq V_{DD} - |V_{tp}|$, and
Region E: $V_{in} > V_{DD} - |V_{tp}|$.

(8 marks)

(ii) For Region B, C and D draw the equivalent circuit model for the CMOS inverter and clearly show the direction of currents in each case.

(6 marks)

(b) For an NMOS transistor having width (W) = 3.6 μm, channel length (L) = 1.2 μm, derive the value of transconductance (g_m) when it operates in the linear region and the saturation region of its DC characteristic (whichever applicable) using the following parameters:

Carrier mobility (μ) = 500 cm^2/V-sec
Permittivity of silicon dioxide (ε) = 30.975×10^{-14} F/cm
Oxide thickness (t_{ox}) = 200×10^{-8} cm
Drain voltage (V_D) = 5 V
Gate voltage (V_G) = 4 V
Threshold voltage = 0.8 V
Source voltage (V_S) = 0 V

(6 marks)

(c) Through appropriate circuit diagram and mathematical analysis show that for a step input to a CMOS inverter the fall time (t_f) can be given by the following expression

$$t_f = 2\frac{C_L}{\beta_n V_{DD}(1-n)}\left[\frac{(n-0.1)}{1-n} + \frac{1}{2}\ln(19-20n)\right] \approx k\frac{C_L}{\beta_n V_{DD}}$$

where, C_L is the load capacitance, $n = V_{tn}/V_{DD}$, V_{tn} is the threshold voltage of the NMOS transistor and β_n is the process gain factor for the NMOS.

(7 marks)

(d) Considering the carrier mobility for PMOS is three times lower than the carrier mobility in NMOS show that the rise and fall time of a 3-input NAND gate is approximately equal when using transistors of equal size (i. e. both PMOS and NMOS have equal width and length).

(3 marks)

Section C continues on the next page

Section C *(continued)*

Answer either question C1 or question C2

C2.

(a) Derive the expression for the average dynamic power dissipation for a square wave input in a symmetric inverter. Clearly state all the assumptions you are making.

(6 marks)

(b) With reference to the circuit shown in Figure C2(b), calculate the average dynamic power consumption of the circuit by considering that the primary inputs are independent and uniformly distributed. Use the following data:
Delays of XOR, OR and NOR gates are 12 ns, 5 ns and 8 ns respectively and the set up time of the register R is 0.2 ns. Lumped capacitances at X, Y and Z are 20 pF, 16 pF and 8 pF respectively. The supply voltage is 3 V.

(18 marks)

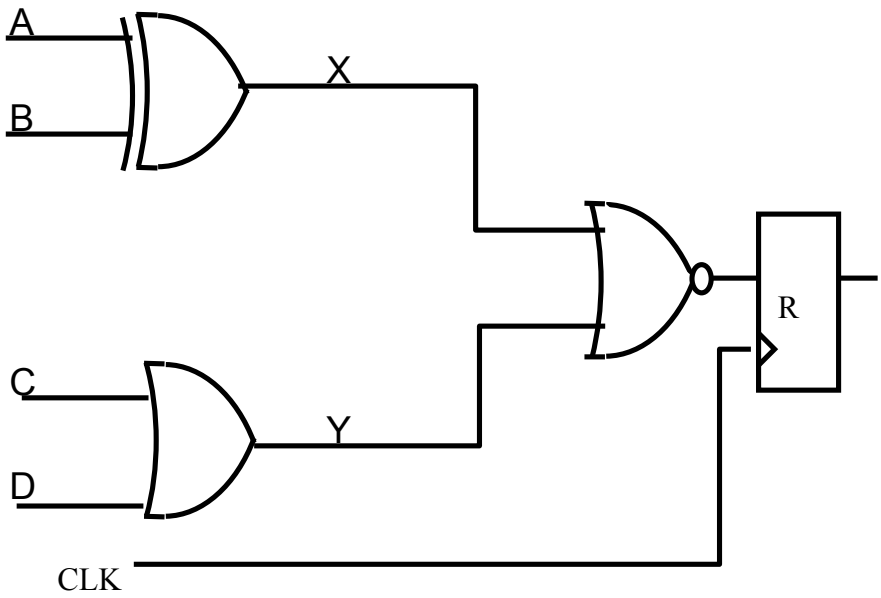

Figure C2(b)

(c) What are the two major components for leakage power dissipation and what are their origins? What are the process level and circuit level parameters one can use to control leakage?

(6 marks)

END OF PAPER