UNIVERSITY OF SOUTHAMPTON ELEC3025W1

SEMESTER 1 EXAMINATIONS 2010/11

INTEGRATED CIRCUIT DESIGN

Duration: 120 min

Answer THREE out of FIVE questions.

University approved calculators MAY be used.

Coloured pens/pencils will be required.

Design rules for a sample CMOS process will be provided.

Graph paper will be available.

Number of Pages: 6

1.
The following boolean expressions are to be implemented as standard cells on an integrated circuit:

$$Y = \overline{A.B + C} + \overline{D}$$
$$Y = (\overline{A}.\overline{B} + \overline{C}.\overline{D}).\overline{E}$$

(a) (i) For each of the boolean expressions derive a transistor level circuit diagram for its implementation as a static NMOS compound gate.

(ii) For each of the boolean expressions derive a transistor level circuit diagram for its implementation as a static CMOS complementary compound gate.

(iii) Discuss the relative merits of NMOS and CMOS technologies in the light of these circuit diagrams.

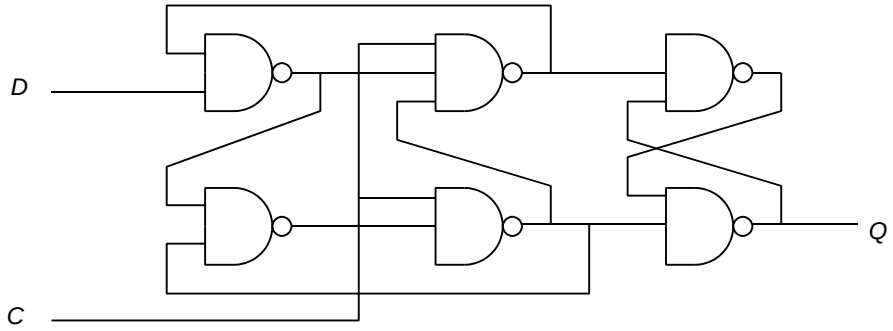
(16 marks)

(b) For each of the boolean expressions derive a suitable stick diagram for efficient implementation of the compound gate using a CMOS process which supports either 1 or 2 metal layers. Where applicable your design should be based on an investigation of possible Euler paths.

(17 marks)

2.

(a)



By drawing sub-circuit schematics (or otherwise), calculate the number of transistors in the above edge triggered D-type flip flop.

(4 marks)

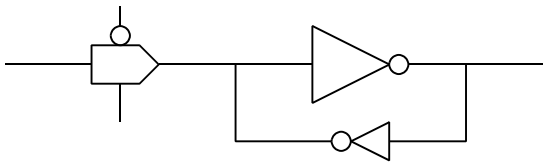
(b) A transparent latch may be built around a multiplexer based on either transmission gates or tristate inverters.
With reference to an appropriate circuit diagram, show that we can build a master slave D-type using two such latches which will have fewer transistors than the edge triggered D-type from part (a).

(8 marks)

(c) Derive a stick diagram for the layout of your chosen master slave D-type.

(12 marks)

(d) Discuss the operation of a D-type based on a *jamb latch* circuit such as shown below:



What are the benefits and drawbacks of this approach?

(9 marks)

3.

(a) Derive the expression for the average dynamic power dissipation for a square wave input in a symmetric inverter by clearly stating all the assumptions you are making.

(6 marks)

(b) With reference to the circuit shown in Figure Q3(b), calculate the power consuming transition probability at the nodes X, Y and Z. Consider that the primary inputs A, B, C and D are independent and uniformly distributed.

(14 marks)

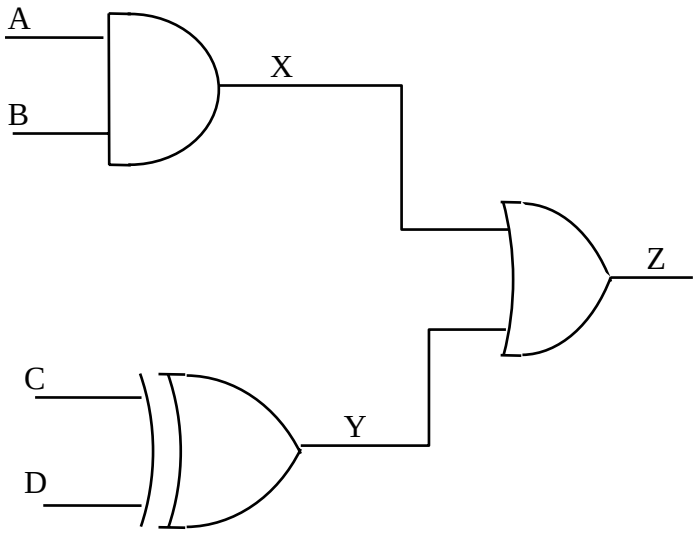


Figure Q3(b)

(c) What are the different levels of power optimisation in a typical VLSI design flow? Describe how the power can be optimised at each of these levels.

(*7 marks*)

(d) List different sources of power dissipation in a CMOS circuit? Discuss their origins.

(6 marks)

4.

(a) Giving appropriate diagram derive the expressions for drain current (I_{ds}) for a NMOS transistor for the following operating conditions.

(i) $V_{ds} << V_{gs} - V_t$ (Channel is uniform between the source and drain)
(ii) $V_{ds} \leq V_{gs} - V_t$ (Channel is non-uniform between the source and drain)
(iii) $V_{ds} > V_{gs} - V_t$ (NMOS is pinched off)

Where, V_{ds} = drain to source voltage, V_{gs} = gate to source voltage and V_t = threshold voltage of the NMOS.

(15 marks)

(b) Draw the small signal AC model of a MOSFET explaining the origin of each components of the model.

(6 marks)

(c) Through appropriate circuit diagram and mathematical analysis show that for a step input to a CMOS inverter the fall time (t_f) can be given by the following expression

$$t_f = 2\frac{C_L}{\beta_n V_{DD}(1-n)}\left[\frac{(n-0.1)}{1-n} + \frac{1}{2}\ln(19-20n)\right] \approx k\frac{C_L}{\beta_n V_{DD}}$$

where, C_L is the load capacitance, $n = V_{tn}/V_{DD}$, V_{tn} is the threshold voltage of the NMOS transistor and β_n is the process gain factor for the NMOS.

(*8 marks*)

(d) Considering the carrier mobility for PMOS is three times lower than the carrier mobility in NMOS what is the ratio of fall time to the rise time for a symmetric inverter (equally sized PMOS and NMOS)?

(4 marks)

5.

(a) Realise the following logic functions using CPL logic

(i) AND/NAND
(ii) OR/NOR
(iii) XOR/XNOR *(6 marks)*

(b) You have 12 transmission gates connected in series. If each of the transmission gates has an "ON" resistance = 20 Ω and output capacitance = 4 pF then what will be the rise time of entire arrangement when all the transmission gates are "ON"?

(6 marks)

(c) If you insert buffer at every 3rd position of the transmission gate chain in Q 5(b) and if each buffer has a delay of 100 ps then what will be rise time of this arrangement?

(5 marks)

(d) (i) Draw a stick diagram for a 2 input NOR gate for implementation using a CMOS process supporting only one metal layer.

(4 marks)

(ii) Given transistor dimensions: $W_N = 0.3\ \mu m$, $W_P = 1.5\ \mu m$ and $L_N = L_P = 0.2\ \mu m$, sketch a mask level layout for the NMOS transistors in your 2 input NOR gate based on the sample design rules provided. *Your sketch need not be to scale.*

(5 marks)

(iii) From your sketch, calculate the area occupied by the NMOS transistors and their associated source and drain contacts. Also calculate the change in the area occupied if the width of the NMOS transistors is increased to $W_N = 0.5\ \mu m$.
What factors might affect the choice of optimum transistor size in a standard cell library?

(7 marks)

END OF PAPER