UNIVERSITY OF SOUTHAMPTON ELEC3025W1

SEMESTER 1 EXAMINATIONS 2009/10

INTEGRATED CIRCUIT DESIGN

Duration: 120 min

Answer THREE out of FIVE questions.

University approved calculators MAY be used.

Coloured pens/pencils will be required.

Design rules for a sample CMOS process will be provided.

Graph paper will be available.

Number of Pages: 8

1.

(a) Which of the following Boolean functions may be implemented as a single static CMOS complementary gate?

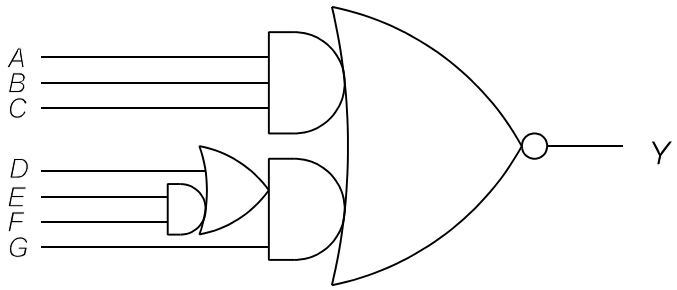
$$Y = A.B$$
$$Y = A \oplus B$$
$$Y = \overline{A + B}$$
$$Y = \overline{A \oplus B}$$
$$Y = \overline{A + B.C}$$
$$Y = (\overline{A + B}) + \overline{C}$$

Where such an implementation is possible, provide a circuit diagram showing the transistor interconnections.

Define the set of Boolean functions which may be realized as single static CMOS complementary gates.

(12 marks)

(b) The following compound gate is to be designed using CMOS technology:



(i) Write a Boolean expression which defines the function of this gate and hence derive a suitable transistor level circuit diagram.

(ii) Derive a suitable stick diagram for this gate, based on an investigation of possible Euler paths.

(iii) It is unlikely that you would find this gate in a standard cell library. In the light of this, contrast the benefits of standard cell design against those of a more highly customized approach.

(21 marks)

2.

(a) Draw a transistor level circuit diagram for a 2-input multiplexor constructed from CMOS transmission gates.

Explain the advantage of this circuit over one based only on NMOS pass transistors.

(7 marks)

(b) Derive a transistor level circuit diagram for a transparent latch based on a transmission gate multiplexor.

Explain the purpose of any additional circuitry that is added to the multiplexor to support its operation as a latch.

Derive a suitable stick diagram for efficient implementation of the latch circuit. Your design should be suitable for use as a standard cell for a CMOS process which supports two metal layers.

(18 marks)

(c) As an alternative to this transparent latch, a six transistor SRAM cell may be used for storage on a CMOS integrated circuit. Contrast the benefits of these two types of storage. In giving your answer you should be sure to consider the support circuitry that would be required for each storage type.

Why might you choose a six NAND gate edge triggered D-Type flip -flop over either of these two options?

(8 marks)

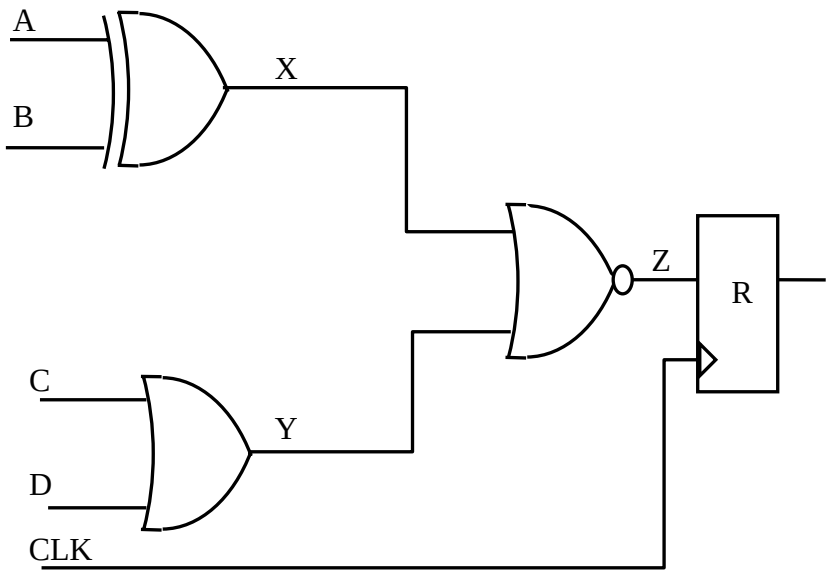
3. (a) Derive the expression for the average dynamic power dissipation for a square wave input in a symmetric inverter, clearly stating all the assumptions you are making.

(7 marks)

(b) Consider the circuit shown in Figure Q3(b). Calculate the average dynamic power consumption of the circuit by considering that the primary inputs are independent and uniformly distributed. Use the following data:

Delay of XOR, OR and NOR gates are 12 ns, 5 ns and 8 ns respectively and the setup time of the register R is 0.2 ns. Lumped capacitances at X, Y and Z are 20 pF, 16 pF and 8 pF respectively. The supply voltage is 3 V.

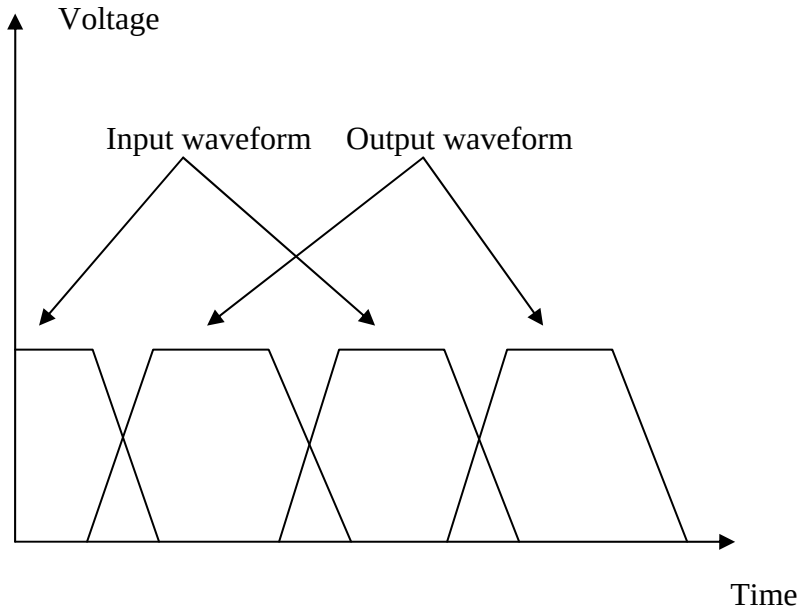
(14 marks)



Q3(b)

(c) A symmetric inverter gives the input-output pattern shown in Figure Q3(c). Sketch the pattern of current drawn from the power supply and the short circuit current, clearly stating the reasons for their behaviour.

(*6 marks*)



Q3(c)

(d) What are the two major components for leakage power dissipation and what are their origins? What are the process level and circuit level parameters one can use to control leakage?

(6 marks)

4. (a) (i) Using a table, clearly show the states of the PMOS and NMOS transistors for each of the following regions of the CMOS inverter characteristics. Consider V_{in} = input voltage, V_{tn} = threshold voltage of the NMOS, V_{DD} = supply voltage and V_{tp} = threshold voltage of the PMOS.

Region A: $0 \leq V_{in} < V_{tn}$,
Region B: $V_{tn} \leq V_{in} < V_{DD}/2$,
Region C: $V_{in} = V_{DD}/2$,
Region D: $V_{DD}/2 < V_{in} \leq V_{DD} - |V_{tp}|$, and
Region E: $V_{in} > V_{DD} - |V_{tp}|$.

(8 marks)

(ii) For Regions B, C and D draw the equivalent circuit model for the CMOS inverter and clearly show the direction of currents in each case.

(6 marks)

(b) For an NMOS transistor having width (W) = 3.6 μm, channel length (L) = 1.2 μm, derive the value of transconductance (g_m) when it operates in the linear region and the saturation region of its DC characteristic (where applicable) using the following parameters:

Carrier mobility (μ) = 500 cm^2/V-sec
Permittivity of silicon dioxide (ε) = 30.975×10^{-14} F/cm
Oxide thickness (t_{ox}) = 200×10^{-8} cm
Drain voltage (V_D) = 5 V
Gate voltage (V_G) = 4 V
Threshold voltage = 0.8 V
Source voltage (V_S) = 0 V

(6 marks)

(c) Through appropriate circuit diagram and mathematical analysis show that for a step input to a CMOS inverter, the fall time (t_f) can be given by the following expression

$$t_f = 2\frac{C_L}{\beta_n V_{DD}(1-n)}\left[\frac{(n-0.1)}{1-n}+\frac{1}{2}\ln(19-20n)\right]\approx k\frac{C_L}{\beta_n V_{DD}}$$

where, C_L is the load capacitance, $n = V_{tn}/V_{DD}$, V_{tn} is the threshold voltage of the NMOS transistor and β_n is the process gain factor for the NMOS.

(*8 marks*)

(d) Considering the carrier mobility for PMOS is three times lower than the carrier mobility in NMOS, show that the rise and fall time of a 3-input NAND gate is approximately equal when using transistors of equal size (i. e., both PMOS and NMOS have equal width and length).

(5 marks)

5.

(a) (i) State Moore's Law?

What factors might cause Moore's law to fail in future?

(5 marks)

(ii) Draw transistor level circuit diagrams for CMOS and NMOS 3-input NAND gates.

Explain what features of CMOS make it more suitable than NMOS for VLSI design.

(5 marks)

(iii) Explain the term ***self-aligned*** as it applies to MOS transistor construction. Illustrate your answer with appropriate mask level and cross sectional diagrams.

(6 marks)

(b) (i) Explain the general principle of operation of a dynamic logic inverter designed in pull-down topology.

(4 marks)

(ii) What are the advantages and disadvantages of a dynamic logic circuit? Explain with circuit diagram (wherever appropriate) how can the disadvantages be handled?

(9 marks)

(iii) Realise the dynamic logic circuit for the following logic function:

$$Y = \overline{(A.B + C.D).E}$$

Where A, B, C, D and E are the inputs to the circuit.

(4 marks)

END OF PAPER