UNIVERSITY OF SOUTHAMPTON ELEC3025W1

SEMESTER 1 EXAMINATIONS 2008/09

INTEGRATED CIRCUIT DESIGN

Duration: 120 min

Answer THREE out of FIVE questions.

University approved calculators MAY be used.

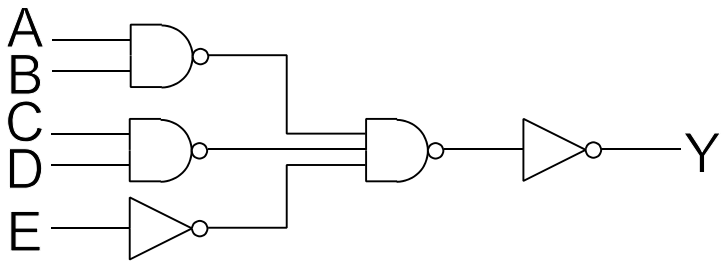
Coloured pens/pencils will be required.

Design rules for a sample CMOS process will be provided.

Graph paper will be available.

Number of Pages: 6

1.
The following circuit is to be implemented in static CMOS logic



(a) Derive a *stick diagram* for the implementation of each of the following basic gates

(i) inverter

(i) 2 input NAND gate

(ii) 3 input NAND gate

Your designs should be suitable for use as standard cells for a CMOS process which supports multiple metal layers (please state whether you design is aimed at a two metal layer process or a three metal layer process).

(9 marks)

(b) Explain the purpose of a *black box* or *abstract* view in the standard cell design process. Illustrate your answer with abstract views for each of the standard cells you have designed.

(5 marks)

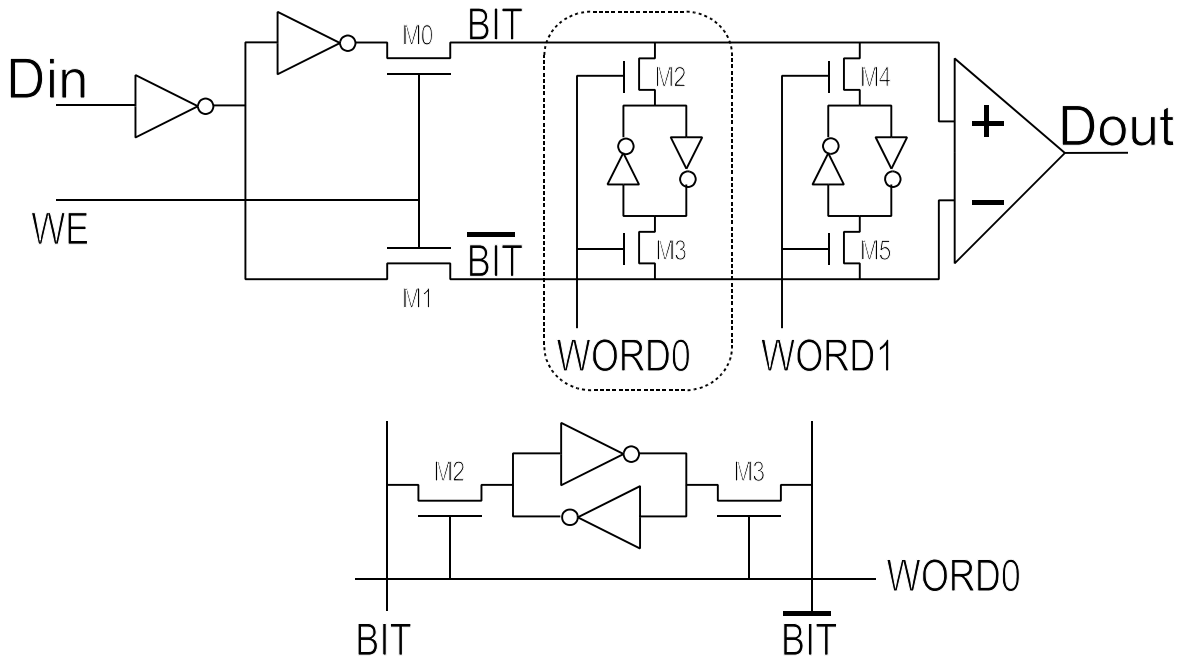
(c) Derive a stick diagram for the full circuit above based on the abstract views you have drawn.

(5 marks)

(d) Derive a boolean equation for Y in terms of A, B, C, D and E. Hence or otherwise derive a stick diagram for an alternative static CMOS implementation of this equation which uses fewer transistors.

(14 marks)

2.
The following figure shows the circuit for a small SRAM together with an enlarged view of one of the 6 transistor SRAM cells:



(a) Explain the operation of the complete SRAM circuit during

(i) a read operation

(ii) a write operation

Be sure to mention any conflict that may occur during read or write. Explain how the relative strengths of the transistors affect the resolution of any conflict. *(12 marks)*

(b) Derive a suitable *stick diagram* for the efficient layout of the six transistor SRAM cell using a process which supports only one metal layer. *(8 marks)*

(c) Based on your stick diagram and the sample 0.4µm CMOS design rules provided, sketch a 0.4µm *mask level layout* for the six transistor SRAM cell. You should assume that all transistors within the cell have a gate length of 0.4µm and a gate width of 1.0µm.

Your sketch need not be to scale. *(13 marks)*

3.

(a) For each of the following logic families draw a *transistor level circuit diagram* of a 3 input NOR gate and briefly describe its operation:

(i) Resistor Transistor Logic (RTL)

(ii) NMOS Logic

(iii) Static CMOS Logic

What are the advantages of CMOS for VLSI design compared to the older RTL and NMOS technologies.

(9 marks)

(b) Draw a *transistor level circuit diagram* for a 3 input NOR gate using pseudo-NMOS logic and briefly explain its operation. Discuss the usefulness of pseudo-NMOS NOR gates within a CMOS system design.

(7 marks)

(c) Realize the following logic functions using CPL logic:

(i) AND/NAND
(ii) OR/NOR

(4 marks)

Explain the general principle of operation of a dynamic logic inverter designed in pull-down topology.

(4 marks)

What are the advantages and disadvantages of a dynamic logic circuit? Explain with circuit diagrams (wherever appropriate) how can the disadvantages be handled?

(9 marks)