UNIVERSITY OF SOUTHAMPTON ELEC3025W1

SEMESTER 1 EXAMINATIONS 2006/07

INTEGRATED CIRCUIT DESIGN

Duration: 120 min

Answer THREE out of FIVE questions.

University approved calculators MAY be used.

Coloured pens/pencils will be required.

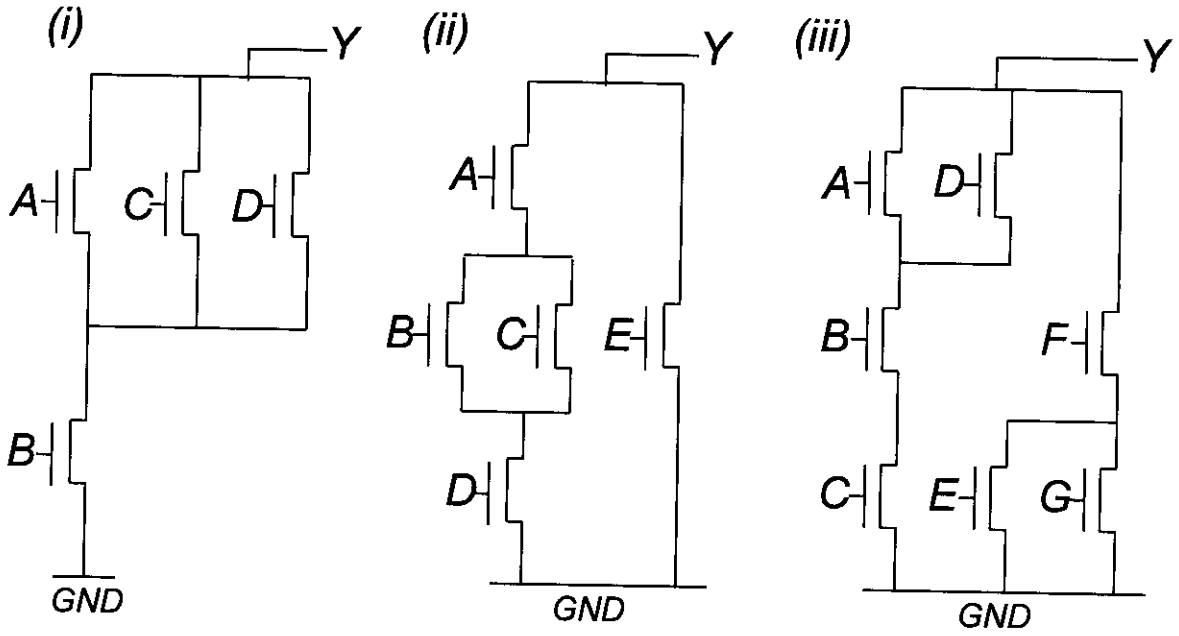
Design rules for a sample CMOS process will be provided.

Graph paper will be available.

Number of Pages: 8

1.

The Pull Down Networks (PDNs) for three static CMOS complementary gates are shown below:



For EACH gate:

(a) Derive a Boolean expression for the gate.

(6 marks)

(b) Design a suitable Pull Up Network (PUN) to complete the gate.

(6 marks)

(c) Find an Euler path for the gate if such a path exists.
Note that you may need to re-arrange the transistors within the schematic in order to find an Euler path.

(10 marks)

(d) Derive a suitable stick diagram for efficient layout of the gate using a CMOS process supporting only one metal layer.

(11 marks)

2.

(a) Briefly describe, with the aid of suitable diagrams, the stages involved in producing a PMOS transistor for a CMOS process. You should relate your answer to the masks listed in the sample design rules provided with this exam paper.

(13 marks)

(b) Figure 2 below is a stick diagram for a 2 input NAND gate which is to be realized in 0.3μm CMOS (based on the sample design rules provided):

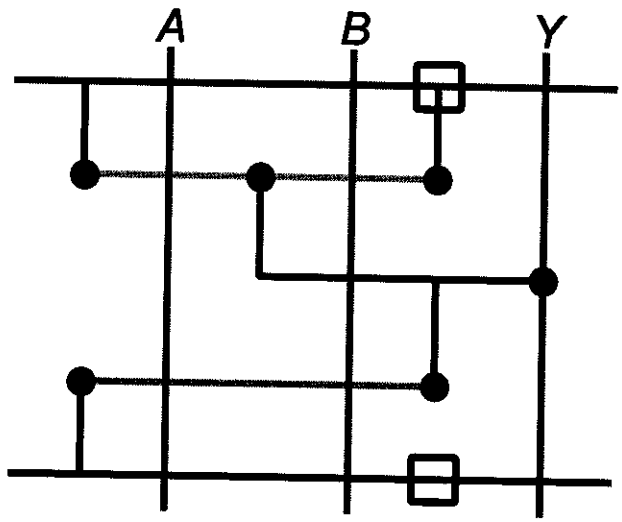


Figure 2 (A colour version of this figure can be found on a sheet accompanying this paper)

Sketch a complete mask level layout for this gate given that the power rails are $1.0\mu m$ in width and the transistor dimensions are as follows:

$$L_p = 0.3\mu m, \quad W_p = 1.4\mu m$$
$$L_n = 0.3\mu m, \quad W_n = 1.0\mu m$$

Your sketch need not be to scale.

From your sketch, derive the height of your NAND gate.
You should give your working and justify any assumptions that you make.

(20 marks)

3.

(a) Show that the rise-time of the inverter of Figure (3.i) is given by:

$$\frac{2C_L V_{dd}}{\mu_p C_{ox} \frac{W_p}{L_p}\left(V_{dd} + V_{tp}\right)^2}$$

Where;
μ_p = hole mobility, C_{ox} = gate capacitance/unit area,
V_{tp} = PMOS-transistor threshold voltage

Clearly state any assumptions made during the derivation of the inverter rise-time equation.

(6 marks)

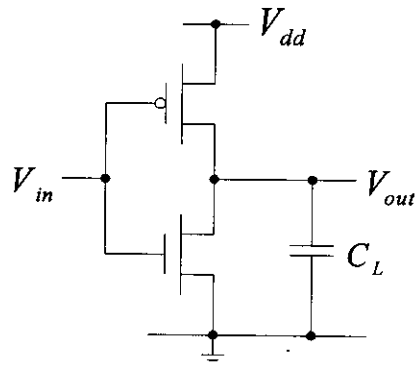


Figure (3.i)

(b) Assume 0.13μm CMOS technology with minimum active area width = 0.2μm; estimate the transistor dimensions (W/L) to obtain minimum-size inverter design? If $V_{tp} = -0.5V$, $\mu_p C_{ox} = 90\mu A/V^2$, $V_{dd} = 1.2V$, $C_L = 2pF$ and the propagation delay = 55ns, work-out the inverter fall-time.

(5 marks)

(c) With the help of a circuit diagram and suitable transistor sizing, suggest one method to reduce the inverter rise-time.

(3 marks)

Question 3 continued on next page

(d) Assume a symmetrical inverter CMOS design as reference, where $(W/L)_n = 0.5/0.35$, $(W/L)_p = 1.5/0.35$, and using partition design style with 2-input and 3-input combinational gates, produce the gate-level schematic of an 8-input AND gate (a0,a1,a2,a3,a4,a5,a6,a7). Estimate the silicon area of the gate.

(13 marks)

(e) With the help of a circuit diagram, briefly explain three disadvantages associated with designing high-input combinational gates using single-gate design approach.

(6 marks)

4.

(a) Derive the expression for the average dynamic power dissipation for a square wave input in a symmetric inverter by clearly stating all the assumptions you are making.

(6 marks)

(b) Consider the circuit shown in Figure (4.ii). Calculate the average dynamic power consumption of the circuit by considering that the primary inputs are independent and uniformly distributed. Use the following data:

Delay of XOR, OR and NOR gates are 12ns, 5ns and 8ns respectively and the set up time of the register R is 0.2ns. Lumped capacitance at the X, Y and Z are 20pF, 16pF and 8pF respectively. The supply voltage is 3V.

(14 marks)

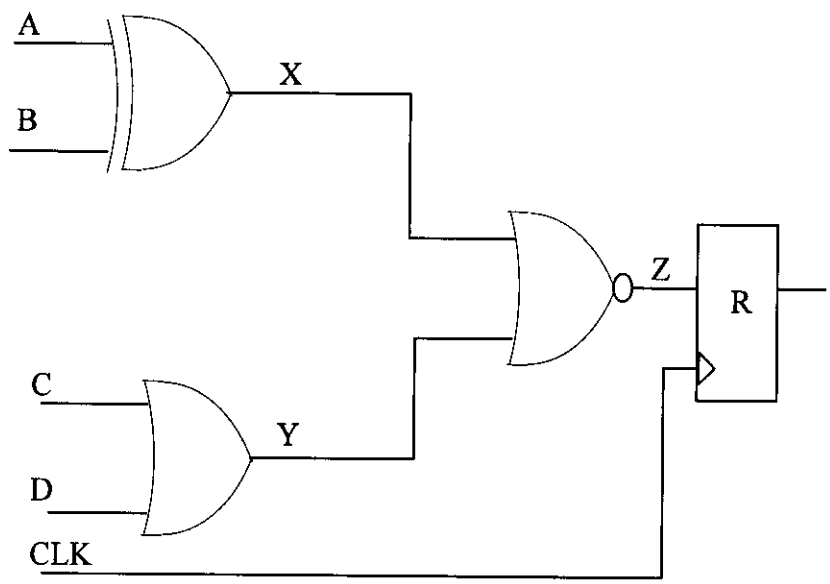


Figure (4.ii)

(c) A symmetric inverter shows the input-output pattern as shown in Figure 4(iii). Sketch the pattern of current drawn from the power supply and the short circuit current by clearly stating the reason for their behaviour.

(7 marks)

Question 4 continued on next page

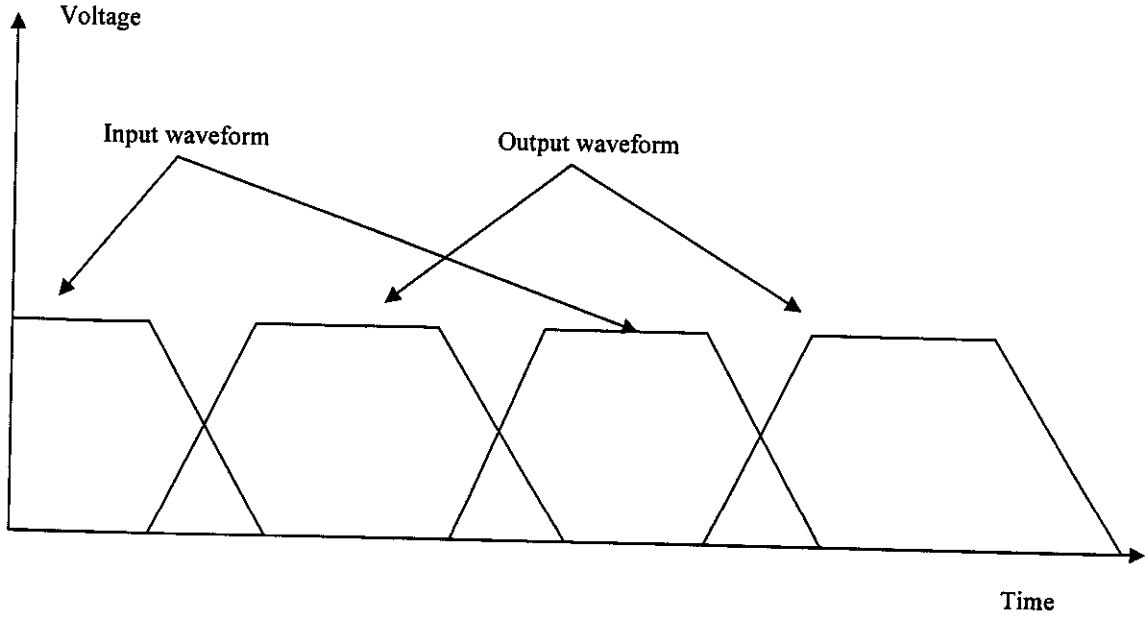


Figure 4(iii)

(d) What are the two major components for leakage power dissipation and what are their origins? What are the process level and circuit level parameters one can use to control leakage?

(6 marks)

5.

(a) Although it is possible to build CMOS systems using only static complementary gates, there are circumstances where alternative circuit construction styles offer advantages.

For each of the following circuits, draw a circuit diagram and briefly describe its operation:

(i) A pseudo-NMOS NOR gate.

(ii) A transparent latch built around a multiplexor based on either transmission gates or tristate inverters.

(iii) A six transistor SRAM cell.

In each case discuss the usefulness of the circuit within a CMOS system design.

(17 marks)

(b) (i) Explain the general principle of operation of a dynamic logic inverter designed in pull-down topology.

(4 marks)

(ii) What are the advantages and disadvantages of a dynamic logic circuit? Explain with circuit diagrams (wherever appropriate) how the disadvantages can be overcome?

(9 marks)

(iii) Realize the dynamic logic circuit for the following logic function:

$$Y = \overline{(AB + CD).E}$$

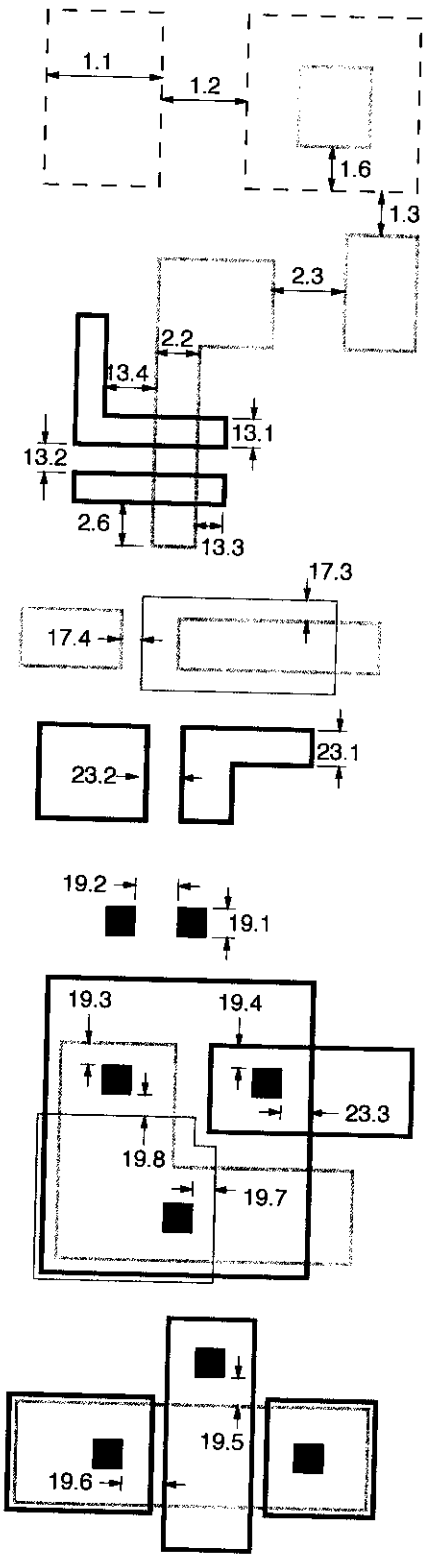
Where A, B, C, D and E are the inputs to the circuit.

(3 marks)

END OF PAPER

ELEC3025 Sample Design Rules

Simplified Design Rules for a 0.3um CMOS process



Design Rule		Distance (microns)
N-well		
1.1	Minimum n-well width	2.0
1.2	Minimum n-well spacing	1.0
1.3	Minimum n-well spacing to active area	1.0
1.6	Minimum n-well enclosure of active area	1.0
Active Area		
2.2	Minimum active area width	0.5
2.3	Minimum active area spacing	0.6
2.6	Minimum source/drain length	0.5
Polysilicon		
13.1	Minimum polysilicon width	0.3
13.2	Minimum polysilicon spacing	0.5
13.3	Minimum polysilicon extension beyond gate	0.5
13.4	Minimum polysilicon spacing to active area	0.1
P implant		
17.3	Minimum p implant enclosure of active area	0.3
17.4	Minimum p implant spacing to active area	0.3
Metal 1		
23.1	Minimum metal 1 width	0.5
23.2	Minimum metal 1 spacing	0.5
Contact Window		
19.1	Minimum/maximum contact dimension	0.3
19.2	Minimum contact spacing	0.6
19.3	Minimum active area enclosure of contact	0.3
19.4	Minimum polysilicon enclosure of contact	0.3
19.7	Minimum p implant enclosure of contact	0.2
19.8	Minimum p implant spacing to contact	0.2
23.3	Minimum metal 1 enclosure of contact	0.2
19.5	Minimum polysilicon contact spacing to active area	0.4
19.6	Minimum active area contact spacing to polysilicon gate	0.4

* This is not a complete set of design rules but is sufficient for most simple cell designs *

ELEC3025 Figure 2