UNIVERSITY OF SOUTHAMPTON ELEC3025W1

SEMESTER 1 EXAMINATIONS 2007/08

INTEGRATED CIRCUIT DESIGN

Duration: 120 min

Answer THREE out of FIVE questions.

University approved calculators MAY be used.

Coloured pens/pencils will be required.

Design rules for a sample CMOS process will be provided.

Graph paper will be available.

Number of Pages: 8

1.

(a) Draw a stick diagram of a 2 input NOR gate for implementation using a CMOS process supporting only one metal layer.

(4 marks)

(b) Sketch a mask level layout for this NOR gate based on the masks shown on the sample design rules provided. *Your sketch need not be to scale*.

(8 marks)

(c) Explain the construction of the PMOS transistors in this gate based on the masks you have drawn. Illustrate your answer with a diagram showing a cross section through the two PMOS transistors.

(8 marks)

(d) The following Boolean function is to be realized as a static CMOS complementary gate:

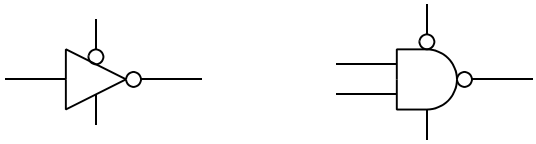
$$Y = \overline{(A + B.C) \; . \; D}$$

(i) Derive a suitable transistor level circuit diagram for this gate.

(ii) Derive a stick diagram for this gate, based on an investigation of possible Euler paths. Your design should be targeted at a CMOS process supporting only one metal layer.

(13 marks)

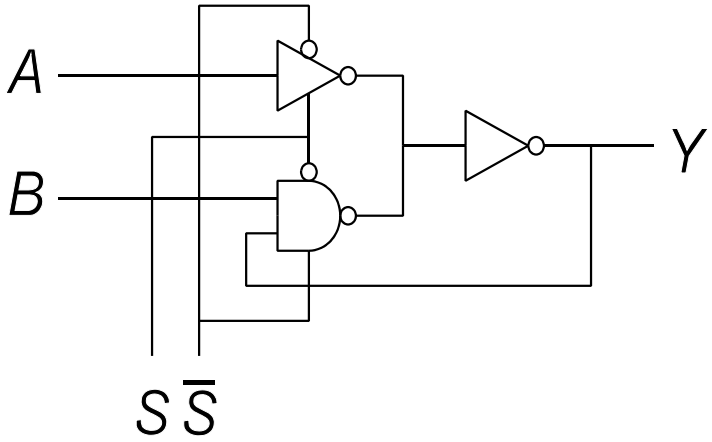
2. The symbols below represent a CMOS inverter and a CMOS NAND gate each with a tristate output:



(a) For each of these gates derive a suitable transistor level circuit diagram. *(5 marks)*

(b) Explain how tristate inverters may be used to facilitate bus connections between multiple functional units on an integrated circuit. What advantages do tristate inverters offer over transmission gates for this task? *(6 marks)*

(c) The following circuit may be used in the construction of a master slave flip-flop.



(i) Derive a transistor level circuit diagram for this circuit.

(ii) Derive a stick diagram for efficient layout of this circuit. You may use either one or two metal layers in your design. *(14 marks)*

(d) Explain the function of the input labelled B in the context of a master slave flip-flop constructed using this circuit. Draw a gate level circuit diagram to illustrate your answer.

There is a potential problem with the operation of the B input in the master slave flip-flop. If possible identify the problem and suggest a solution. *(8 marks)*

5.

(a) (i) Derive a stick diagram for the layout of a 2-input AND gate based on static CMOS logic. The layout should be suitable for use as a standard cell for a CMOS process that supports just one metal layer.

(5 marks)

(ii) Redesign your gate for use as a standard cell for a CMOS process that supports two metal layers. What is the advantage of this approach over the one metal design?

(4 marks)

(iii) Redesign your gate for use as a standard cell for a CMOS process that supports three metal layers. What is the advantage of this approach over the two metal design?

(3 marks)

(iv) Draw *black box* or *abstract* views of each of these designs. What purpose do these views have in the standard cell design process?

(5 marks)

(b) Realise the following logic functions using CPL logic:

(i) AND/NAND
(ii) OR/NOR
(iii) XOR/XNOR

(6 marks)

(c) (i) You have 12 transmission gates connected in series. If each of the transmission gates has an "ON" resistance = 20 Ω and output capacitance = 4 pF then what will be the rise time of entire arrangement when all the transmission gates are "ON"?

(5 marks)

(ii) If you insert a buffer at every 3rd position of this chain of transmission gates and if each buffer has a delay of 100 ps then what will be rise time of this arrangement?

(5 marks)

END OF PAPER