UNIVERSITY OF SOUTHAMPTON ELEC3025W1

SEMESTER 1 EXAMINATIONS 2006/07

INTEGRATED CIRCUIT DESIGN

Duration: 120 min

Answer THREE out of FIVE questions.

University approved calculators MAY be used.

Coloured pens/pencils will be required.

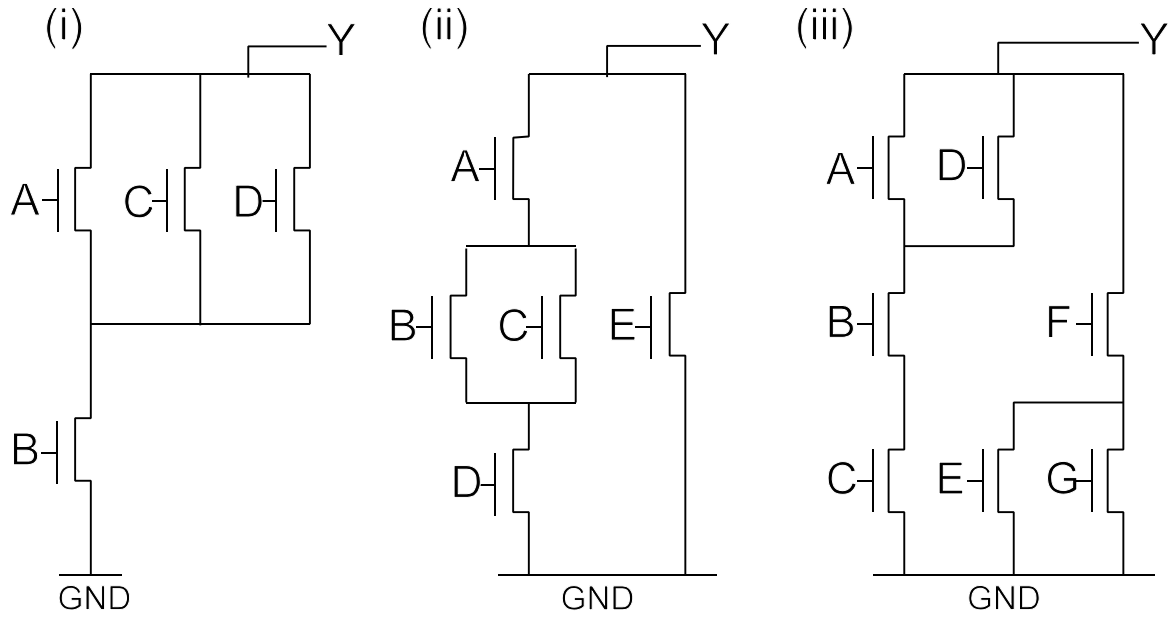
Design rules for a sample CMOS process will be provided.

Graph paper will be available.

Number of Pages: 8

1.

The Pull Down Networks (PDNs) for three static CMOS complementary gates are shown below:



For EACH gate:

(a) Derive a Boolean expression for the gate.

(6 marks)

(b) Design a suitable Pull Up Network (PUN) to complete the gate.

(6 marks)

(c) Find an Euler path for the gate if such a path exists.
Note that you may need to re-arrange the transistors within the schematic in order to find an Euler path.

(10 marks)

(d) Derive a suitable stick diagram for efficient layout of the gate using a CMOS process supporting only one metal layer.

(11 marks)

2.

(a) Briefly describe, with the aid of suitable diagrams, the stages involved in producing a PMOS transistor for a CMOS process.
You should relate your answer to the masks listed in the sample design rules provided with this exam paper.

(13 marks)

(b) Figure 2 below is a stick diagram for a 2 input NAND gate which is to be realized in 0.3µm CMOS (based on the sample design rules provided):

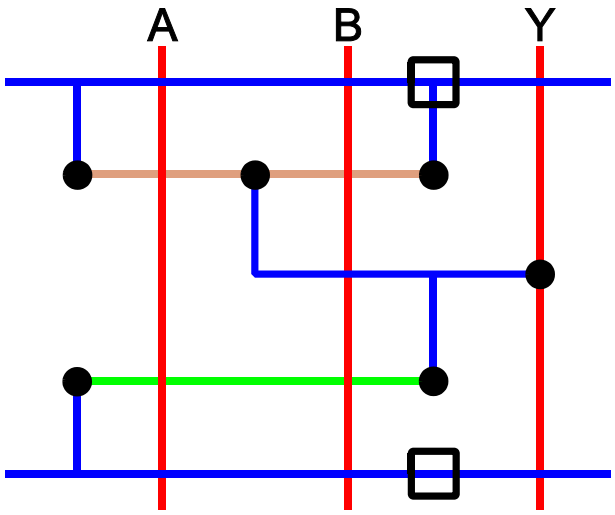


Figure 2 (A colour version of this figure can be found on a sheet accompanying this paper)

Sketch a complete mask level layout for this gate given that the power rails are $1.0\mu m$ in width and the transistor dimensions are as follows:

$$L_p = 0.3\mu m, \quad W_p = 1.4\mu m$$
$$L_n = 0.3\mu m, \quad W_n = 1.0\mu m$$

Your sketch need not be to scale.

From your sketch, derive the height of your NAND gate.
You should give your working and justify any assumptions that you make.

(20 marks)

5.

(a) Although it is possible to build CMOS systems using only static complementary gates, there are circumstances where alternative circuit construction styles offer advantages.

For each of the following circuits, draw a circuit diagram and briefly describe its operation:

(i) A pseudo-NMOS NOR gate.

(ii) A transparent latch built around a multiplexor based on either transmission gates or tristate inverters.

(iii) A six transistor SRAM cell.

In each case discuss the usefulness of the circuit within a CMOS system design.

(17 marks)

(b) (i) Explain the general principle of operation of a dynamic logic inverter designed in pull-down topology.

(4 marks)

(ii) What are the advantages and disadvantages of a dynamic logic circuit? Explain with circuit diagram (wherever appropriate) how can the disadvantages be handled?

(9 marks)

(iii) Realize the dynamic logic circuit for the following logic function:

$$Y = \overline{(AB + CD).E}$$

Where A, B, C, D and E are the inputs to the circuit.

(3 marks)

END OF PAPER