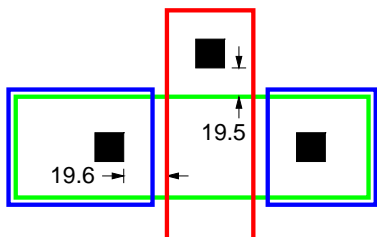
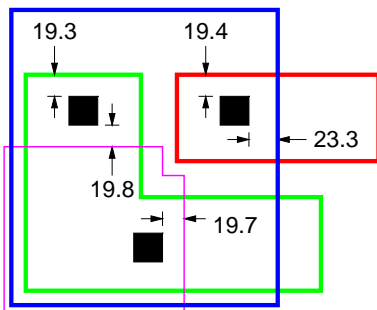
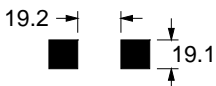
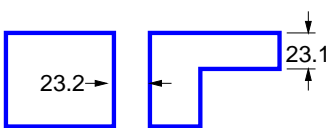
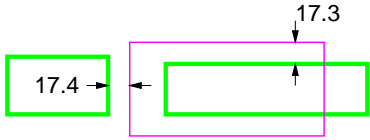
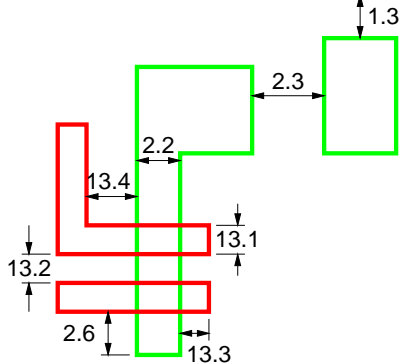
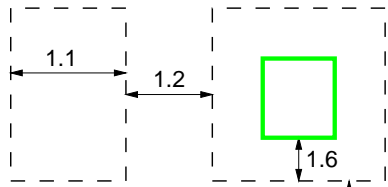


# ELEC3025 Sample Design Rules

## Simplified Design Rules for a 0.4um CMOS process

Design Rule	Distance (microns)
<b>N-well</b>	
1.1 Minimum n-well width	2.4
1.2 Minimum n-well spacing	1.2
1.3 Minimum n-well spacing to active area	1.2
1.6 Minimum n-well enclosure of active area	1.2
<b>Active Area</b>	
2.2 Minimum active area width	0.6
2.3 Minimum active area spacing	0.8
2.6 Minimum source/drain length	0.6
<b>Polysilicon</b>	
13.1 Minimum polysilicon width	0.4
13.2 Minimum polysilicon spacing	0.6
13.3 Minimum polysilicon extension beyond gate	0.6
13.4 Minimum polysilicon spacing to active area	0.2
<b>P implant</b>	
17.3 Minimum p implant enclosure of active area	0.4
17.4 Minimum p implant spacing to active area	0.4
<b>Metal 1</b>	
23.1 Minimum metal 1 width	0.6
23.2 Minimum metal 1 spacing	0.6
<b>Contact Window</b>	
19.1 Minimum/maximum contact dimension	0.4
19.2 Minimum contact spacing	0.6
19.3 Minimum active area enclosure of contact	0.3
19.4 Minimum polysilicon enclosure of contact	0.3
19.7 Minimum p implant enclosure of contact	0.2
19.8 Minimum p implant spacing to contact	0.2
23.3 Minimum metal 1 enclosure of contact	0.2
19.5 Minimum polysilicon contact spacing to active area	0.4
19.6 Minimum active area contact spacing to polysilicon gate	0.4



\* This is not a complete set of design rules but is sufficient for most simple cell designs \*