UNIVERSITY OF SOUTHAMPTON ELEC3025W1

SEMESTER 1 EXAMINATIONS 2005/06

INTEGRATED CIRCUIT DESIGN

Duration: 120 min

Answer THREE out of FIVE questions.

University approved calculators MAY be used.

Coloured pens/pencils will be required.

Design rules for a sample CMOS process will be provided.

Graph paper will be available.

Number of Pages: 8

1.

(a) Discuss the advantages of semi-custom standard cell integrated circuit design when compared to:

(i) Field Programmable Gate Array (FPGA) design.
(ii) Full custom design.

(8 marks)

(b) Describe the layout of a chip that employs standard cell design and hence derive a simple set of requirements for a standard cell library for a CMOS process supporting two metal layers.

(8 marks)

(c) The following Boolean function is to be realized as a static CMOS complementary gate:

$$Y = \overline{A.B+(C+D).(E+F)}$$

(i) Derive a suitable transistor level circuit diagram for this gate.

(ii) Derive a stick diagram for this gate, based on an investigation of possible Euler paths. Your design should be suitable for use as a standard cell for a CMOS process supporting two metal layers.

(17 marks)

2. (a) Any Boolean function may be expressed in *Sum Of Products* (SOP) form and hence implemented using only two levels of logic (a first level using AND gates and a second level using OR gates) provided that inverted and non-inverted inputs are available.

Derive an implementation for each of the Boolean functions:

$$X = \overline{A} + B.(C + D)$$
$$Y = \overline{A.(B + C)}$$
$$Z = B \oplus \overline{C}$$

using two levels of logic (AND and OR gates).

You may assume the availability of inverted inputs.

(11 marks)

(b) A CMOS PLA employs *Pseudo-NMOS* NOR gates and inverters in order to implement sets of SOP expressions.

(i) Draw a transistor level schematic diagram of a *Pseudo-NMOS* NOR gate and briefly describe its operation.

(ii) Explain how *Pseudo-NMOS* NOR gates are used in the AND and OR planes of a PLA. Illustrate your answer with a gate level schematic diagram of a PLA to implement the Boolean functions:

$$X = \overline{A} + B.(C + D)$$
$$Y = \overline{A.(B + C)}$$
$$Z = B \oplus \overline{C}$$

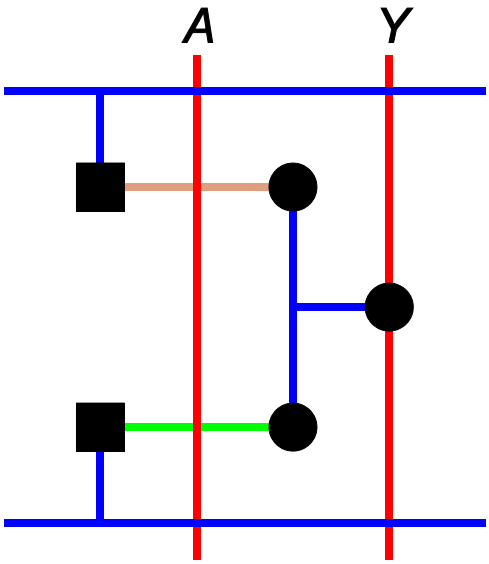
(iii) Draw a stick diagram layout of the AND plane of the PLA described in part (ii).

You may assume the availability of inverted inputs.

(22 marks)

4.

(a) The figure below is a stick diagram for an inverter which is to be realized in 0.4µm CMOS (based on the sample design rules provided):



(i) Sketch a *mask level layout* for the NMOS transistor from this gate including the source, drain and substrate contacts, given the following transistor dimensions:

$$W_n = 1.2\mu m$$
$$L_n = 0.4\mu m$$

Your sketch need not be to scale.

(ii) From your sketch, derive the chip area occupied by the NMOS transistor including contacts and the ratio of this area to the area of the transistor without contacts.
You should give your working and justify any assumptions that you make.

(iii) In the light of this calculation, discuss the benefits of employing Euler paths in cell design.

(15 marks)

Question 4 continued on next page