UNIVERSITY OF SOUTHAMPTON ELEC3025A

SEMESTER 1 EXAMINATIONS 2004/05

INTEGRATED CIRCUIT DESIGN

Duration: 120 min

Answer THREE out of FIVE questions.

University approved calculators MAY be used.

Coloured pens/pencils will be required.

Design rules for a sample CMOS process will be provided.

Graph paper will be available.

Number of Pages: 9

1.

(a) (i) Which of the following Boolean functions may be implemented as a single static CMOS complementary gate?

$$Y = A + B$$
$$Y = \overline{A.B}$$
$$Y = \overline{A \oplus B}$$
$$Y = \overline{A.B + C.D}$$
$$Y = \overline{A.B}.\overline{C}.\overline{D.E}$$

Where such an implementation is possible, derive a suitable transistor level circuit diagram.

(ii) Define the set of Boolean functions which may be realized as single static CMOS complementary gates.

(15 marks)

(b) The following Boolean function is to be realized in static CMOS logic:

$$Y = \overline{(A.B + C).D + E}$$

(i) Derive a suitable transistor level circuit diagram for this gate.

(ii) Derive a stick diagram for this gate, based on an investigation of possible Euler paths.

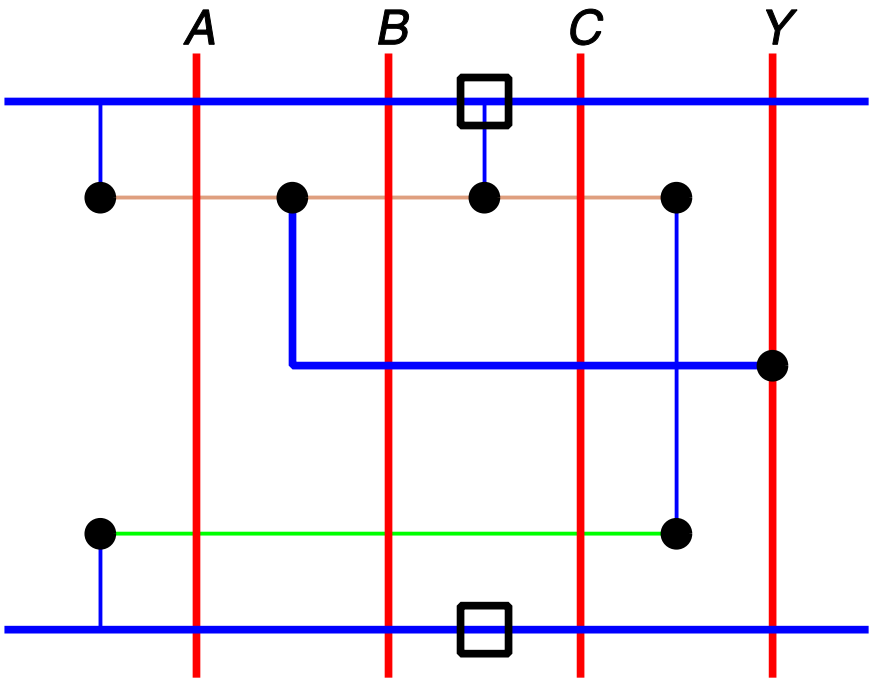
(18 marks)

2.

(a) Briefly describe, with the aid of suitable diagrams, the stages involved in producing a PMOS transistor for a CMOS process.
You should relate your answer to the masks listed in the sample design rules provided with this exam paper.

(13 marks)

(b) The figure below is a stick diagram for a 3 input NAND gate which is to be realized in 0.4µm CMOS (based on the sample design rules provided):



Sketch a complete mask level layout for this gate given the following transistor dimensions:

$$W_n = W_p = 1.0\mu m$$
$$L_n = L_p = 0.4\mu m$$

Your sketch need not be to scale.
From your sketch, derive the width of your NAND gate.
You should give your working and justify any assumptions that you make.

(20 marks)

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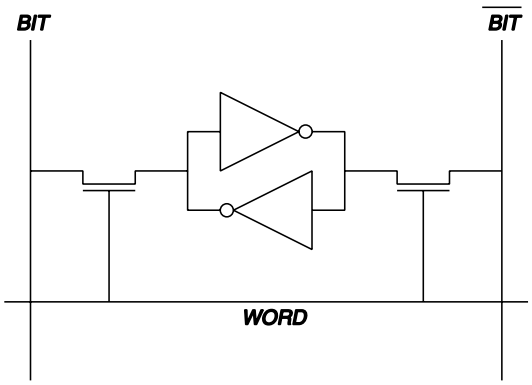
Question 5 continued

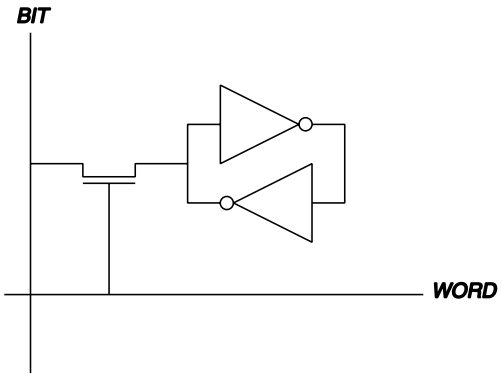
(b) (i) The following figure represents the circuit diagram of a 6 transistor static RAM cell:



Briefly explain the operation of this cell for both read and write operations. Be sure to mention any conflict that may occur during read or write.

(10 marks)

(ii) An alternative static RAM cell uses just 5 transistors:



Discuss the problems associated with using this 5 transistor cell when compared to the 6 transistor version. You should consider the resolution of conflicts during operation, the sizing of transistors, and the design of associated read and write circuitry.

(7 marks)

END OF PAPER