UNIVERSITY OF SOUTHAMPTON ELEC3025A

SEMESTER 1 EXAMINATIONS 2003/04

INTEGRATED CIRCUIT DESIGN

Duration: 120 min

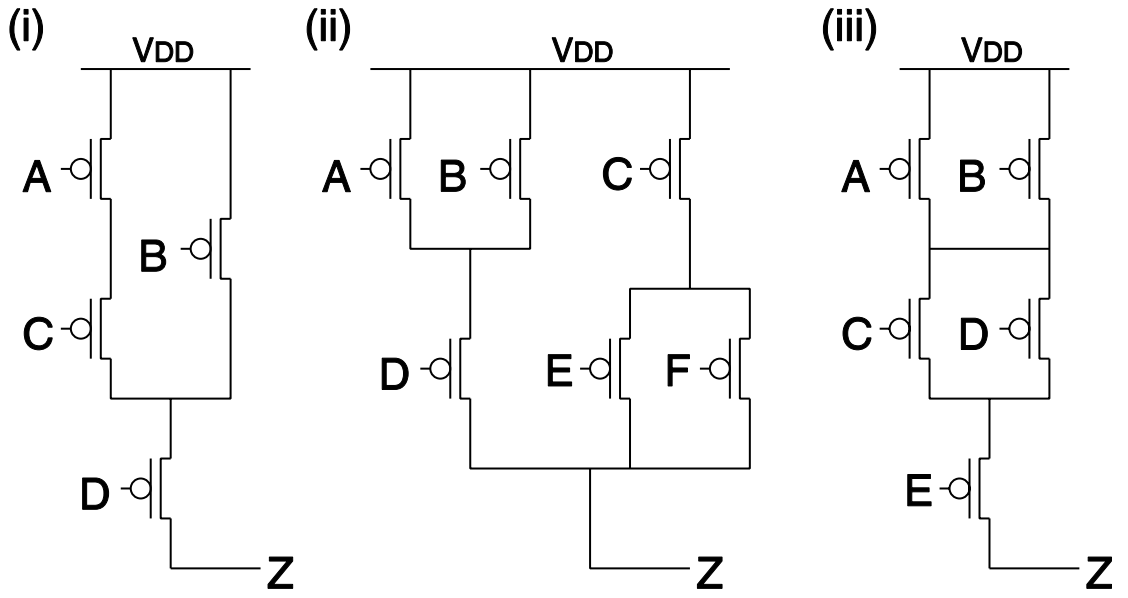
Answer THREE out of FIVE questions.

Calculators MAY be used, but not ones with text storage facilities.

Coloured pencils will be provided.

Number of Pages 8

1. The Pull Up Networks (PUNs) for three static CMOS complementary gates are shown below:



For EACH gate:

(a) Derive a Boolean expression for the gate.

(6 marks)

(b) Design a suitable Pull Down Network (PDN) to complete the gate.

(6 marks)

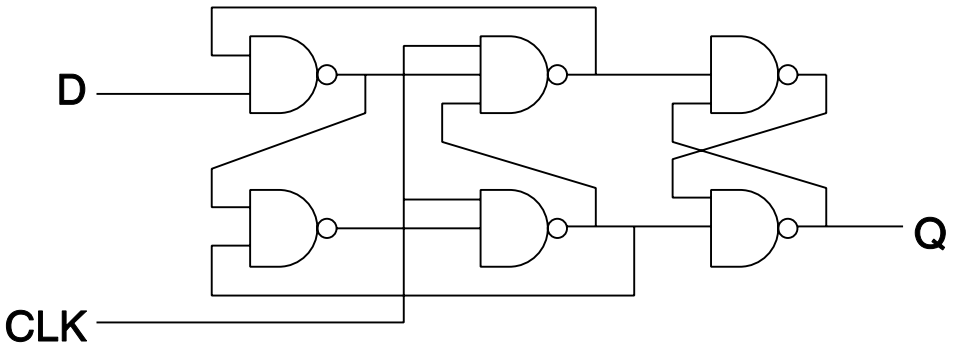
(c) Find an Euler path for the gate if such a path exists.
Note that you may need to re-arrange the transistors within the schematic in order to find an Euler path.

(10 marks)

(d) Derive a suitable stick diagram for efficient layout of the gate using a CMOS process supporting only one metal layer.

(11 marks)

2. (a)



By drawing sub-circuit schematics (or otherwise), calculate the number of transistors in the above edge triggered D-type flip flop.

(4 marks)

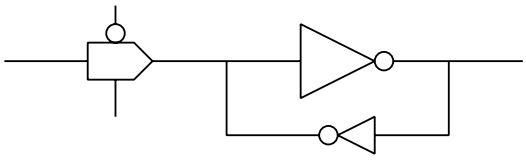
(b) A transparent latch may be built around a multiplexer based on either transmission gates or tristate inverters.
With reference to an appropriate circuit diagram, show that we can build a master slave D-type using two such latches which will have fewer transistors than the edge triggered D-type from part (a).

(8 marks)

(c) Derive a stick diagram for the layout of your chosen master slave D-type.

(12 marks)

(d) Discuss the operation of a D-type based on a *jamb latch* circuit such as shown below:



What are the benefits and drawbacks of this approach?

(9 marks)

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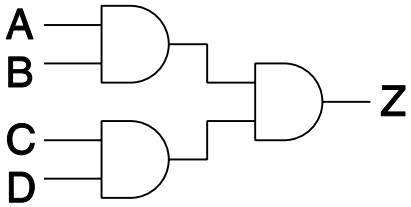
5. (a) Assume a symmetrical inverter CMOS design as reference, where $(W/L)_n=1/0.5$, $(W/L)_p=3/0.5$.

(i) Sketch the transistor level schematic of a 4-input (a,b,c,d) AND gate. Estimate the silicon area of the gate.

(6 marks)

(ii) An alternative implementation of a 4-input (a,b,c,d) AND gate is shown below:



Estimate the silicon area of this design.

(6 marks)

(iii) Compare the area and speed performance of the above two implementations of the 4-input AND gate.

(5 marks)

(b) (i) Derive a stick diagram for the layout of the 4-input AND gate designed in part (a)(i).
The layout should be suitable for use as a standard cell for a CMOS process that supports three metal layers.

(5 marks)

(ii) Draw a *black box* or *abstract* view of this gate as it might be supplied to an ASIC designer.
What other information is normally supplied with the *abstract* view to help the designer make use of the gate?

(4 marks)

(iii) Discuss with the aid of appropriate figures, the process of constructing a multi-cell layout based on these *abstract* views for a CMOS process that supports three metal layers.

(7 marks)

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