UNIVERSITY OF SOUTHAMPTON EL331W1

SEMESTER 1 EXAMINATIONS 2001/02

INTEGRATED CIRCUIT DESIGN

Duration: 120 min

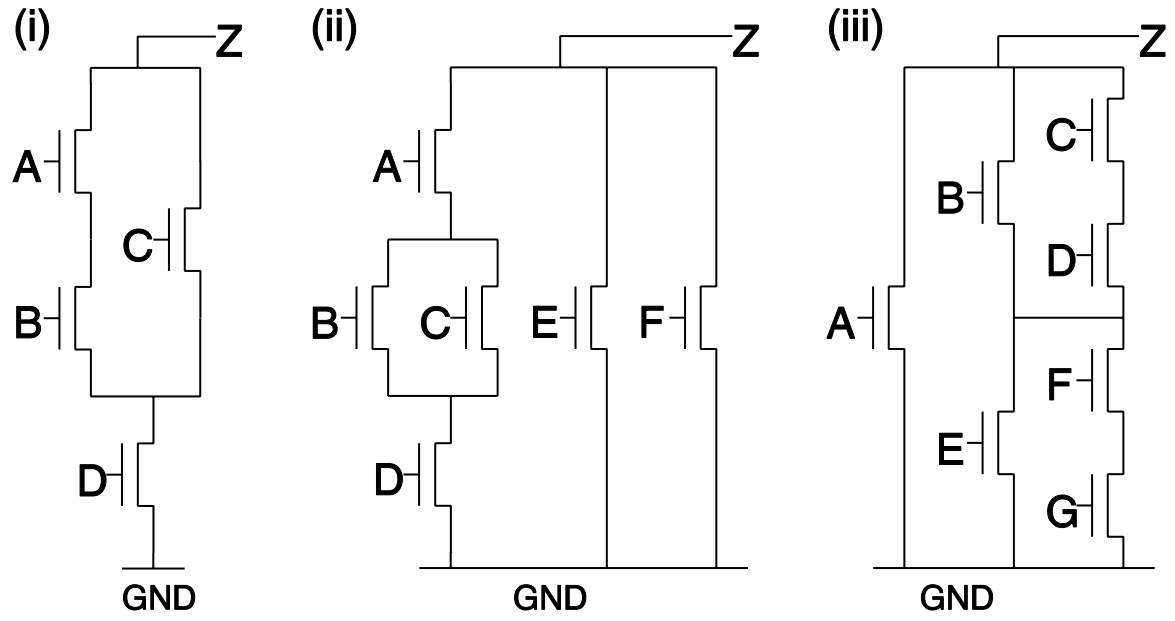
Answer THREE out of FIVE questions.

Calculators MAY be used, but not ones with text storage facilities.

Coloured pencils will be provided.

Number of Pages 8

1. The Pull Down Networks (PDNs) for three static CMOS complementary gates are shown below:



For EACH gate:

(a) Derive a Boolean expression for the gate.

(6 marks)

(b) Design a suitable Pull Up Network (PUN) to complete the gate.

(6 marks)

(c) Find an Euler path for the gate if such a path exists.
Note that you may need to re-arrange the transistors within the schematic in order to find an Euler path.

(10 marks)

(d) Derive a suitable stick diagram for efficient layout of the gate using a CMOS process supporting only one metal layer.

(11 marks)

2. (a) Any Boolean function may be expressed in *Sum Of Products* (SOP) form and hence implemented using only two levels of logic (a first level using AND gates and a second level using OR gates) provided that inverted and non-inverted inputs are available.

Derive an implementation for each of the Boolean functions:

$$X = A + \overline{B}.C.D + B.\overline{D}$$
$$Y = (B + \overline{C}).\overline{D}$$
$$Z = \overline{\overline{A}.(C + D)}$$

using two levels of logic (AND and OR gates).

You may assume the availability of inverted inputs.

(11 marks)

(b) A CMOS PLA employs *Pseudo-NMOS* NOR gates and inverters in order to implement sets of SOP expressions.

(i) Draw a transistor level schematic diagram of a *Pseudo-NMOS* NOR gate and briefly describe its operation.

(ii) Explain how *Pseudo-NMOS* NOR gates are used in the AND and OR planes of a PLA. Illustrate your answer with a gate level schematic diagram of a PLA to implement the Boolean functions:

$$X = A + \overline{B}.C.D + B.\overline{D}$$
$$Y = (B + \overline{C}).\overline{D}$$
$$Z = \overline{\overline{A}.(C + D)}$$

(iii) Draw a stick diagram layout of the AND plane of the PLA described in part (ii).

You may assume the availability of inverted inputs.

(22 marks)

5. (a) Produce a circuit schematic of an inverter gate using dynamic CMOS logic, and explain the gate operation.

(10 marks)

(b) Briefly discuss the two limitations of dynamic logic: charge leakage and charge sharing.

(6 marks)

(c) Describe the standard cell approach to ASIC design and the restrictions it imposes on the design of individual gates. Illustrate your answer with a stick diagram for the dynamic inverter, suitable for implementation as a standard cell using a CMOS process with two metal layers.

(10 marks)

(d) Re-design the gate for a CMOS process with three metal layers.
Explain how the use of three metal layers can be exploited to reduce circuit area.

(7 marks)

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