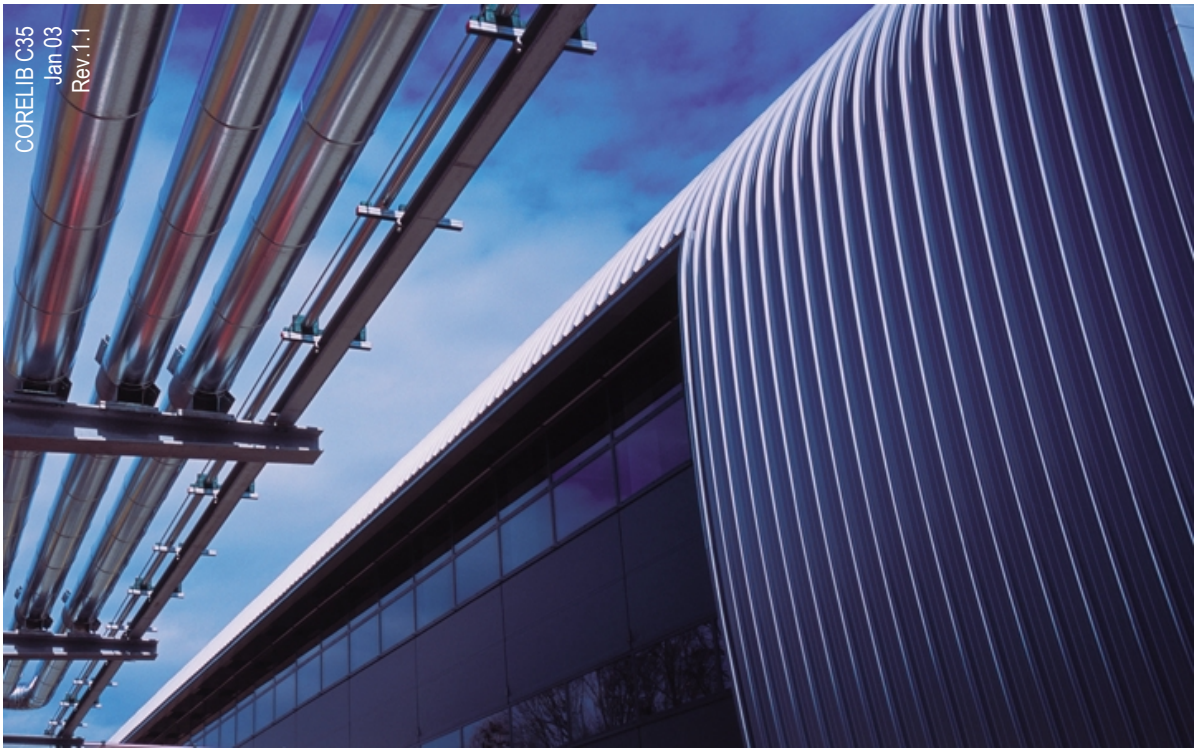
austriamicrosystems

0.35µm CMOS Digital Standard Cell Databook C35



The Company

For 20 years austriamicrosystems has specialized in developing and producing application-specific integrated circuits - ASICs - and application-specific standard products - ASSPs. It offers a broad range of customer solutions for the automotive, communications, industrial & medical markets. austriamicrosystems, whose headquarters are located near Graz/Austria, is one of the market leaders in mixed analog/digital ASICs.
austriamicrosystems offers a flexible interface according to its customers requirements and provides all elements of the value chain as a "one stop shop" for IC- and system solutions: R&D, design, process development, mask lithography, wafer production, assembly and testing. The company provides a wide range of semiconductor processes tailored to the customer's needs, such as HV-CMOS, BiCMOS, SiGe and CMOS in structural widths down to 0.35 µm.
In addition austriamicrosystems maintains design centres in Austria, Italy, Switzerland and USA and sales offices in Germany, France, Italy, Japan, Switzerland, UK and USA.

Customer focused

The company is organized into four distinct market and customer oriented business units: Automotive, Communications, Foundry, Industry & Medical. Taking its lead from clearly defined core objectives each business unit assumes full responsibility for sales, marketing and design for its customers.

Quality oriented

All quality assurance measures are based on ISO 9000. The company is certified according to ISO 9001 and QS9000/VDA6.1. austriamicrosystems has also been awarded the CECC 90000 certificate, the STACK Technical Approval for advanced quality management by STACK and the Q1-approval by Ford. The company commits itself to responsible, visionary environmental management. Based on this commitment austriamicrosystems has been one of the first semiconductor manufacturers certified in accordance with ISO 14001 and validated EMAS (Eco Management and Audit Scheme).

COT service

A unique feature of the company's technical capabilities is the COT (Customer Own Tooling) service for mixed signal circuits. These projects involve the customer carrying out the design of the circuit, whilst austriamicrosystems provides the "Design Kits". They consist of library elements, component models, process-specific parameters and interface files for the CAD software, all for very diverse design platforms. Depending on customer requirements the COT service package is completed by support in evaluation and ramp up of production. For these projects, customers have access to a broad range of high performance processes available.

A special service is provided to customers through the supply of so-called MPWs (Multi-Product Wafer runs). By combining several different chips on a wafer, the customer is offered a cheap entry to modern microelectronics. This is also of considerable interest to universities and research laboratories because it means they can try out the most advanced process technologies (e.g. SiGe-BiCMOS) at an early stage in their development.

Preface

This standard cell databook addresses logic and system designers developing application specific integrated circuits (ASICs). It contains information relevant to the austriamicrosystems standard cell families available for 0.35µm triple/four metal CMOS process technologies. Lowest power consumption, high speed, noise immunity and applicability to a wide range of automotive, communications, industrial & medical design requirements are the key benefits of this advanced process.

The digital standard cells can also be used together with the analog CMOS standard cells, which provides an optimum solution for mixed signal ASICs.

The 0.35 µm CMOS process family is a high-performance modular platform for complex deep submicron designs. austriamicrosystems' parallel support of advanced and mature process technologies guarantees long-term availability of the circuit. The variety of available process platforms enables the migration of products or product families with long life cycles to new technologies at a later stage. The functional equivalence of the cell libraries between the platforms provides the flexibility for an easier transfer of existing designs to new technologies.

All standard cells of the company are designed and supported in a way to provide a solid integration into the austriamicrosystems design environment. The integration of the cells with commonly used CAE/CAD tools is greatly simplified since the logical and physical characteristics of the library follow basic industry conventions.

The functions available in the cell libraries are optimized for the usage with synthesis tools. Timing-driven placement with in-place optimization is possible since all functions are available with different drive strengths.

The Core Cells are characterized for 3.3 Volts with nonlinear delays dependent on input slope and output load, which gives timing accuracy similar to a circuit simulator.

Two Periphery Cells libraries are available: One for use in pure 3.3V systems and one for mixed 3.3V/5V systems. The 3.3V / 5V library provides level shifting capabilities for 5V I/O and 3.3V core operation and requires separate supply voltages at both 3.3V and 5V.

The databook contains logic and timing information, cell area and a brief description of the austriamicrosystems standard cells.

Additional information can be retrieved from austriamicrosystems' website www.austriamicrosystems.com

N O T E S

Power Calculation

Power consumption figures for all cells are calculated under the following conditions:

Input slope = 1ns
Output load = 30 fF * drive strength for the core cells.
Output load = 2.5 pF * drive strength for the periphery cells.

The applied testpattern for power calculation covers all possible input combinations for combinatorial cells and therefore provides an averaging of power for all possible input patterns. Sequential cells are related to their clock-input signal. The values are given in µW and are related to a 1MHz toggling frequency. For other frequencies, the given number must be linearly scaled.

Modelling of Pull-Up/Pull-Down I/O Cells

When I/O cells with Pull-up or Pull-down function (e.g. BBCUxP and BBCDxP) are used in input mode with a high-impedance signal on the PAD pin they will always generate a logical 1 (pull-up) or logical 0 (pull-down) at the internal Y pin. This situation is however modelled in our Verilog and VHDL simulation with an X state at the output, this is shown in the truth-tables provided.

Definition of Rise/Fall Times

For all cells the following output transitions are defined as “Rise” or “Fall”. The transitions to/from a high-impedance “Z” state are only used for tri-state cells (e.g. BTx, ITx, BTxP, BUDDxP and BUDUxP).

Rise	Fall
$0 \rightarrow 1$	$1 \rightarrow 0$
$Z \rightarrow 1$	$Z \rightarrow 0$
$0 \rightarrow Z$	$1 \rightarrow Z$

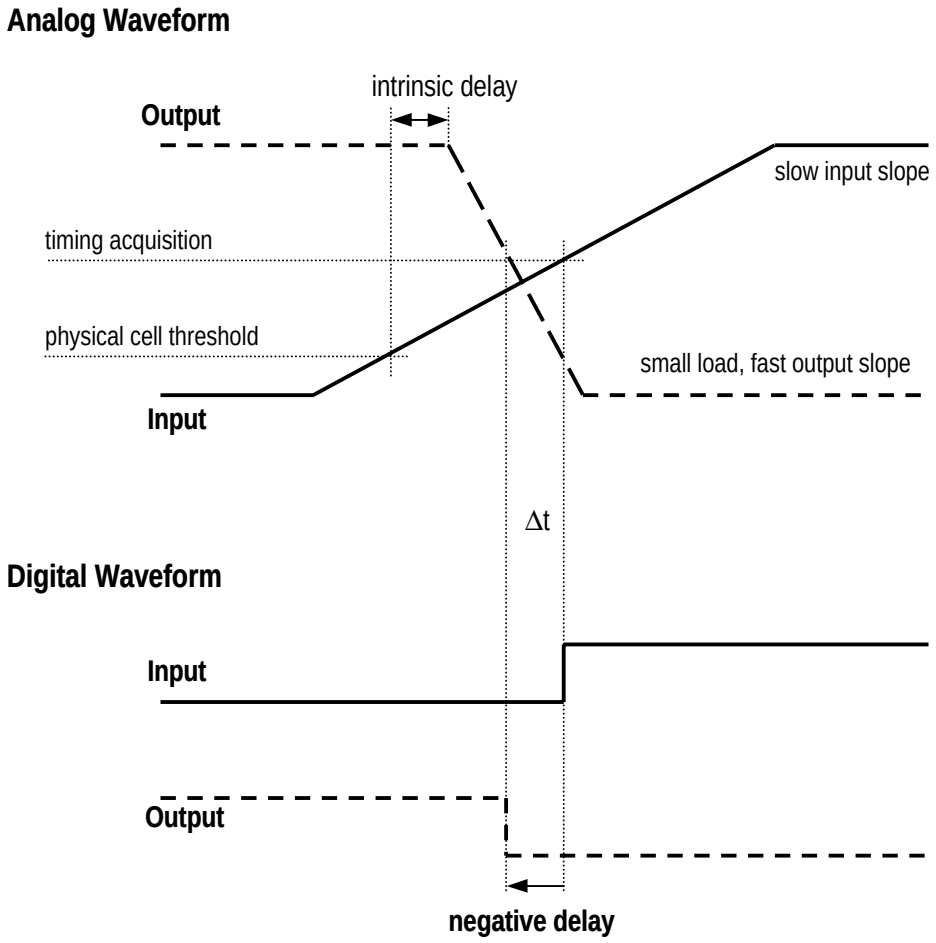
Related Documents / Revisions

Rev.	Date	Related Documents & Comments
1.0	Sep 2002	Release of C35 CORELIB Databook. 0.35µm CMOS C35 Process Parameters (Doc.# ENG-182 Rev 1.0) 0.35µm CMOS C35 Design Rules (Doc.# ENG-183 Rev 1.0)
1.1	Jan 2003	Updated Min. Width values for C, RN, SN in all D-type, JK and Toggle Flip Flops as well as GN, RN, SN in all D-Latches

Interpreting 'Negative Delays'

Under certain conditions, delay calculations may result in negative delay values.

These 'negative delays' are mainly caused by the difference between **timing acquisition** and the **physical cell threshold** as shown in the drawing below.

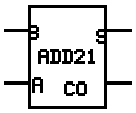


Note: Negative delays are set to "0" by some simulation tools.

ADD21 is a one-bit half adder with 1x drive strength.

Truth Table

A	B	CO	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0



Capacitance

Pin	Cap [pF]
A	0.008
B	0.009

Area

0.226 mils^2
146 µm^2

Power

0.91 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

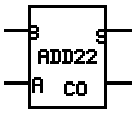
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay A => CO	0.18	1.83	0.22	1.88	0.25	1.35	0.66	1.78
Delay A => S	0.17	1.83	0.18	1.83	0.34	1.40	0.40	1.46
Delay B => CO	0.18	1.83	0.15	1.81	0.27	1.38	0.70	1.83
Delay B => S	0.15	1.81	0.12	1.78	0.34	1.41	0.32	1.39
Slew A => CO	0.12	4.23	0.16	4.25	0.12	2.40	0.16	2.40
Slew A => S	0.12	4.28	0.15	4.25	0.10	2.39	0.11	2.39
Slew B => CO	0.13	4.26	0.16	4.25	0.13	2.40	0.17	2.38
Slew B => S	0.11	4.30	0.15	4.30	0.10	2.38	0.11	2.39

ADD22 is a one-bit half adder with 2x drive strength.

Truth Table

A	B	CO	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0



Capacitance

Pin	Cap [pF]
A	0.013
B	0.016

Area

0.226 mils^2
146 µm^2

Power

1.75 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

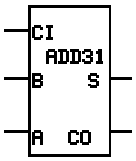
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**
Delay A => CO	0.14	1.73	0.16	1.74	0.21	1.28	0.61	1.69
Delay A => S	0.15	1.73	0.14	1.73	0.27	1.30	0.30	1.33
Delay B => CO	0.15	1.73	0.09	1.68	0.23	1.30	0.65	1.75
Delay B => S	0.13	1.71	0.08	1.67	0.27	1.30	0.23	1.26
Slew A => CO	0.10	4.08	0.14	4.07	0.10	2.33	0.14	2.33
Slew A => S	0.10	4.06	0.13	4.12	0.08	2.34	0.08	2.33
Slew B => CO	0.10	4.07	0.14	4.08	0.11	2.34	0.15	2.33
Slew B => S	0.09	4.09	0.13	4.08	0.08	2.34	0.08	2.31

ADD31 is a one-bit full adder with 1x drive strength.

Truth Table

A	B	CI	CO	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



Capacitance

Pin	Cap [pF]
A	0.023
B	0.020
CI	0.015

Area

0.423 mils^2
273 µm^2

Power

1.13 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

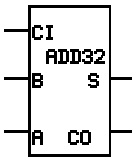
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay A => CO	0.22	1.88	0.25	1.92	0.30	1.43	0.58	1.72
Delay A => S	0.31	1.99	0.30	1.98	0.42	1.55	0.44	1.57
Delay B => CO	0.23	1.90	0.37	2.03	0.30	1.43	0.68	1.81
Delay B => S	0.30	1.98	0.39	2.06	0.43	1.56	0.56	1.70
Delay CI => CO	0.20	1.86	0.30	1.96	0.26	1.39	0.61	1.77
Delay CI => S	0.31	1.99	0.48	2.15	0.41	1.53	0.49	1.61
Slew A => CO	0.13	4.26	0.16	4.26	0.14	2.40	0.17	2.40
Slew A => S	0.15	4.31	0.18	4.29	0.14	2.40	0.14	2.40
Slew B => CO	0.13	4.27	0.16	4.25	0.14	2.41	0.18	2.41
Slew B => S	0.15	4.28	0.18	4.28	0.14	2.41	0.14	2.40
Slew CI => CO	0.13	4.27	0.17	4.25	0.14	2.40	0.18	2.40
Slew CI => S	0.16	4.31	0.17	4.31	0.14	2.40	0.13	2.40

ADD32 is a one-bit full adder with 2x drive strength.

Truth Table

A	B	CI	CO	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



Capacitance

Pin	Cap [pF]
A	0.038
B	0.034
CI	0.025

Area

0.423 mils^2
273 µm^2

Power

2.1 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

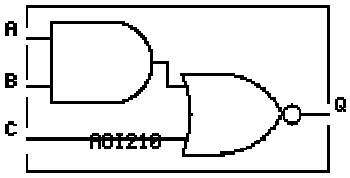
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**
Delay A => CO	0.19	1.78	0.21	1.81	0.26	1.34	0.53	1.63
Delay A => S	0.25	1.85	0.23	1.84	0.35	1.44	0.37	1.45
Delay B => CO	0.20	1.79	0.32	1.91	0.26	1.35	0.62	1.72
Delay B => S	0.24	1.84	0.32	1.93	0.36	1.45	0.48	1.56
Delay CI => CO	0.17	1.76	0.26	1.84	0.22	1.32	0.57	1.68
Delay CI => S	0.26	1.85	0.41	2.01	0.34	1.42	0.41	1.47
Slew A => CO	0.11	4.10	0.14	4.09	0.12	2.34	0.15	2.33
Slew A => S	0.13	4.11	0.16	4.12	0.11	2.33	0.11	2.33
Slew B => CO	0.11	4.09	0.14	4.09	0.12	2.34	0.15	2.33
Slew B => S	0.12	4.13	0.15	4.12	0.11	2.33	0.11	2.33
Slew CI => CO	0.11	4.07	0.15	4.08	0.12	2.34	0.16	2.34
Slew CI => S	0.13	4.13	0.15	4.14	0.11	2.34	0.10	2.33

AOI210 is an AND / NOR circuit with 0.5x drive strength providing the logical function Q = NOT (A.B+C).

Truth Table

A	B	C	Q
0	X	0	1
X	0	0	1
X	X	1	0
1	1	X	0



Capacitance

Pin	Cap [pF]
A	0.004
B	0.005
C	0.004

Area

0.113 mils^2
73 µm^2

Power

0.26 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

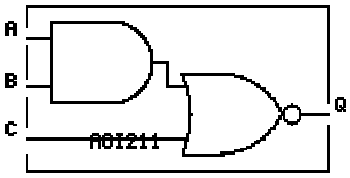
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**
Delay A => Q	0.12	1.74	0.33	1.94	0.07	0.93	0.11	1.17
Delay B => Q	0.14	1.75	0.40	1.97	0.08	0.93	0.02	1.02
Delay C => Q	0.09	1.70	0.35	2.02	0.07	1.15	0.13	1.43
Slew A => Q	0.20	4.27	0.51	4.26	0.15	2.13	0.58	2.25
Slew B => Q	0.25	4.30	0.54	4.29	0.15	2.14	0.55	2.22
Slew C => Q	0.23	4.29	0.52	4.29	0.12	2.57	0.51	2.63

AOI211 is an AND / NOR circuit with 1x drive strength providing the logical function Q = NOT (A.B+C).

Truth Table

A	B	C	Q
0	X	0	1
X	0	0	1
X	X	1	0
1	1	X	0



Capacitance

Pin	Cap [pF]
A	0.007
B	0.010
C	0.007

Area

0.113 mils^2
73 µm^2

Power

0.49 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

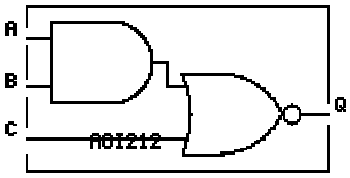
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay A => Q	0.10	1.67	0.29	1.86	0.07	0.90	0.09	1.14
Delay B => Q	0.12	1.69	0.37	1.88	0.07	0.90	0.01	0.99
Delay C => Q	0.08	1.63	0.32	1.94	0.06	1.08	0.10	1.37
Slew A => Q	0.16	4.08	0.48	4.08	0.13	2.05	0.55	2.17
Slew B => Q	0.20	4.13	0.51	4.13	0.13	2.06	0.52	2.15
Slew C => Q	0.20	4.13	0.48	4.11	0.10	2.43	0.47	2.50

AOI212 is an AND / NOR circuit with 2x drive strength providing the logical function Q = NOT (A.B+C).

Truth Table

A	B	C	Q
0	X	0	1
X	0	0	1
X	X	1	0
1	1	X	0



Capacitance

Pin	Cap [pF]
A	0.011
B	0.016
C	0.016

Area

0.141 mils^2
91 µm^2

Power

0.9 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

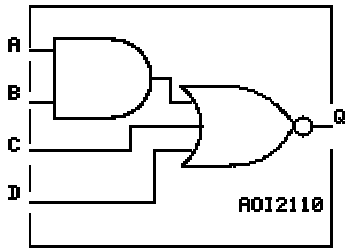
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**
Delay A => Q	0.09	1.67	0.31	1.90	0.06	0.87	0.05	1.12
Delay B => Q	0.11	1.68	0.39	1.92	0.06	0.88	-0.02	0.97
Delay C => Q	0.07	1.63	0.29	1.93	0.05	1.05	0.09	1.35
Slew A => Q	0.14	4.06	0.46	4.08	0.11	2.02	0.50	2.15
Slew B => Q	0.19	4.13	0.48	4.12	0.11	2.02	0.48	2.11
Slew C => Q	0.18	4.11	0.45	4.12	0.08	2.36	0.43	2.41

AOI2110 is an AND / NOR circuit with 0.5x drive strength providing the logical function Q = NOT (A.B+C+D).

Truth Table

A	B	C	D	Q
0	X	0	0	1
X	0	0	0	1
X	X	X	1	0
X	X	1	X	0
1	1	X	X	0



Capacitance

Pin	Cap [pF]
A	0.005
B	0.007
C	0.005
D	0.005

Area

0.141 mils^2
91 µm^2

Power

0.35 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

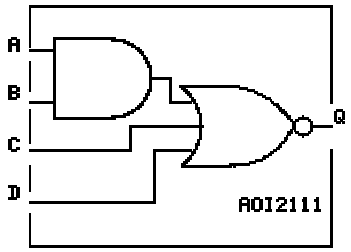
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**
Delay A => Q	0.18	1.75	0.31	1.87	0.12	0.99	0.23	1.23
Delay B => Q	0.20	1.77	0.38	1.89	0.12	0.99	0.13	1.08
Delay C => Q	0.15	1.72	0.32	1.91	0.13	1.21	0.30	1.50
Delay D => Q	0.11	1.67	0.36	1.96	0.09	1.18	0.21	1.47
Slew A => Q	0.29	4.23	0.62	4.23	0.26	2.24	0.74	2.33
Slew B => Q	0.34	4.26	0.66	4.27	0.26	2.25	0.69	2.33
Slew C => Q	0.34	4.26	0.65	4.27	0.23	2.66	0.63	2.70
Slew D => Q	0.32	4.26	0.61	4.26	0.16	2.62	0.52	2.65

AOI2111 is an AND / NOR circuit with 1x drive strength providing the logical function Q = NOT (A.B+C+D).

Truth Table

A	B	C	D	Q
0	X	0	0	1
X	0	0	0	1
X	X	X	1	0
X	X	1	X	0
1	1	X	X	0



Capacitance

Pin	Cap [pF]
A	0.009
B	0.012
C	0.009
D	0.010

Area

0.141 mils^2
91 µm^2

Power

0.66 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

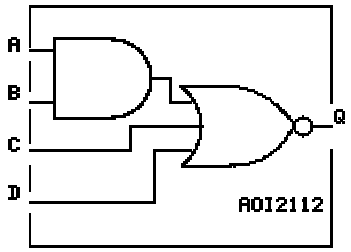
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay A => Q	0.16	1.71	0.28	1.82	0.10	0.95	0.21	1.20
Delay B => Q	0.17	1.72	0.35	1.84	0.10	0.96	0.10	1.05
Delay C => Q	0.13	1.68	0.29	1.86	0.11	1.14	0.27	1.43
Delay D => Q	0.09	1.64	0.33	1.92	0.08	1.11	0.17	1.40
Slew A => Q	0.25	4.13	0.59	4.15	0.23	2.16	0.71	2.25
Slew B => Q	0.29	4.16	0.62	4.17	0.23	2.16	0.66	2.25
Slew C => Q	0.29	4.17	0.62	4.17	0.19	2.50	0.59	2.55
Slew D => Q	0.27	4.17	0.56	4.16	0.12	2.45	0.48	2.51

AOI2112 is an AND / NOR circuit with 2x drive strength providing the logical function Q = NOT (A.B+C+D).

Truth Table

A	B	C	D	Q
0	X	0	0	1
X	0	0	0	1
X	X	X	1	0
X	X	1	X	0
1	1	X	X	0



Capacitance

Pin	Cap [pF]
A	0.018
B	0.022
C	0.019
D	0.018

Area

0.197 mils^2
127 µm^2

Power

1.19 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

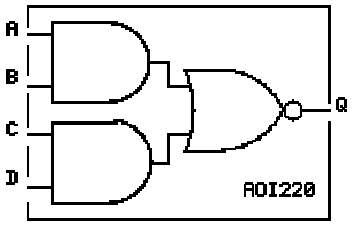
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**
Delay A => Q	0.13	1.67	0.24	1.78	0.08	0.92	0.17	1.17
Delay B => Q	0.15	1.69	0.32	1.80	0.08	0.92	0.06	1.02
Delay C => Q	0.11	1.65	0.26	1.84	0.09	1.09	0.23	1.39
Delay D => Q	0.07	1.61	0.29	1.89	0.06	1.07	0.12	1.36
Slew A => Q	0.19	4.05	0.55	4.06	0.19	2.09	0.66	2.19
Slew B => Q	0.23	4.09	0.58	4.10	0.19	2.09	0.63	2.18
Slew C => Q	0.23	4.10	0.55	4.08	0.15	2.42	0.56	2.47
Slew D => Q	0.21	4.08	0.48	4.09	0.09	2.37	0.43	2.43

AOI220 is an AND / NOR circuit with 0.5x drive strength providing the logical function Q = NOT (A.B+C.D).

Truth Table

A	B	C	D	Q
0	X	0	X	1
0	X	X	0	1
X	0	0	X	1
X	0	X	0	1
X	X	1	1	0
1	1	X	X	0



Capacitance

Pin	Cap [pF]
A	0.004
B	0.005
C	0.004
D	0.005

Area

0.141 mils^2
91 µm^2

Power

0.33 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

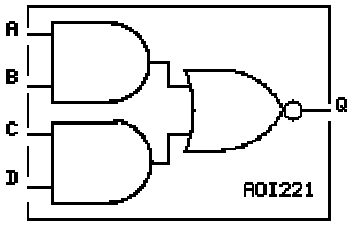
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**
Delay A => Q	0.18	1.80	0.40	2.01	0.12	0.97	0.20	1.21
Delay B => Q	0.20	1.81	0.46	2.03	0.12	0.97	0.12	1.07
Delay C => Q	0.10	1.72	0.44	2.05	0.06	0.89	0.04	1.14
Delay D => Q	0.12	1.73	0.50	2.08	0.07	0.90	-0.02	0.99
Slew A => Q	0.29	4.33	0.61	4.34	0.23	2.21	0.70	2.31
Slew B => Q	0.34	4.37	0.61	4.38	0.23	2.21	0.63	2.29
Slew C => Q	0.27	4.34	0.52	4.33	0.12	2.09	0.49	2.21
Slew D => Q	0.32	4.39	0.55	4.38	0.12	2.09	0.47	2.17

AOI221 is an AND / NOR circuit with 1x drive strength providing the logical function Q = NOT (A.B+C.D).

Truth Table

A	B	C	D	Q
0	X	0	X	1
0	X	X	0	1
X	0	0	X	1
X	0	X	0	1
X	X	1	1	0
1	1	X	X	0



Capacitance

Pin	Cap [pF]
A	0.007
B	0.009
C	0.007
D	0.009

Area

0.141 mils^2
91 µm^2

Power

0.6 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

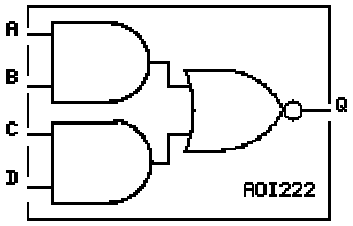
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay A => Q	0.15	1.72	0.36	1.91	0.10	0.93	0.18	1.18
Delay B => Q	0.17	1.73	0.42	1.93	0.10	0.93	0.09	1.03
Delay C => Q	0.09	1.65	0.41	1.98	0.05	0.86	0.03	1.12
Delay D => Q	0.11	1.67	0.48	2.00	0.06	0.87	-0.04	0.97
Slew A => Q	0.24	4.15	0.56	4.15	0.20	2.12	0.67	2.24
Slew B => Q	0.29	4.20	0.58	4.20	0.20	2.12	0.61	2.21
Slew C => Q	0.23	4.17	0.48	4.14	0.10	2.03	0.47	2.15
Slew D => Q	0.27	4.20	0.50	4.18	0.10	2.02	0.46	2.12

AOI222 is an AND / NOR circuit with 2x drive strength providing the logical function Q = NOT (A.B+C.D).

Truth Table

A	B	C	D	Q
0	X	0	X	1
0	X	X	0	1
X	0	0	X	1
X	0	X	0	1
X	X	1	1	0
1	1	X	X	0



Capacitance

Pin	Cap [pF]
A	0.013
B	0.017
C	0.013
D	0.017

Area

0.169 mils^2
109 µm^2

Power

1.1 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

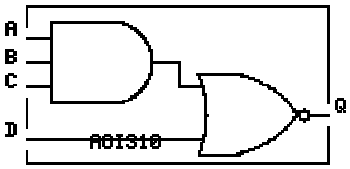
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**
Delay A => Q	0.13	1.67	0.33	1.87	0.09	0.92	0.16	1.17
Delay B => Q	0.15	1.69	0.39	1.89	0.09	0.93	0.07	1.03
Delay C => Q	0.08	1.62	0.38	1.95	0.05	0.87	0.01	1.12
Delay D => Q	0.10	1.63	0.46	1.97	0.05	0.88	-0.05	0.97
Slew A => Q	0.21	4.08	0.53	4.09	0.17	2.11	0.62	2.22
Slew B => Q	0.25	4.14	0.55	4.13	0.17	2.11	0.58	2.19
Slew C => Q	0.20	4.09	0.46	4.09	0.09	2.03	0.45	2.16
Slew D => Q	0.24	4.13	0.47	4.13	0.09	2.03	0.44	2.12

AOI310 is an AND / NOR circuit with 0.5x drive strength providing the logical function Q = NOT (A.B.C+D).

Truth Table

A	B	C	D	Q
0	X	X	0	1
X	0	X	0	1
X	X	0	0	1
X	X	X	1	0
1	1	1	X	0



Capacitance

Pin	Cap [pF]
A	0.006
B	0.005
C	0.005
D	0.004

Area

0.141 mils^2
91 µm^2

Power

0.32 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

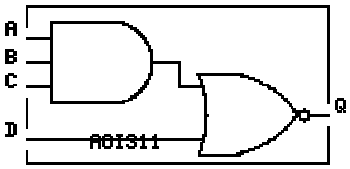
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**
Delay A => Q	0.20	1.82	0.52	2.04	0.09	0.86	-0.05	0.85
Delay B => Q	0.17	1.80	0.45	2.01	0.08	0.86	0.02	0.96
Delay C => Q	0.14	1.76	0.38	1.97	0.07	0.84	0.06	1.06
Delay D => Q	0.14	1.76	0.44	2.07	0.08	1.16	0.18	1.45
Slew A => Q	0.35	4.40	0.59	4.39	0.17	2.00	0.53	2.08
Slew B => Q	0.28	4.35	0.54	4.32	0.17	2.00	0.57	2.11
Slew C => Q	0.21	4.27	0.50	4.25	0.17	1.99	0.60	2.15
Slew D => Q	0.35	4.40	0.62	4.40	0.19	2.65	0.64	2.70

AOI311 is an AND / NOR circuit with 1x drive strength providing the logical function Q = NOT (A.B.C+D).

Truth Table

A	B	C	D	Q
0	X	X	0	1
X	0	X	0	1
X	X	0	0	1
X	X	X	1	0
1	1	1	X	0



Capacitance

Pin	Cap [pF]
A	0.011
B	0.008
C	0.008
D	0.007

Area

0.141 mils^2
91 µm^2

Power

0.62 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

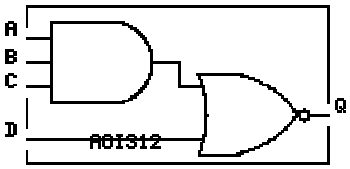
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay A => Q	0.18	1.74	0.49	1.95	0.08	0.83	-0.07	0.82
Delay B => Q	0.15	1.72	0.42	1.92	0.07	0.83	-0.00	0.93
Delay C => Q	0.11	1.69	0.34	1.89	0.06	0.81	0.04	1.04
Delay D => Q	0.13	1.69	0.41	1.99	0.07	1.10	0.16	1.39
Slew A => Q	0.31	4.22	0.56	4.22	0.14	1.93	0.51	2.02
Slew B => Q	0.24	4.16	0.52	4.16	0.14	1.93	0.56	2.03
Slew C => Q	0.18	4.11	0.48	4.10	0.14	1.92	0.57	2.08
Slew D => Q	0.31	4.23	0.59	4.21	0.17	2.51	0.63	2.55

AOI312 is an AND / NOR circuit with 2x drive strength providing the logical function Q = NOT (A.B.C+D).

Truth Table

A	B	C	D	Q
0	X	X	0	1
X	0	X	0	1
X	X	0	0	1
X	X	X	1	0
1	1	1	X	0



Capacitance

Pin	Cap [pF]
A	0.021
B	0.015
C	0.014
D	0.013

Area

0.169 mils^2
109 µm^2

Power

1.18 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

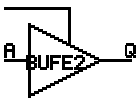
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**
Delay A => Q	0.16	1.71	0.47	1.92	0.07	0.83	-0.08	0.82
Delay B => Q	0.14	1.69	0.40	1.88	0.07	0.82	-0.01	0.93
Delay C => Q	0.10	1.66	0.32	1.85	0.05	0.81	0.03	1.03
Delay D => Q	0.12	1.66	0.39	1.96	0.06	1.07	0.14	1.36
Slew A => Q	0.28	4.16	0.55	4.15	0.13	1.92	0.51	2.02
Slew B => Q	0.21	4.09	0.49	4.08	0.13	1.92	0.55	2.04
Slew C => Q	0.15	4.05	0.46	4.05	0.13	1.92	0.56	2.07
Slew D => Q	0.28	4.16	0.55	4.14	0.14	2.41	0.61	2.50

BUFE2 is a buffer with 2x drive strength. The output is in a high impedance state when the E input is low. This cell is intended to be used in bus logic, internal to the circuit.

Truth Table

A	E	Q
0	1	0
X	0	Z
1	1	1



Capacitance

Pin	Cap [pF]
A	0.005
E	0.008
Q	0.008

Area

0.226 mils^2
146 µm^2

Power

0.84 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

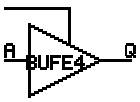
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**
Delay A => Q	0.17	1.77	0.24	1.85	0.20	1.30	0.53	1.65
Delay E => Q	0.12	1.88	0.17	1.92	0.14	1.06	0.26	1.17
Slew A => Q	0.11	4.07	0.15	4.10	0.10	2.34	0.14	2.33

BUFE4 is a buffer with 4x drive strength. The output is in a high impedance state when the E input is low. This cell is intended to be used in bus logic, internal to the circuit.

Truth Table

A	E	Q
0	1	0
X	0	Z
1	1	1



Capacitance

Pin	Cap [pF]
A	0.009
E	0.013
Q	0.008

Area

0.254 mils^2
164 µm^2

Power

1.66 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

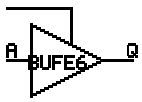
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.004**	**1.28**	**0.004**	**1.28**	**0.004**	**1.28**	**0.004**	**1.28**
Delay A => Q	0.15	1.76	0.22	1.83	0.17	1.27	0.49	1.61
Delay E => Q	0.10	1.67	0.12	1.74	0.11	0.97	0.20	1.06
Slew A => Q	0.08	4.09	0.12	4.10	0.07	2.32	0.12	2.33

BUFE6 is a buffer with 6x drive strength. The output is in a high impedance state when the E input is low. This cell is intended to be used in bus logic, internal to the circuit.

Truth Table

A	E	Q
0	1	0
X	0	Z
1	1	1



Capacitance

Pin	Cap [pF]
A	0.013
E	0.019
Q	0.010

Area

0.282 mils^2
182 µm^2

Power

2.51 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

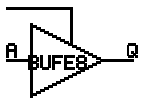
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.006**	**1.92**	**0.006**	**1.92**	**0.006**	**1.92**	**0.006**	**1.92**
Delay A => Q	0.13	1.71	0.19	1.79	0.15	1.23	0.46	1.57
Delay E => Q	0.09	1.52	0.09	1.58	0.10	0.89	0.18	0.97
Slew A => Q	0.07	4.01	0.11	4.00	0.07	2.30	0.11	2.29

BUFE8 is a buffer with 8x drive strength. The output is in a high impedance state when the E input is low. This cell is intended to be used in bus logic, internal to the circuit.

Truth Table

A	E	Q
0	1	0
X	0	Z
1	1	1



Capacitance

Pin	Cap [pF]
A	0.018
E	0.025
Q	0.020

Area

0.395 mils^2
255 µm^2

Power

3.26 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

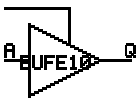
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.008**	**2.56**	**0.008**	**2.56**	**0.008**	**2.56**	**0.008**	**2.56**
Delay A => Q	0.14	1.72	0.20	1.78	0.16	1.25	0.48	1.59
Delay E => Q	0.09	1.44	0.09	1.50	0.10	0.85	0.19	0.93
Slew A => Q	0.09	4.05	0.12	3.99	0.08	2.31	0.12	2.31

BUFE10 is a buffer with 10x drive strength. The output is in a high impedance state when the E input is low. This cell is intended to be used in bus logic, internal to the circuit.

Truth Table

A	E	Q
0	1	0
X	0	Z
1	1	1



Capacitance

Pin	Cap [pF]
A	0.022
E	0.030
Q	0.020

Area

0.423 mils^2
273 µm^2

Power

4.19 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

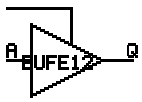
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.01**	**3.2**	**0.01**	**3.2**	**0.01**	**3.2**	**0.01**	**3.2**
Delay A => Q	0.14	1.72	0.19	1.79	0.15	1.24	0.46	1.58
Delay E => Q	0.09	1.39	0.09	1.44	0.10	0.79	0.18	0.87
Slew A => Q	0.08	4.08	0.12	4.04	0.07	2.32	0.12	2.32

BUFE12 is a buffer with 12x drive strength. The output is in a high impedance state when the E input is low. This cell is intended to be used in bus logic, internal to the circuit.

Truth Table

A	E	Q
0	1	0
X	0	Z
1	1	1



Capacitance

Pin	Cap [pF]
A	0.026
E	0.036
Q	0.022

Area

0.508 mils^2
328 µm^2

Power

4.75 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

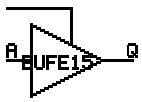
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.012**	**3.84**	**0.012**	**3.84**	**0.012**	**3.84**	**0.012**	**3.84**
Delay A => Q	0.13	1.71	0.18	1.78	0.15	1.23	0.46	1.56
Delay E => Q	0.09	1.34	0.08	1.40	0.09	0.73	0.15	0.79
Slew A => Q	0.08	4.03	0.12	4.03	0.07	2.30	0.11	2.31

BUFE15 is a buffer with 15x drive strength. The output is in a high impedance state when the E input is low. This cell is intended to be used in bus logic, internal to the circuit.

Truth Table

A	E	Q
0	1	0
X	0	Z
1	1	1



Capacitance

Pin	Cap [pF]
A	0.032
E	0.045
Q	0.030

Area

0.564 mils^2
364 µm^2

Power

5.85 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

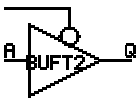
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.015**	**4.8**	**0.015**	**4.8**	**0.015**	**4.8**	**0.015**	**4.8**
Delay A => Q	0.13	1.71	0.18	1.77	0.15	1.22	0.46	1.56
Delay E => Q	0.09	1.41	0.08	1.49	0.09	0.83	0.15	0.88
Slew A => Q	0.08	4.06	0.12	3.99	0.07	2.29	0.12	2.31

BUFT2 is a buffer with 2x drive strength. The output is in a high impedance state when the EN input is high. This cell is intended to be used in bus logic, internal to the circuit.

Truth Table

A	EN	Q
0	0	0
X	1	Z
1	0	1



Capacitance

Pin	Cap [pF]
A	0.005
EN	0.007
Q	0.008

Area

0.226 mils^2
146 µm^2

Power

0.85 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

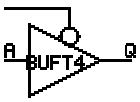
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**
Delay A => Q	0.18	1.78	0.24	1.86	0.19	1.29	0.53	1.65
Delay EN => Q	0.25	1.99	0.62	2.36	0.13	1.03	0.52	1.46
Slew A => Q	0.11	4.13	0.15	4.12	0.10	2.34	0.14	2.34

BUFT4 is a buffer with 4x drive strength. The output is in a high impedance state when the EN input is high. This cell is intended to be used in bus logic, internal to the circuit.

Truth Table

A	EN	Q
0	0	0
X	1	Z
1	0	1



Capacitance

Pin	Cap [pF]
A	0.009
EN	0.013
Q	0.008

Area

0.254 mils^2
164 µm^2

Power

1.67 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

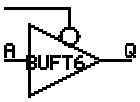
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.004**	**1.28**	**0.004**	**1.28**	**0.004**	**1.28**	**0.004**	**1.28**
Delay A => Q	0.15	1.77	0.22	1.84	0.17	1.26	0.49	1.61
Delay EN => Q	0.20	1.77	0.53	2.09	0.10	0.97	0.46	1.39
Slew A => Q	0.09	4.11	0.12	4.09	0.07	2.31	0.12	2.32

BUFT6 is a buffer with 6x drive strength. The output is in a high impedance state when the EN input is high. This cell is intended to be used in bus logic, internal to the circuit.

Truth Table

A	EN	Q
0	0	0
X	1	Z
1	0	1



Capacitance

Pin	Cap [pF]
A	0.013
EN	0.018
Q	0.010

Area

0.282 mils^2
182 µm^2

Power

2.28 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

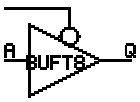
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.006**	**1.92**	**0.006**	**1.92**	**0.006**	**1.92**	**0.006**	**1.92**
Delay A => Q	0.14	1.72	0.19	1.78	0.15	1.23	0.46	1.57
Delay EN => Q	0.17	1.62	0.49	1.94	0.09	0.95	0.43	1.36
Slew A => Q	0.08	4.02	0.11	3.99	0.06	2.29	0.11	2.31

BUFT8 is a buffer with 8x drive strength. The output is in a high impedance state when the EN input is high. This cell is intended to be used in bus logic, internal to the circuit.

Truth Table

A	EN	Q
0	0	0
X	1	Z
1	0	1



Capacitance

Pin	Cap [pF]
A	0.017
EN	0.025
Q	0.020

Area

0.395 mils^2
255 µm^2

Power

3.28 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

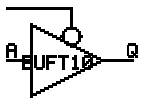
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.008**	**2.56**	**0.008**	**2.56**	**0.008**	**2.56**	**0.008**	**2.56**
Delay A => Q	0.15	1.71	0.20	1.79	0.16	1.24	0.48	1.58
Delay EN => Q	0.18	1.54	0.49	1.85	0.10	0.99	0.45	1.40
Slew A => Q	0.09	3.99	0.12	3.98	0.08	2.30	0.12	2.31

BUFT10 is a buffer with 10x drive strength. The output is in a high impedance state when the EN input is high. This cell is intended to be used in bus logic, internal to the circuit.

Truth Table

A	EN	Q
0	0	0
X	1	Z
1	0	1



Capacitance

Pin	Cap [pF]
A	0.021
EN	0.030
Q	0.020

Area

0.423 mils^2
273 µm^2

Power

3.93 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

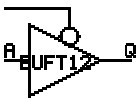
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.01**	**3.2**	**0.01**	**3.2**	**0.01**	**3.2**	**0.01**	**3.2**
Delay A => Q	0.14	1.74	0.19	1.79	0.15	1.23	0.46	1.57
Delay EN => Q	0.17	1.47	0.48	1.78	0.09	1.02	0.43	1.43
Slew A => Q	0.08	4.07	0.12	4.01	0.07	2.30	0.12	2.32

BUFT12 is a buffer with 12x drive strength. The output is in a high impedance state when the EN input is high. This cell is intended to be used in bus logic, internal to the circuit.

Truth Table

A	EN	Q
0	0	0
X	1	Z
1	0	1



Capacitance

Pin	Cap [pF]
A	0.025
EN	0.036
Q	0.022

Area

0.508 mils^2
328 µm^2

Power

4.66 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

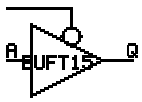
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.012**	**3.84**	**0.012**	**3.84**	**0.012**	**3.84**	**0.012**	**3.84**
Delay A => Q	0.13	1.72	0.18	1.78	0.15	1.22	0.46	1.56
Delay EN => Q	0.16	1.40	0.47	1.72	0.09	1.05	0.42	1.45
Slew A => Q	0.08	4.05	0.11	4.00	0.07	2.31	0.11	2.31

BUFT15 is a buffer with 15x drive strength. The output is in a high impedance state when the EN input is high. This cell is intended to be used in bus logic, internal to the circuit.

Truth Table

A	EN	Q
0	0	0
X	1	Z
1	0	1



Capacitance

Pin	Cap [pF]
A	0.032
EN	0.045
Q	0.030

Area

0.564 mils^2
364 µm^2

Power

5.81 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

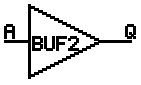
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.015**	**4.8**	**0.015**	**4.8**	**0.015**	**4.8**	**0.015**	**4.8**
Delay A => Q	0.13	1.71	0.18	1.78	0.15	1.22	0.46	1.56
Delay EN => Q	0.16	1.50	0.46	1.81	0.09	0.95	0.42	1.35
Slew A => Q	0.08	4.06	0.12	4.00	0.07	2.31	0.12	2.29

BUF2 is a noninverting buffer with 2x drive strength.

Truth Table

A	Q
0	0
1	1



Capacitance

Pin	Cap [pF]
A	0.003

Area

0.085 mils^2
55 µm^2

Power

0.84 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

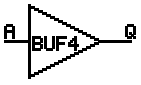
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.5**		**2**		**0.5**		**2**	
Load [pF]	**0.004**	**0.64**	**0.004**	**0.64**	**0.004**	**0.64**	**0.004**	**0.64**
Delay A => Q	0.23	1.81	0.27	1.84	0.30	1.35	0.58	1.64
Slew A => Q	0.12	4.13	0.16	4.13	0.12	2.33	0.17	2.33

BUF4 is a noninverting buffer with 4x drive strength.

Truth Table

A	Q
0	0
1	1



Capacitance

Pin	Cap [pF]
A	0.005

Area

0.113 mils^2
73 µm^2

Power

1.6 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

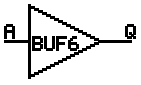
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.5**		**2**		**0.5**		**2**	
Load [pF]	**0.008**	**1.28**	**0.008**	**1.28**	**0.008**	**1.28**	**0.008**	**1.28**
Delay A => Q	0.20	1.77	0.24	1.81	0.27	1.32	0.52	1.58
Slew A => Q	0.10	4.05	0.14	4.11	0.09	2.33	0.14	2.33

BUF6 is a noninverting buffer with 6x drive strength.

Truth Table

A	Q
0	0
1	1



Capacitance

Pin	Cap [pF]
A	0.007

Area

0.113 mils^2
73 µm^2

Power

2.36 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

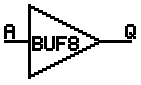
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.5**		**2**		**0.5**		**2**	
Load [pF]	**0.012**	**1.92**	**0.012**	**1.92**	**0.012**	**1.92**	**0.012**	**1.92**
Delay A => Q	0.19	1.76	0.23	1.77	0.26	1.30	0.50	1.55
Slew A => Q	0.09	4.06	0.13	4.06	0.09	2.30	0.14	2.30

BUF8 is a noninverting buffer with 8x drive strength.

Truth Table

A	Q
0	0
1	1



Capacitance

Pin	Cap [pF]
A	0.009

Area

0.141 mils^2
91 µm^2

Power

3.22 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.5**		**2**		**0.5**		**2**	
Load [pF]	**0.016**	**2.56**	**0.016**	**2.56**	**0.016**	**2.56**	**0.016**	**2.56**
Delay A => Q	0.19	1.74	0.23	1.77	0.26	1.28	0.50	1.53
Slew A => Q	0.10	3.99	0.14	4.05	0.10	2.29	0.14	2.29

BUF12 is a noninverting buffer with 12x drive strength.

Truth Table

A	Q
0	0
1	1

Capacitance

Pin	Cap [pF]
A	0.013

Area

0.169 mils^2
109 µm^2

Power

4.67 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.5**		**2**		**0.5**		**2**	
Load [pF]	**0.024**	**3.84**	**0.024**	**3.84**	**0.024**	**3.84**	**0.024**	**3.84**
Delay A => Q	0.18	1.75	0.22	1.76	0.25	1.28	0.48	1.53
Slew A => Q	0.09	4.07	0.13	4.06	0.09	2.31	0.14	2.30

BUF15 is a noninverting buffer with 15x drive strength.

Truth Table

A	Q
0	0
1	1

Capacitance

Pin	Cap [pF]
A	0.018

Area

0.226 mils^2
146 µm^2

Power

5.95 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.5**		**2**		**0.5**		**2**	
Load [pF]	**0.03**	**4.8**	**0.03**	**4.8**	**0.03**	**4.8**	**0.03**	**4.8**
Delay A => Q	0.17	1.74	0.20	1.75	0.24	1.27	0.47	1.51
Slew A => Q	0.09	4.07	0.13	4.07	0.09	2.31	0.13	2.31

BUSHD is a busholder circuit which prevents internal tristate buses from floating to undefined logic levels when tristated.

Truth Table

A
A

Capacitance

Pin	Cap [pF]
A	0.005

Area

0.085 mils^2
55 µm^2

CLKBU2 is a Symmetrical Buffer for clock tree synthesis with 2x drive strength.

Truth Table

A	Q
0	0
1	1

Capacitance

Pin	Cap [pF]
A	0.003

Area

0.085 mils^2
55 µm^2

Power

0.72 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**
Delay A => Q	0.18	1.79	0.33	1.92	0.21	1.52	0.56	1.87
Slew A => Q	0.11	4.14	0.16	4.07	0.11	2.93	0.16	2.93

CLKBU4 is a Symmetrical Buffer for clock tree synthesis with 4x drive strength.

Truth Table

A	Q
0	0
1	1

Capacitance

Pin	Cap [pF]
A	0.005

Area

0.113 mils^2
73 µm^2

Power

1.37 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

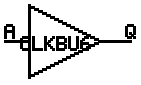
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.004**	**1.28**	**0.004**	**1.28**	**0.004**	**1.28**	**0.004**	**1.28**
Delay A => Q	0.15	1.74	0.28	1.88	0.17	1.48	0.49	1.80
Slew A => Q	0.09	4.11	0.14	4.11	0.08	2.92	0.14	2.91

CLKBU6 is a Symmetrical Buffer for clock tree synthesis with 6x drive strength.

Truth Table

A	Q
0	0
1	1



Capacitance

Pin	Cap [pF]
A	0.007

Area

0.113 mils^2
73 µm^2

Power

2 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

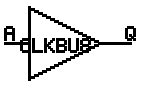
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.006**	**1.92**	**0.006**	**1.92**	**0.006**	**1.92**	**0.006**	**1.92**
Delay A => Q	0.14	1.71	0.27	1.83	0.16	1.43	0.47	1.75
Slew A => Q	0.08	4.05	0.13	4.06	0.07	2.83	0.13	2.86

CLKBU8 is a Symmetrical Buffer for clock tree synthesis with 8x drive strength.

Truth Table

A	Q
0	0
1	1



Capacitance

Pin	Cap [pF]
A	0.008

Area

0.141 mils^2
91 µm^2

Power

2.93 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

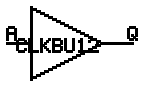
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.008**	**2.56**	**0.008**	**2.56**	**0.008**	**2.56**	**0.008**	**2.56**
Delay A => Q	0.14	1.69	0.27	1.83	0.16	1.44	0.47	1.75
Slew A => Q	0.09	4.00	0.14	4.05	0.08	2.88	0.14	2.86

CLKBU12 is a Symmetrical Buffer for clock tree synthesis with 12x drive strength.

Truth Table

A	Q
0	0
1	1



Capacitance

Pin	Cap [pF]
A	0.012

Area

0.169 mils^2
109 µm^2

Power

4.2 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

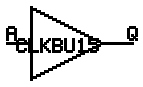
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.012**	**3.84**	**0.012**	**3.84**	**0.012**	**3.84**	**0.012**	**3.84**
Delay A => Q	0.14	1.70	0.28	1.84	0.15	1.19	0.44	1.50
Slew A => Q	0.08	4.04	0.13	4.06	0.07	2.31	0.13	2.30

CLKBU15 is a Symmetrical Buffer for clock tree synthesis with 15x drive strength.

Truth Table

A	Q
0	0
1	1



Capacitance

Pin	Cap [pF]
A	0.016

Area

0.226 mils^2
146 µm^2

Power

5.24 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.015**	**4.8**	**0.015**	**4.8**	**0.015**	**4.8**	**0.015**	**4.8**
Delay A => Q	0.13	1.70	0.27	1.82	0.14	1.17	0.43	1.48
Slew A => Q	0.08	4.05	0.13	4.07	0.07	2.31	0.13	2.30

CLKIN0 is a Symmetrical Inverter for clock tree synthesis with 0.5x drive strength.

Truth Table

A	Q
0	1
1	0

Capacitance

Pin	Cap [pF]
A	0.004

Area

0.056 mils^2
36 µm^2

Power

0.17 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**
Delay A => Q	0.06	1.89	0.31	2.24	0.05	1.44	0.06	1.71
Slew A => Q	0.13	4.71	0.43	4.66	0.08	3.24	0.42	3.29

CLKIN1 is a Symmetrical Inverter for clock tree synthesis with 1x drive strength.

Truth Table

A	Q
0	1
1	0

Capacitance

Pin	Cap [pF]
A	0.005

Area

0.056 mils^2
36 µm^2

Power

0.32 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay A => Q	0.04	1.70	0.25	2.06	0.04	1.34	0.03	1.62
Slew A => Q	0.09	4.28	0.38	4.25	0.06	3.03	0.36	3.07

CLKIN2 is a Symmetrical Inverter for clock tree synthesis with 2x drive strength.

Truth Table

A	Q
0	1
1	0

Capacitance

Pin	Cap [pF]
A	0.008

Area

0.056 mils^2
36 µm^2

Power

0.63 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**
Delay A => Q	0.04	1.61	0.22	1.98	0.03	1.29	0.01	1.58
Slew A => Q	0.07	4.10	0.34	4.12	0.04	2.95	0.34	2.96

CLKIN3 is a Symmetrical Inverter for clock tree synthesis with 3x drive strength.

Truth Table

A	Q
0	1
1	0

Capacitance

Pin	Cap [pF]
A	0.012

Area

0.056 mils^2
36 µm^2

Power

0.94 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay A => Q	0.03	1.59	0.21	1.96	0.03	1.29	0.01	1.56
Slew A => Q	0.06	4.06	0.33	4.07	0.04	2.90	0.34	2.93

CLKIN4 is a Symmetrical Inverter for clock tree synthesis with 4x drive strength.

Truth Table

A	Q
0	1
1	0

Capacitance

Pin	Cap [pF]
A	0.017

Area

0.085 mils^2
55 µm^2

Power

1.21 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.004**	**1.28**	**0.004**	**1.28**	**0.004**	**1.28**	**0.004**	**1.28**
Delay A => Q	0.03	1.60	0.20	1.98	0.03	1.29	-0.01	1.57
Slew A => Q	0.05	4.06	0.30	4.11	0.03	2.92	0.31	2.95

CLKIN6 is a Symmetrical Inverter for clock tree synthesis with 6x drive strength.

Truth Table

A	Q
0	1
1	0

Capacitance

Pin	Cap [pF]
A	0.023

Area

0.085 mils^2
55 µm^2

Power

1.79 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.006**	**1.92**	**0.006**	**1.92**	**0.006**	**1.92**	**0.006**	**1.92**
Delay A => Q	0.03	1.58	0.19	1.95	0.03	1.28	-0.02	1.56
Slew A => Q	0.05	4.01	0.28	4.06	0.03	2.89	0.29	2.91

CLKIN8 is a Symmetrical Inverter for clock tree synthesis with 8x drive strength.

Truth Table

A	Q
0	1
1	0

Capacitance

Pin	Cap [pF]
A	0.032

Area

0.113 mils^2
73 µm^2

Power

2.46 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.008**	**2.56**	**0.008**	**2.56**	**0.008**	**2.56**	**0.008**	**2.56**
Delay A => Q	0.03	1.58	0.20	1.95	0.03	1.29	-0.00	1.57
Slew A => Q	0.06	4.02	0.31	4.05	0.04	2.91	0.32	2.94

CLKIN10 is a Symmetrical Inverter for clock tree synthesis with 10x drive strength.

Truth Table

A	Q
0	1
1	0

Capacitance

Pin	Cap [pF]
A	0.040

Area

0.141 mils^2
91 µm^2

Power

3.02 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.01**	**3.2**	**0.01**	**3.2**	**0.01**	**3.2**	**0.01**	**3.2**
Delay A => Q	0.03	1.59	0.19	1.96	0.03	1.28	-0.01	1.56
Slew A => Q	0.05	4.05	0.30	4.08	0.03	2.90	0.31	2.93

CLKIN12 is a Symmetrical Inverter for clock tree synthesis with 12x drive strength.

Truth Table

A	Q
0	1
1	0

Capacitance

Pin	Cap [pF]
A	0.047

Area

0.141 mils^2
91 µm^2

Power

3.61 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.012**	**3.84**	**0.012**	**3.84**	**0.012**	**3.84**	**0.012**	**3.84**
Delay A => Q	0.03	1.59	0.19	1.95	0.03	1.28	-0.01	1.56
Slew A => Q	0.05	4.04	0.29	4.06	0.03	2.89	0.30	2.92

CLKIN15 is a Symmetrical Inverter for clock tree synthesis with 15x drive strength.

Truth Table

A	Q
0	1
1	0

Capacitance

Pin	Cap [pF]
A	0.059

Area

0.169 mils^2
109 µm^2

Power

4.54 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

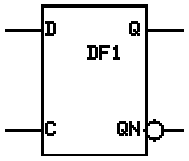
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.015**	**4.8**	**0.015**	**4.8**	**0.015**	**4.8**	**0.015**	**4.8**
Delay A => Q	0.03	1.59	0.19	1.95	0.03	1.29	-0.01	1.56
Slew A => Q	0.05	4.04	0.30	4.06	0.03	2.89	0.31	2.92

DF1 is a static, master-slave D flip-flop with 1x drive strength.

Truth Table

C	D	Q	QN
↑	0	0	1
↑	1	1	0



Capacitance

Pin	Cap [pF]
C	0.004
D	0.005

Area

0.423 mils^2
273 µm^2

Power

1.13 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay C => Q	0.50	2.14	0.67	2.31	0.57	1.63	0.73	1.79
Delay C => QN	0.67	2.30	0.83	2.47	0.58	1.63	0.76	1.80
Slew C => Q	0.11	4.25	0.11	4.25	0.09	2.40	0.09	2.37
Slew C => QN	0.10	4.24	0.10	4.23	0.07	2.38	0.07	2.37

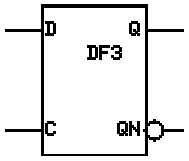
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
D => C	0	0.002	0.039	0.108

	Min Width	
	High	**Low**
C	0.376	0.326

DF3 is a static, master-slave D flip-flop with 3x drive strength.

Truth Table

C	D	Q	QN
↑	0	0	1
↑	1	1	0



Capacitance

Pin	Cap [pF]
C	0.004
D	0.005

Area

0.423 mils^2
273 µm^2

Power

1.76 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay C => Q	0.53	2.09	0.71	2.27	0.61	1.67	0.77	1.83
Delay C => QN	0.77	2.30	0.93	2.46	0.68	1.72	0.85	1.90
Slew C => Q	0.10	4.01	0.10	4.01	0.10	2.32	0.10	2.33
Slew C => QN	0.10	4.01	0.10	4.03	0.09	2.34	0.09	2.33

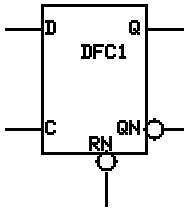
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
D => C	0	0.002	0.039	0.108

	Min Width	
	High	**Low**
C	0.376	0.326

DFC1 is a static, master-slave D flip-flop with 1x drive strength. CLEAR is asynchronous and active low.

Truth Table

C	D	RN	Q	QN
↑	0	1	0	1
↑	1	1	1	0
X	X	0	0	1



Capacitance

Pin	Cap [pF]
C	0.004
D	0.005
RN	0.011

Area

0.48 mils^2
310 µm^2

Power

1.23 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay C => Q	0.47	2.12	0.65	2.30	0.62	1.68	0.78	1.85
Delay C => QN	0.72	2.36	0.88	2.52	0.56	1.60	0.73	1.78
Delay RN => Q	n.a.	n.a.	n.a.	n.a.	0.16	1.22	0.53	1.61
Delay RN => QN	0.31	1.96	0.70	2.34	n.a.	n.a.	n.a.	n.a.
Slew C => Q	0.11	4.25	0.11	4.25	0.10	2.39	0.10	2.38
Slew C => QN	0.10	4.23	0.10	4.23	0.07	2.37	0.08	2.37
Slew RN => Q	n.a.	n.a.	n.a.	n.a.	0.09	2.39	0.13	2.38
Slew RN => QN	0.13	4.25	0.13	4.24	n.a.	n.a.	n.a.	n.a.

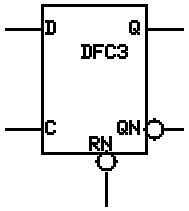
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
D => C	0	0.002	0.039	0.088
RN => C	0	n.a.	0.515	n.a.

	Min Width	
	High	**Low**
C	0.376	0.326
RN	n.a.	0.360

DFC3 is a static, master-slave D flip-flop with 3x drive strength. CLEAR is asynchronous and active low.

Truth Table

C	D	RN	Q	QN
↑	0	1	0	1
↑	1	1	1	0
X	X	0	0	1



Capacitance

Pin	Cap [pF]
C	0.004
D	0.005
RN	0.011

Area

0.48 mils^2
310 µm^2

Power

1.92 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay C => Q	0.49	2.06	0.67	2.23	0.66	1.73	0.82	1.89
Delay C => QN	0.82	2.35	0.98	2.52	0.64	1.69	0.82	1.86
Delay RN => Q	n.a.	n.a.	n.a.	n.a.	0.20	1.25	0.60	1.66
Delay RN => QN	0.41	1.96	0.82	2.36	n.a.	n.a.	n.a.	n.a.
Slew C => Q	0.10	4.04	0.10	4.01	0.11	2.34	0.11	2.33
Slew C => QN	0.10	4.03	0.10	4.02	0.09	2.33	0.09	2.32
Slew RN => Q	n.a.	n.a.	n.a.	n.a.	0.10	2.33	0.14	2.34
Slew RN => QN	0.12	4.03	0.12	4.02	n.a.	n.a.	n.a.	n.a.

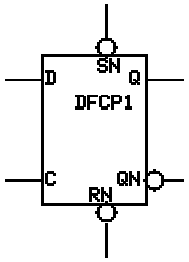
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
D => C	0	0.002	0.039	0.088
RN => C	0	n.a.	0.516	n.a.

	Min Width	
	High	**Low**
C	0.376	0.326
RN	n.a.	0.360

DFCP1 is a static, master-slave D flip-flop with 1x drive strength. PRESET and CLEAR are asynchronous and active low.

Truth Table

C	D	RN	SN	Q	QN
↑	0	1	1	0	1
↑	1	1	1	1	0
X	X	0	0	0	0
X	X	0	1	0	1
X	X	1	0	1	0



Capacitance

Pin	Cap [pF]
C	0.004
D	0.005
RN	0.015
SN	0.014

Area

0.508 mils^2
328 µm^2

Power

1.34 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay C => Q	0.49	2.14	0.66	2.31	0.63	1.70	0.80	1.87
Delay C => QN	0.71	2.35	0.87	2.51	0.61	1.66	0.79	1.84
Delay RN => Q	0.12	1.78	0.11	1.76	0.16	1.23	0.54	1.63
Delay RN => QN	0.28	1.93	0.66	2.31	n.a.	n.a.	n.a.	n.a.
Delay SN => Q	0.34	1.98	0.73	2.37	n.a.	n.a.	n.a.	n.a.
Delay SN => QN	0.13	1.81	0.17	1.83	0.20	1.29	0.59	1.70
Slew C => Q	0.11	4.26	0.11	4.24	0.10	2.38	0.11	2.38
Slew C => QN	0.10	4.22	0.10	4.24	0.08	2.39	0.08	2.37
Slew RN => Q	0.11	4.30	0.15	4.30	0.10	2.40	0.14	2.39
Slew RN => QN	0.13	4.24	0.14	4.24	n.a.	n.a.	n.a.	n.a.
Slew SN => Q	0.12	4.25	0.12	4.25	n.a.	n.a.	n.a.	n.a.
Slew SN => QN	0.12	4.30	0.15	4.30	0.11	2.39	0.14	2.39

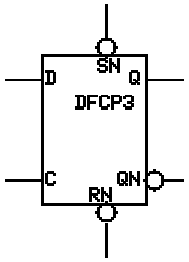
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
D => C	0.012	0	0	0.109
RN => C	0	n.a.	0.494	n.a.
SN => C	0	n.a.	0.364	n.a.

	Min Width	
	High	**Low**
C	0.376	0.326
RN	n.a.	0.360
SN	n.a.	0.380

DFCP3 is a static, master-slave D flip-flop with 3x drive strength. PRESET and CLEAR are asynchronous and active low.

Truth Table

C	D	RN	SN	Q	QN
↑	0	1	1	0	1
↑	1	1	1	1	0
X	X	0	0	0	0
X	X	0	1	0	1
X	X	1	0	1	0



Capacitance

Pin	Cap [pF]
C	0.004
D	0.005
RN	0.015
SN	0.014

Area

0.508 mils^2
328 µm^2

Power

1.88 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay C => Q	0.51	2.07	0.69	2.25	0.67	1.77	0.84	1.94
Delay C => QN	0.78	2.33	0.94	2.49	0.70	1.77	0.88	1.95
Delay RN => Q	0.14	1.70	0.17	1.73	0.21	1.30	0.61	1.71
Delay RN => QN	0.35	1.91	0.76	2.31	n.a.	n.a.	n.a.	n.a.
Delay SN => Q	0.41	1.96	0.82	2.36	n.a.	n.a.	n.a.	n.a.
Delay SN => QN	0.15	1.74	0.22	1.79	0.24	1.36	0.65	1.78
Slew C => Q	0.11	4.05	0.10	4.00	0.11	2.39	0.11	2.39
Slew C => QN	0.10	4.03	0.10	4.03	0.09	2.38	0.11	2.39
Slew RN => Q	0.10	4.08	0.14	4.06	0.11	2.40	0.14	2.40
Slew RN => QN	0.13	4.03	0.12	4.03	n.a.	n.a.	n.a.	n.a.
Slew SN => Q	0.11	4.03	0.11	4.03	n.a.	n.a.	n.a.	n.a.
Slew SN => QN	0.12	4.07	0.15	4.09	0.12	2.40	0.16	2.40

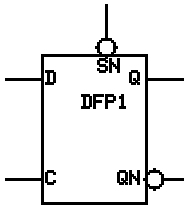
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
D => C	0.012	0	0	0.109
RN => C	0	n.a.	0.494	n.a.
SN => C	0	n.a.	0.365	n.a.

	Min Width	
	High	**Low**
C	0.376	0.326
RN	n.a.	0.360
SN	n.a.	0.380

DFP1 is a static, master-slave D flip-flop with 1x drive strength. PRESET is asynchronous and active low.

Truth Table

C	D	SN	Q	QN
↑	0	1	0	1
↑	1	1	1	0
X	X	0	1	0



Capacitance

Pin	Cap [pF]
C	0.004
D	0.005
SN	0.012

Area

0.48 mils^2
310 µm^2

Power

1.28 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay C => Q	0.50	2.14	0.68	2.32	0.57	1.64	0.74	1.80
Delay C => QN	0.64	2.29	0.81	2.45	0.62	1.68	0.80	1.85
Delay SN => Q	0.37	2.01	0.77	2.40	n.a.	n.a.	n.a.	n.a.
Delay SN => QN	n.a.	n.a.	n.a.	n.a.	0.19	1.27	0.58	1.67
Slew C => Q	0.11	4.25	0.11	4.25	0.09	2.39	0.09	2.39
Slew C => QN	0.10	4.25	0.10	4.23	0.09	2.39	0.09	2.39
Slew SN => Q	0.12	4.24	0.12	4.25	n.a.	n.a.	n.a.	n.a.
Slew SN => QN	n.a.	n.a.	n.a.	n.a.	0.10	2.38	0.14	2.38

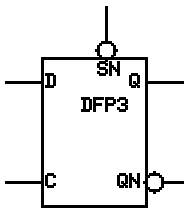
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
D => C	0.015	0	0	0.124
SN => C	0	n.a.	0.406	n.a.

	Min Width	
	High	**Low**
C	0.376	0.326
SN	n.a.	0.380

DFP3 is a static, master-slave D flip-flop with 3x drive strength. PRESET is asynchronous and active low.

Truth Table

C	D	SN	Q	QN
↑	0	1	0	1
↑	1	1	1	0
X	X	0	1	0



Capacitance

Pin	Cap [pF]
C	0.004
D	0.005
SN	0.012

Area

0.48 mils^2
310 µm^2

Power

1.85 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay C => Q	0.53	2.10	0.71	2.27	0.61	1.67	0.78	1.83
Delay C => QN	0.72	2.27	0.89	2.44	0.72	1.75	0.90	1.93
Delay SN => Q	0.47	2.02	0.88	2.42	n.a.	n.a.	n.a.	n.a.
Delay SN => QN	n.a.	n.a.	n.a.	n.a.	0.23	1.30	0.64	1.71
Slew C => Q	0.11	4.04	0.10	4.06	0.10	2.32	0.10	2.32
Slew C => QN	0.10	4.05	0.10	4.04	0.10	2.32	0.10	2.31
Slew SN => Q	0.12	4.05	0.12	4.05	n.a.	n.a.	n.a.	n.a.
Slew SN => QN	n.a.	n.a.	n.a.	n.a.	0.12	2.31	0.15	2.31

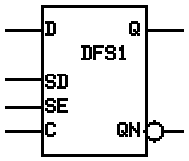
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
D => C	0.015	0	0	0.003
SN => C	0	n.a.	0.406	n.a.

	Min Width	
	High	**Low**
C	0.376	0.326
SN	n.a.	0.380

DFS1 is a static, master-slave Scan D flip-flop with 1x drive strength. SCAN ENABLE switches between normal DATA input and SCAN DATA input.

Truth Table

C	D	SD	SE	Q	QN
↑	0	X	0	0	1
↑	X	0	1	0	1
↑	X	1	1	1	0
↑	1	X	0	1	0



Capacitance

Pin	Cap [pF]
C	0.004
D	0.004
SD	0.009
SE	0.006

Area

0.564 mils^2
364 µm^2

Power

1.37 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay C => Q	0.49	2.14	0.66	2.31	0.53	1.60	0.69	1.75
Delay C => QN	0.65	2.29	0.80	2.45	0.60	1.66	0.77	1.82
Slew C => Q	0.12	4.26	0.11	4.25	0.09	2.37	0.09	2.39
Slew C => QN	0.11	4.25	0.11	4.25	0.09	2.40	0.09	2.40

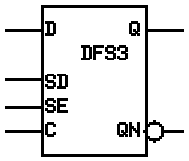
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
D => C	0	0.002	0	0
SD => C	0	0.121	0	0
SE => C	0.202	0.41	0	0

	Min Width	
	High	**Low**
C	0.376	0.326

DFS3 is a static, master-slave Scan D flip-flop with 3x drive strength. SCAN ENABLE switches between normal DATA input and SCAN DATA input.

Truth Table

C	D	SD	SE	Q	QN
↑	0	X	0	0	1
↑	X	0	1	0	1
↑	X	1	1	1	0
↑	1	X	0	1	0



Capacitance

Pin	Cap [pF]
C	0.004
D	0.004
SD	0.009
SE	0.006

Area

0.592 mils^2
382 µm^2

Power

2.04 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay C => Q	0.52	2.08	0.69	2.25	0.57	1.63	0.72	1.79
Delay C => QN	0.75	2.28	0.90	2.43	0.69	1.72	0.86	1.89
Slew C => Q	0.10	4.01	0.10	4.04	0.10	2.31	0.10	2.32
Slew C => QN	0.10	4.02	0.10	4.02	0.10	2.30	0.10	2.31

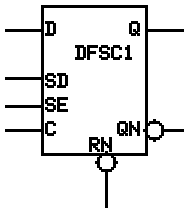
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
D => C	0	0.002	0	0
SD => C	0	0.12	0	0
SE => C	0.2	0.392	0	0

	Min Width	
	High	**Low**
C	0.376	0.326

DFSC1 is a static, master-slave Scan D flip-flop with 1x drive strength. SCAN ENABLE switches between normal DATA input and SCAN DATA input. CLEAR is asynchronous and active low.

Truth Table

C	D	RN	SD	SE	Q	QN
↑	0	1	X	0	0	1
↑	X	1	0	1	0	1
↑	X	1	1	1	1	0
↑	1	1	X	0	1	0
X	X	0	X	X	0	1



Capacitance

Pin	Cap [pF]
C	0.004
D	0.004
RN	0.011
SD	0.009
SE	0.006

Area

0.592 mils^2
382 µm^2

Power

1.35 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay C => Q	0.50	2.14	0.73	2.34	0.60	1.67	0.78	1.86
Delay C => QN	0.71	2.37	0.90	2.54	0.60	1.63	0.82	1.84
Delay RN => Q	n.a.	n.a.	n.a.	n.a.	0.20	1.26	0.56	1.66
Delay RN => QN	0.34	2.01	0.74	2.43	n.a.	n.a.	n.a.	n.a.
Slew C => Q	0.12	4.25	0.11	4.24	0.10	2.39	0.10	2.39
Slew C => QN	0.11	4.26	0.11	4.25	0.09	2.40	0.10	2.40
Slew RN => Q	n.a.	n.a.	n.a.	n.a.	0.17	2.41	0.17	2.43
Slew RN => QN	0.17	4.34	0.17	4.27	n.a.	n.a.	n.a.	n.a.

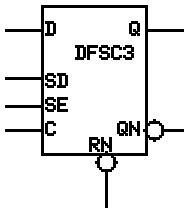
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
D => C	0	0.002	0	0
RN => C	0	n.a.	0.466	n.a.
SD => C	0	0.123	0	0
SE => C	0.227	0.412	0	0

	Min Width	
	High	**Low**
C	0.376	0.326
RN	n.a.	0.360

DFSC3 is a static, master-slave Scan D flip-flop with 3x drive strength. SCAN ENABLE switches between normal DATA input and SCAN DATA input. CLEAR is asynchronous and active low.

Truth Table

C	D	RN	SD	SE	Q	QN
↑	0	1	X	0	0	1
↑	X	1	0	1	0	1
↑	X	1	1	1	1	0
↑	1	1	X	0	1	0
X	X	0	X	X	0	1



Capacitance

Pin	Cap [pF]
C	0.004
D	0.004
RN	0.011
SD	0.009
SE	0.006

Area

0.621 mils^2
401 µm^2

Power

1.98 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay C => Q	0.50	2.07	0.73	2.28	0.63	1.72	0.81	1.86
Delay C => QN	0.81	2.35	1.00	2.50	0.65	1.68	0.83	1.92
Delay RN => Q	n.a.	n.a.	n.a.	n.a.	0.21	1.27	0.65	1.74
Delay RN => QN	0.44	1.99	0.88	2.42	n.a.	n.a.	n.a.	n.a.
Slew C => Q	0.10	4.01	0.11	4.02	0.11	2.31	0.12	2.32
Slew C => QN	0.10	4.01	0.10	4.02	0.10	2.31	0.10	2.32
Slew RN => Q	n.a.	n.a.	n.a.	n.a.	0.10	2.36	0.14	2.31
Slew RN => QN	0.17	4.07	0.17	4.08	n.a.	n.a.	n.a.	n.a.

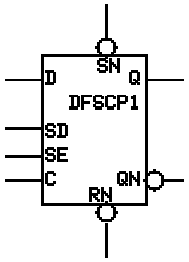
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
D => C	0.236	0.318	0	0
RN => C	0	n.a.	0.467	n.a.
SD => C	0.075	0.151	0	0
SE => C	0.225	0.417	0	0

	Min Width	
	High	**Low**
C	0.376	0.326
RN	n.a.	0.360

DFSCP1 is a static, master-slave Scan D flip-flop with 1x drive strength. SCAN ENABLE switches between normal DATA input and SCAN DATA input. PRESET and CLEAR are asynchronous and active low.

Truth Table

C	D	RN	SD	SE	SN	Q	QN
↑	0	1	X	0	1	0	1
↑	X	1	0	1	1	0	1
↑	X	1	1	1	1	1	0
↑	1	1	X	0	1	1	0
X	X	0	X	X	0	0	0
X	X	0	X	X	1	0	1
X	X	1	X	X	0	1	0



Capacitance

Pin	Cap [pF]
C	0.004
D	0.004
RN	0.015
SD	0.009
SE	0.006
SN	0.014

Area

0.621 mils^2
401 µm^2

Power

1.53 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay C => Q	0.50	2.16	0.74	2.39	0.60	1.69	0.81	1.89
Delay C => QN	0.70	2.32	0.91	2.50	0.60	1.71	0.84	1.92
Delay RN => Q	0.11	1.82	0.11	1.81	0.20	1.26	0.64	1.69
Delay RN => QN	0.30	1.98	0.71	2.37	n.a.	n.a.	n.a.	n.a.
Delay SN => Q	0.40	2.04	0.83	2.43	n.a.	n.a.	n.a.	n.a.
Delay SN => QN	0.15	1.84	0.21	1.85	0.21	1.34	0.64	1.76
Slew C => Q	0.12	4.36	0.17	4.25	0.12	2.40	0.10	2.40
Slew C => QN	0.11	4.25	0.11	4.25	0.11	2.41	0.10	2.39
Slew RN => Q	0.17	4.41	0.17	4.30	0.16	2.45	0.17	2.43
Slew RN => QN	0.17	4.34	0.17	4.32	n.a.	n.a.	n.a.	n.a.
Slew SN => Q	0.17	4.33	0.17	4.30	n.a.	n.a.	n.a.	n.a.
Slew SN => QN	0.14	4.34	0.17	4.32	0.17	2.48	0.18	2.43

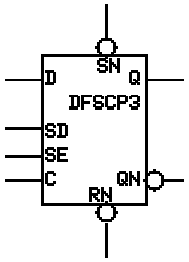
	Setup		Hold	
	rise	fall	rise	fall
D => C	0.281	0	0	0
RN => C	0	n.a.	0.456	n.a.
SD => C	0	0.002	0	0
SE => C	0.189	0.463	0	0
SN => C	0	n.a.	0.29	n.a.

	Min Width	
	High	Low
C	0.376	0.326
RN	n.a.	0.360
SN	n.a.	0.380

DFSCP3 is a static, master-slave Scan D flip-flop with 3x drive strength. SCAN ENABLE switches between normal DATA input and SCAN DATA input. CLEAR and PRESET are asynchronous and active low.

Truth Table

C	D	RN	SD	SE	SN	Q	QN
↑	0	1	X	0	1	0	1
↑	X	1	0	1	1	0	1
↑	X	1	1	1	1	1	0
↑	1	1	X	0	1	1	0
X	X	0	X	X	0	0	0
X	X	0	X	X	1	0	1
X	X	1	X	X	0	1	0



Capacitance

Pin	Cap [pF]
C	0.004
D	0.004
RN	0.015
SD	0.009
SE	0.006
SN	0.014

Area

0.649 mils^2
419 µm^2

Power

2.06 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay C => Q	0.50	2.11	0.74	2.32	0.64	1.75	0.81	1.88
Delay C => QN	0.80	2.33	0.91	2.48	0.70	1.74	0.94	1.99
Delay RN => Q	0.16	1.70	0.20	1.77	0.22	1.31	0.65	1.76
Delay RN => QN	0.40	1.95	0.84	2.40	n.a.	n.a.	n.a.	n.a.
Delay SN => Q	0.43	1.99	0.83	2.38	n.a.	n.a.	n.a.	n.a.
Delay SN => QN	0.20	1.75	0.23	1.83	0.24	1.36	0.66	1.80
Slew C => Q	0.10	4.01	0.11	4.02	0.12	2.31	0.12	2.31
Slew C => QN	0.10	4.03	0.10	4.03	0.11	2.32	0.15	2.32
Slew RN => Q	0.17	4.04	0.17	4.08	0.11	2.38	0.15	2.36
Slew RN => QN	0.17	4.04	0.17	4.05	n.a.	n.a.	n.a.	n.a.
Slew SN => Q	0.17	4.10	0.17	4.06	n.a.	n.a.	n.a.	n.a.
Slew SN => QN	0.17	4.10	0.17	4.09	0.17	2.38	0.17	2.39

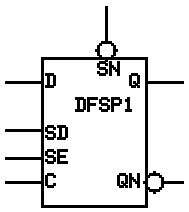
	Setup		Hold	
	rise	fall	rise	fall
D => C	0.28	0.25	0	0
RN => C	0	n.a.	0.456	n.a.
SD => C	0.102	0.112	0	0
SE => C	0.188	0.462	0	0
SN => C	0	n.a.	0.29	n.a.

	Min Width	
	High	Low
C	0.376	0.326
RN	n.a.	0.360
SN	n.a.	0.380

DFSP1 is a static, master-slave Scan D flip-flop with 1x drive strength. SCAN ENABLE switches between normal DATA input and SCAN DATA input. PRESET is asynchronous and active low.

Truth Table

C	D	SD	SE	SN	Q	QN
↑	0	X	0	1	0	1
↑	X	0	1	1	0	1
↑	X	1	1	1	1	0
↑	1	X	0	1	1	0
X	X	X	X	0	1	0



Capacitance

Pin	Cap [pF]
C	0.004
D	0.004
SD	0.009
SE	0.006
SN	0.012

Area

0.592 mils^2
382 µm^2

Power

1.44 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay C => Q	0.51	2.15	0.73	2.35	0.56	1.64	0.71	1.82
Delay C => QN	0.60	2.28	0.81	2.46	0.65	1.72	0.84	1.91
Delay SN => Q	0.40	2.05	0.84	2.46	n.a.	n.a.	n.a.	n.a.
Delay SN => QN	n.a.	n.a.	n.a.	n.a.	0.20	1.30	0.63	1.72
Slew C => Q	0.12	4.26	0.12	4.26	0.10	2.39	0.09	2.39
Slew C => QN	0.11	4.25	0.11	4.25	0.10	2.39	0.10	2.39
Slew SN => Q	0.12	4.31	0.17	4.31	n.a.	n.a.	n.a.	n.a.
Slew SN => QN	n.a.	n.a.	n.a.	n.a.	0.17	2.43	0.16	2.39

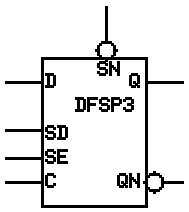
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
D => C	0.222	0.113	0	0
SD => C	0	0.002	0	0
SE => C	0.17	0.458	0	0
SN => C	0	n.a.	0.326	n.a.

	Min Width	
	High	**Low**
C	0.376	0.326
SN	n.a.	0.380

DFSP3 is a static, master-slave Scan D flip-flop with 3x drive strength. SCAN ENABLE switches between normal DATA input and SCAN DATA input. PRESET is asynchronous and active low.

Truth Table

C	D	SD	SE	SN	Q	QN
↑	0	X	0	1	0	1
↑	X	0	1	1	0	1
↑	X	1	1	1	1	0
↑	1	X	0	1	1	0
X	X	X	X	0	1	0



Capacitance

Pin	Cap [pF]
C	0.004
D	0.004
SD	0.009
SE	0.006
SN	0.012

Area

0.621 mils^2
401 µm^2

Power

2 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay C => Q	0.54	2.12	0.74	2.32	0.60	1.68	0.72	1.81
Delay C => QN	0.70	2.26	0.91	2.41	0.73	1.81	0.94	1.98
Delay SN => Q	0.50	2.06	0.92	2.45	n.a.	n.a.	n.a.	n.a.
Delay SN => QN	n.a.	n.a.	n.a.	n.a.	0.23	1.31	0.64	1.74
Slew C => Q	0.11	4.01	0.10	4.03	0.10	2.31	0.10	2.31
Slew C => QN	0.10	4.02	0.10	4.02	0.10	2.32	0.10	2.32
Slew SN => Q	0.11	4.05	0.12	4.07	n.a.	n.a.	n.a.	n.a.
Slew SN => QN	n.a.	n.a.	n.a.	n.a.	0.17	2.35	0.17	2.36

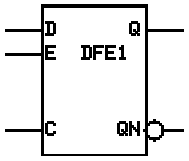
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
D => C	0.271	0	0	0
SD => C	0	0.002	0	0
SE => C	0.168	0.456	0	0
SN => C	0	n.a.	0.326	n.a.

	Min Width	
	High	**Low**
C	0.376	0.326
SN	n.a.	0.380

DFE1 is a static, master-slave D flip-flop with 1x drive strength and active high load enable.

Truth Table

C	D	E	Q	QN
↑	0	1	0	1
↑	1	1	1	0



Capacitance

Pin	Cap [pF]
C	0.004
D	0.009
E	0.006

Area

0.508 mils^2
328 µm^2

Power

1.35 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay C => Q	0.52	2.16	0.69	2.34	0.56	1.63	0.71	1.79
Delay C => QN	0.67	2.31	0.83	2.47	0.62	1.67	0.80	1.85
Slew C => Q	0.12	4.25	0.12	4.25	0.10	2.38	0.10	2.39
Slew C => QN	0.11	4.24	0.11	4.23	0.09	2.39	0.09	2.40

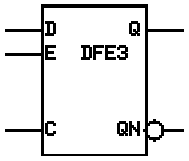
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
D => C	0.069	0.12	0	0
E => C	0.196	0.368	0	0

	Min Width	
	High	**Low**
C	0.376	0.326

DFE3 is a static, master-slave D flip-flop with 3x drive strength and active high load enable.

Truth Table

C	D	E	Q	QN
↑	0	1	0	1
↑	1	1	1	0



Capacitance

Pin	Cap [pF]
C	0.004
D	0.009
E	0.006

Area

0.536 mils^2
346 µm^2

Power

2.03 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay C => Q	0.54	2.10	0.72	2.28	0.59	1.66	0.74	1.81
Delay C => QN	0.76	2.30	0.92	2.45	0.70	1.74	0.88	1.92
Slew C => Q	0.10	4.01	0.10	4.00	0.10	2.30	0.10	2.31
Slew C => QN	0.10	4.01	0.10	4.02	0.10	2.32	0.10	2.31

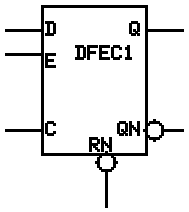
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
D => C	0	0.092	0	0
E => C	0.194	0.365	0	0

	Min Width	
	High	**Low**
C	0.376	0.326

DFEC1 is a static, master-slave D flip-flop with 1x drive strength and active high load enable. CLEAR is asynchronous and active low.

Truth Table

C	D	E	RN	Q	QN
↑	0	1	1	0	1
↑	1	1	1	1	0
X	X	X	0	0	1



Capacitance

Pin	Cap [pF]
C	0.004
D	0.009
E	0.006
RN	0.011

Area

0.536 mils^2
346 µm^2

Power

1.4 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay C => Q	0.49	2.14	0.66	2.31	0.61	1.69	0.77	1.85
Delay C => QN	0.73	2.36	0.89	2.53	0.59	1.64	0.76	1.81
Delay RN => Q	n.a.	n.a.	n.a.	n.a.	0.28	1.42	0.70	1.84
Delay RN => QN	0.50	2.14	0.93	2.56	n.a.	n.a.	n.a.	n.a.
Slew C => Q	0.12	4.25	0.12	4.24	0.10	2.36	0.11	2.39
Slew C => QN	0.12	4.23	0.11	4.25	0.09	2.39	0.09	2.38
Slew RN => Q	n.a.	n.a.	n.a.	n.a.	0.15	2.41	0.18	2.40
Slew RN => QN	0.14	4.26	0.15	4.24	n.a.	n.a.	n.a.	n.a.

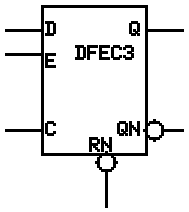
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
D => C	0	0.14	0	0
E => C	0.215	0.362	0	0
RN => C	0	n.a.	0.465	n.a.

	Min Width	
	High	**Low**
C	0.376	0.326
RN	n.a.	0.360

DFEC3 is a static, master-slave D flip-flop with 3x drive strength and active high load enable. CLEAR is asynchronous and active low.

Truth Table

C	D	E	RN	Q	QN
↑	0	1	1	0	1
↑	1	1	1	1	0
X	X	X	0	0	1



Capacitance

Pin	Cap [pF]
C	0.004
D	0.009
E	0.006
RN	0.011

Area

0.564 mils^2
364 µm^2

Power

2.08 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay C => Q	0.50	2.07	0.68	2.24	0.64	1.72	0.80	1.89
Delay C => QN	0.82	2.36	0.98	2.52	0.66	1.70	0.84	1.87
Delay RN => Q	n.a.	n.a.	n.a.	n.a.	0.32	1.45	0.74	1.88
Delay RN => QN	0.59	2.14	1.02	2.56	n.a.	n.a.	n.a.	n.a.
Slew C => Q	0.10	4.02	0.10	4.03	0.11	2.29	0.12	2.32
Slew C => QN	0.10	4.03	0.11	4.02	0.09	2.31	0.09	2.31
Slew RN => Q	n.a.	n.a.	n.a.	n.a.	0.16	2.33	0.19	2.33
Slew RN => QN	0.12	4.03	0.13	4.02	n.a.	n.a.	n.a.	n.a.

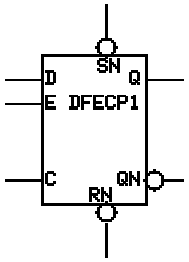
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
D => C	0	0.137	0	0
E => C	0.214	0.359	0	0
RN => C	0	n.a.	0.465	n.a.

	Min Width	
	High	**Low**
C	0.376	0.326
RN	n.a.	0.360

DFECP1 is a static, master-slave D flip-flop with 1x drive strength and active high load enable. PRESET and CLEAR are asynchronous and active low.

Truth Table

C	D	E	RN	SN	Q	QN
↑	0	1	1	1	0	1
↑	1	1	1	1	1	0
X	X	X	0	0	0	0
X	X	X	0	1	0	1
X	X	X	1	0	1	0



Capacitance

Pin	Cap [pF]
C	0.004
D	0.009
E	0.006
RN	0.015
SN	0.014

Area

0.592 mils^2
382 µm^2

Power

1.41 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay C => Q	0.50	2.17	0.72	2.34	0.60	1.69	0.81	1.89
Delay C => QN	0.70	2.36	0.91	2.54	0.65	1.70	0.83	1.90
Delay RN => Q	0.20	1.89	0.30	1.99	0.30	1.49	0.72	1.92
Delay RN => QN	0.44	2.08	0.86	2.50	n.a.	n.a.	n.a.	n.a.
Delay SN => Q	0.43	2.14	0.84	2.55	n.a.	n.a.	n.a.	n.a.
Delay SN => QN	0.15	1.83	0.21	1.85	0.21	1.33	0.64	1.76
Slew C => Q	0.12	4.24	0.11	4.24	0.11	2.39	0.11	2.38
Slew C => QN	0.11	4.25	0.11	4.24	0.10	2.38	0.10	2.39
Slew RN => Q	0.15	4.30	0.19	4.31	0.15	2.44	0.19	2.44
Slew RN => QN	0.17	4.25	0.17	4.25	n.a.	n.a.	n.a.	n.a.
Slew SN => Q	0.17	4.31	0.17	4.31	n.a.	n.a.	n.a.	n.a.
Slew SN => QN	0.14	4.32	0.17	4.31	0.17	2.40	0.16	2.39

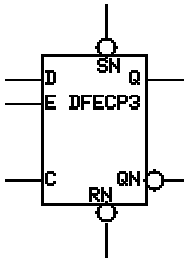
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
D => C	0.095	0.102	0	0
E => C	0.179	0.402	0	0
RN => C	0	n.a.	0.455	n.a.
SN => C	0	n.a.	0.294	n.a.

	Min Width	
	High	**Low**
C	0.376	0.326
RN	n.a.	0.360
SN	n.a.	0.380

DFECP3 is a static, master-slave D flip-flop with 3x drive strength and active high load enable. PRESET and CLEAR are asynchronous and active low.

Truth Table

C	D	E	RN	SN	Q	QN
↑	0	1	1	1	0	1
↑	1	1	1	1	1	0
X	X	X	0	0	0	0
X	X	X	0	1	0	1
X	X	X	1	0	1	0



Capacitance

Pin	Cap [pF]
C	0.004
D	0.009
E	0.006
RN	0.015
SN	0.014

Area

0.621 mils^2
401 µm^2

Power

2.11 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay C => Q	0.50	2.08	0.72	2.29	0.70	1.72	0.81	1.90
Delay C => QN	0.80	2.32	0.91	2.51	0.70	1.74	0.92	1.96
Delay RN => Q	0.20	1.82	0.34	1.93	0.33	1.51	0.77	1.94
Delay RN => QN	0.51	2.06	0.94	2.48	n.a.	n.a.	n.a.	n.a.
Delay SN => Q	0.50	2.11	0.91	2.50	n.a.	n.a.	n.a.	n.a.
Delay SN => QN	0.18	1.74	0.22	1.80	0.24	1.34	0.65	1.76
Slew C => Q	0.11	4.00	0.10	4.00	0.12	2.29	0.12	2.31
Slew C => QN	0.10	4.01	0.10	4.02	0.10	2.32	0.10	2.31
Slew RN => Q	0.13	4.08	0.17	4.09	0.16	2.37	0.19	2.38
Slew RN => QN	0.12	4.03	0.13	4.02	n.a.	n.a.	n.a.	n.a.
Slew SN => Q	0.17	4.04	0.17	4.02	n.a.	n.a.	n.a.	n.a.
Slew SN => QN	0.12	4.07	0.15	4.08	0.17	2.33	0.17	2.33

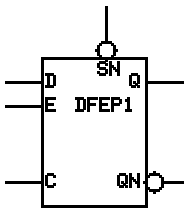
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
D => C	0.094	0.102	0	0
E => C	0.178	0.399	0	0
RN => C	0	n.a.	0.455	n.a.
SN => C	0	n.a.	0.294	n.a.

	Min Width	
	High	**Low**
C	0.376	0.326
RN	n.a.	0.360
SN	n.a.	0.380

DFEP1 is a static, master-slave D flip-flop with 1x drive strength and active high load enable. PRESET is asynchronous and active low.

Truth Table

C	D	E	SN	Q	QN
↑	0	1	1	0	1
↑	1	1	1	1	0
X	X	X	0	1	0



Capacitance

Pin	Cap [pF]
C	0.004
D	0.009
E	0.006
SN	0.010

Area

0.536 mils^2
346 µm^2

Power

1.35 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay C => Q	0.52	2.17	0.69	2.34	0.56	1.64	0.72	1.80
Delay C => QN	0.64	2.29	0.81	2.44	0.66	1.71	0.83	1.89
Delay SN => Q	0.49	2.19	0.90	2.59	n.a.	n.a.	n.a.	n.a.
Delay SN => QN	n.a.	n.a.	n.a.	n.a.	0.20	1.28	0.59	1.69
Slew C => Q	0.12	4.25	0.12	4.24	0.10	2.39	0.10	2.39
Slew C => QN	0.11	4.24	0.11	4.24	0.09	2.38	0.10	2.40
Slew SN => Q	0.16	4.25	0.17	4.25	n.a.	n.a.	n.a.	n.a.
Slew SN => QN	n.a.	n.a.	n.a.	n.a.	0.12	2.40	0.16	2.39

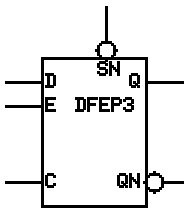
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
D => C	0.093	0.088	0	0
E => C	0.165	0.409	0	0
SN => C	0	n.a.	0.33	n.a.

	Min Width	
	High	**Low**
C	0.376	0.326
SN	n.a.	0.380

DFEP3 is a static, master-slave D flip-flop with 3x drive strength and active high load enable. PRESET is asynchronous and active low.

Truth Table

C	D	E	SN	Q	QN
↑	0	1	1	0	1
↑	1	1	1	1	0
X	X	X	0	1	0



Capacitance

Pin	Cap [pF]
C	0.004
D	0.009
E	0.006
SN	0.010

Area

0.564 mils^2
364 µm^2

Power

2.06 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay C => Q	0.55	2.11	0.72	2.28	0.59	1.67	0.75	1.83
Delay C => QN	0.71	2.26	0.87	2.41	0.74	1.78	0.92	1.96
Delay SN => Q	0.59	2.18	1.01	2.60	n.a.	n.a.	n.a.	n.a.
Delay SN => QN	n.a.	n.a.	n.a.	n.a.	0.23	1.31	0.64	1.72
Slew C => Q	0.10	4.02	0.10	4.01	0.10	2.30	0.10	2.30
Slew C => QN	0.10	4.02	0.10	4.00	0.10	2.29	0.10	2.31
Slew SN => Q	0.15	4.02	0.15	4.03	n.a.	n.a.	n.a.	n.a.
Slew SN => QN	n.a.	n.a.	n.a.	n.a.	0.11	2.31	0.16	2.31

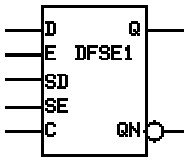
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
D => C	0.094	0.083	0	0
E => C	0.163	0.406	0	0
SN => C	0	n.a.	0.33	n.a.

	Min Width	
	High	**Low**
C	0.376	0.326
SN	n.a.	0.380

DFSE1 is a static, master-slave Scan D flip-flop with 1x drive strength and active high load enable. SCAN ENABLE switches between normal DATA input and SCAN DATA input.

Truth Table

C	D	E	SD	SE	Q	QN
↑	0	1	X	0	0	1
↑	X	X	0	1	0	1
↑	X	X	1	1	1	0
↑	1	1	X	0	1	0



Capacitance

Pin	Cap [pF]
C	0.004
D	0.009
E	0.006
SD	0.009
SE	0.006

Area

0.649 mils^2
419 µm^2

Power

1.41 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay C => Q	0.60	2.23	0.80	2.42	0.61	1.80	0.80	1.93
Delay C => QN	0.80	2.40	0.92	2.57	0.70	1.74	0.93	1.98
Slew C => Q	0.15	4.26	0.14	4.25	0.13	2.40	0.13	2.40
Slew C => QN	0.13	4.25	0.11	4.25	0.10	2.40	0.10	2.40

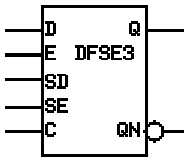
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
D => C	0.197	0.279	0	0
E => C	0.353	0.529	0	0
SD => C	0.069	0.121	0	0
SE => C	0.202	0.378	0	0

	Min Width	
	High	**Low**
C	0.376	0.326

DFSE3 is a static, master-slave Scan D flip-flop with 3x drive strength and active high load enable. SCAN ENABLE switches between normal DATA input and SCAN DATA input.

Truth Table

C	D	E	SD	SE	Q	QN
↑	0	1	X	0	0	1
↑	X	X	0	1	0	1
↑	X	X	1	1	1	0
↑	1	1	X	0	1	0



Capacitance

Pin	Cap [pF]
C	0.004
D	0.009
E	0.006
SD	0.009
SE	0.006

Area

0.677 mils^2
437 µm^2

Power

2.05 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay C => Q	0.60	2.21	0.83	2.41	0.70	1.83	0.81	1.94
Delay C => QN	0.90	2.39	1.01	2.58	0.80	1.86	1.03	2.00
Slew C => Q	0.14	4.01	0.13	4.04	0.12	2.32	0.13	2.33
Slew C => QN	0.11	4.04	0.11	4.02	0.11	2.32	0.10	2.31

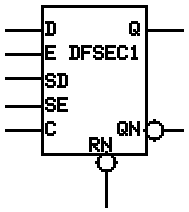
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
D => C	0.103	0	0	0
E => C	0.341	0.526	0	0
SD => C	0	0.002	0	0
SE => C	0.202	0.378	0	0

	Min Width	
	High	**Low**
C	0.376	0.326

DFSEC1 is a static, master-slave Scan D flip-flop with 1x drive strength and active high load enable. SCAN ENABLE switches between normal DATA input and SCAN DATA input. CLEAR is asynchronous and active low.

Truth Table

C	D	E	RN	SD	SE	Q	QN
↑	0	1	1	X	0	0	1
↑	X	X	1	0	1	0	1
↑	X	X	1	1	1	1	0
↑	1	1	1	X	0	1	0
X	X	X	0	X	X	0	1



Capacitance

Pin	Cap [pF]
C	0.004
D	0.009
E	0.006
RN	0.011
SD	0.010
SE	0.006

Area

0.677 mils^2
437 µm^2

Power

1.4 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay C => Q	0.51	2.23	0.73	2.41	0.70	1.85	0.84	2.01
Delay C => QN	0.80	2.46	1.00	2.61	0.67	1.74	0.83	1.93
Delay RN => Q	n.a.	n.a.	n.a.	n.a.	0.30	1.46	0.75	1.93
Delay RN => QN	0.57	2.17	1.01	2.66	n.a.	n.a.	n.a.	n.a.
Slew C => Q	0.17	4.26	0.14	4.25	0.17	2.40	0.17	2.40
Slew C => QN	0.17	4.32	0.12	4.27	0.17	2.38	0.10	2.40
Slew RN => Q	n.a.	n.a.	n.a.	n.a.	0.18	2.50	0.22	2.46
Slew RN => QN	0.17	4.32	0.17	4.32	n.a.	n.a.	n.a.	n.a.

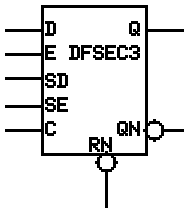
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
D => C	0.191	0	0	0
E => C	0.381	0.52	0	0
RN => C	0	n.a.	0.466	n.a.
SD => C	0.061	0	0	0
SE => C	0.221	0.251	0	0

	Min Width	
	High	**Low**
C	0.376	0.326
RN	n.a.	0.360

DFSEC3 is a static, master-slave Scan D flip-flop with 3x drive strength and active high load enable. SCAN ENABLE switches between normal DATA input and SCAN DATA input. CLEAR is asynchronous and active low.

Truth Table

C	D	E	RN	SD	SE	Q	QN
↑	0	1	1	X	0	0	1
↑	X	X	1	0	1	0	1
↑	X	X	1	1	1	1	0
↑	1	1	1	X	0	1	0
X	X	X	0	X	X	0	1



Capacitance

Pin	Cap [pF]
C	0.004
D	0.009
E	0.006
RN	0.011
SD	0.010
SE	0.006

Area

0.705 mils^2
455 µm^2

Power

2.13 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay C => Q	0.57	2.16	0.74	2.35	0.70	1.82	0.90	2.03
Delay C => QN	0.90	2.45	1.10	2.59	0.70	1.80	0.94	1.99
Delay RN => Q	n.a.	n.a.	n.a.	n.a.	0.39	1.49	0.81	1.98
Delay RN => QN	0.70	2.19	1.11	2.64	n.a.	n.a.	n.a.	n.a.
Slew C => Q	0.17	4.02	0.17	4.04	0.17	2.41	0.17	2.33
Slew C => QN	0.17	4.03	0.14	4.07	0.17	2.31	0.10	2.32
Slew RN => Q	n.a.	n.a.	n.a.	n.a.	0.17	2.38	0.19	2.38
Slew RN => QN	0.17	4.14	0.17	4.09	n.a.	n.a.	n.a.	n.a.

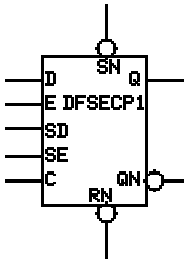
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
D => C	0.191	0	0	0
E => C	0.361	0.517	0	0
RN => C	0	n.a.	0.466	n.a.
SD => C	0.061	0	0	0
SE => C	0.222	0.261	0	0

	Min Width	
	High	**Low**
C	0.376	0.326
RN	n.a.	0.360

DFSECP1 is a static, master-slave Scan D flip-flop with 1x drive strength and active high load enable. SCAN ENABLE switches between normal DATA input and SCAN DATA input. CLEAR and PRESET are asynchronous and active low.

Truth Table

C	D	E	RN	SD	SE	SN	Q	QN
↑	0	1	1	X	0	1	0	1
↑	X	X	1	0	1	1	0	1
↑	X	X	1	1	1	1	1	0
↑	1	1	1	X	0	1	1	0
X	X	X	0	X	X	0	0	0
X	X	X	0	X	X	1	0	1
X	X	X	1	X	X	0	1	0



Capacitance

Pin	Cap [pF]
C	0.004
D	0.009
E	0.006
RN	0.015
SD	0.009
SE	0.006
SN	0.014

Area

0.705 mils^2
455 µm^2

Power

1.59 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay C => Q	0.56	2.23	0.74	2.43	0.70	1.82	0.88	2.04
Delay C => QN	0.80	2.41	0.92	2.61	0.70	1.79	0.94	1.97
Delay RN => Q	0.20	1.95	0.30	2.06	0.31	1.60	0.80	2.00
Delay RN => QN	0.50	2.13	0.91	2.59	n.a.	n.a.	n.a.	n.a.
Delay SN => Q	0.43	2.21	0.86	2.65	n.a.	n.a.	n.a.	n.a.
Delay SN => QN	0.14	1.84	0.22	1.88	0.21	1.35	0.64	1.78
Slew C => Q	0.17	4.31	0.17	4.27	0.16	2.39	0.14	2.40
Slew C => QN	0.12	4.25	0.12	4.25	0.17	2.44	0.17	2.40
Slew RN => Q	0.17	4.37	0.26	4.35	0.18	2.51	0.27	2.51
Slew RN => QN	0.17	4.38	0.17	4.30	n.a.	n.a.	n.a.	n.a.
Slew SN => Q	0.17	4.37	0.17	4.32	n.a.	n.a.	n.a.	n.a.
Slew SN => QN	0.17	4.39	0.17	4.35	0.17	2.45	0.21	2.42

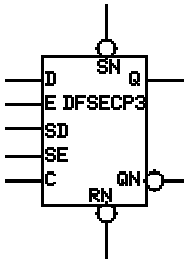
	Setup		Hold	
	rise	fall	rise	fall
D => C	0.234	0.242	0	0
E => C	0.316	0.577	0	0
RN => C	0	n.a.	0.456	n.a.
SD => C	0.094	0.102	0	0
SE => C	0.185	0.416	0	0
SN => C	0	n.a.	0.29	n.a.

	Min Width	
	High	Low
C	0.376	0.326
RN	n.a.	0.360
SN	n.a.	0.380

DFSECP3 is a static, master-slave Scan D flip-flop with 3x drive strength and active high load enable. SCAN ENABLE switches between normal DATA input and SCAN DATA input. CLEAR and PRESET are asynchronous and active low.

Truth Table

C	D	E	RN	SD	SE	SN	Q	QN
↑	0	1	1	X	0	1	0	1
↑	X	X	1	0	1	1	0	1
↑	X	X	1	1	1	1	1	0
↑	1	1	1	X	0	1	1	0
X	X	X	0	X	X	0	0	0
X	X	X	0	X	X	1	0	1
X	X	X	1	X	X	0	1	0



Capacitance

Pin	Cap [pF]
C	0.004
D	0.009
E	0.006
RN	0.015
SD	0.009
SE	0.006
SN	0.014

Area

0.733 mils^2
473 µm^2

Power

2.17 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay C => Q	0.60	2.15	0.76	2.37	0.70	1.83	0.91	2.05
Delay C => QN	0.85	2.36	1.01	2.55	0.80	1.82	1.04	2.06
Delay RN => Q	0.20	1.85	0.40	2.02	0.40	1.58	0.81	2.02
Delay RN => QN	0.58	2.11	1.01	2.56	n.a.	n.a.	n.a.	n.a.
Delay SN => Q	0.51	2.17	0.93	2.57	n.a.	n.a.	n.a.	n.a.
Delay SN => QN	0.19	1.76	0.22	1.85	0.26	1.35	0.73	1.77
Slew C => Q	0.17	4.10	0.17	4.11	0.15	2.34	0.14	2.33
Slew C => QN	0.10	4.03	0.10	4.02	0.17	2.33	0.17	2.38
Slew RN => Q	0.17	4.17	0.18	4.19	0.18	2.44	0.30	2.43
Slew RN => QN	0.17	4.11	0.17	4.07	n.a.	n.a.	n.a.	n.a.
Slew SN => Q	0.17	4.13	0.17	4.03	n.a.	n.a.	n.a.	n.a.
Slew SN => QN	0.17	4.11	0.17	4.08	0.17	2.38	0.17	2.38

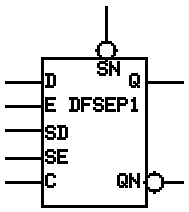
	Setup		Hold	
	rise	fall	rise	fall
D => C	0.232	0.24	0	0
E => C	0.314	0.574	0	0
RN => C	0	n.a.	0.456	n.a.
SD => C	0	0.002	0	0
SE => C	0.185	0.416	0	0
SN => C	0	n.a.	0.29	n.a.

	Min Width	
	High	Low
C	0.376	0.326
RN	n.a.	0.360
SN	n.a.	0.380

DFSEP1 is a static, master-slave Scan D flip-flop with 1x drive strength and active high load enable. SCAN ENABLE switches between normal DATA input and SCAN DATA input. PRESET is asynchronous and active low.

Truth Table

C	D	E	SD	SE	SN	Q	QN
↑	0	1	X	0	1	0	1
↑	X	X	0	1	1	0	1
↑	X	X	1	1	1	1	0
↑	1	1	X	0	1	1	0
X	X	X	X	X	0	1	0



Capacitance

Pin	Cap [pF]
C	0.004
D	0.009
E	0.006
SD	0.009
SE	0.006
SN	0.010

Area

0.677 mils^2
437 µm^2

Power

1.52 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay C => Q	0.60	2.27	0.84	2.45	0.62	1.77	0.81	1.95
Delay C => QN	0.70	2.38	0.91	2.55	0.73	1.84	0.94	2.01
Delay SN => Q	0.50	2.24	0.95	2.72	n.a.	n.a.	n.a.	n.a.
Delay SN => QN	n.a.	n.a.	n.a.	n.a.	0.21	1.31	0.63	1.75
Slew C => Q	0.17	4.25	0.17	4.28	0.13	2.40	0.13	2.40
Slew C => QN	0.12	4.25	0.12	4.25	0.17	2.41	0.17	2.47
Slew SN => Q	0.18	4.33	0.17	4.33	n.a.	n.a.	n.a.	n.a.
Slew SN => QN	n.a.	n.a.	n.a.	n.a.	0.17	2.42	0.17	2.43

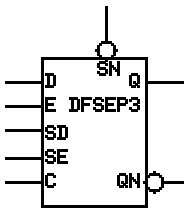
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
D => C	0.236	0.223	0	0
E => C	0	0.589	0	0
SD => C	0	0.002	0	0
SE => C	0.171	0.418	0	0
SN => C	0	n.a.	0.326	n.a.

	Min Width	
	High	**Low**
C	0.376	0.326
SN	n.a.	0.380

DFSEP3 is a static, master-slave Scan D flip-flop with 3x drive strength and active high load enable. SCAN ENABLE switches between normal DATA input and SCAN DATA input. PRESET is asynchronous and active low.

Truth Table

C	D	E	SD	SE	SN	Q	QN
↑	0	1	X	0	1	0	1
↑	X	X	0	1	1	0	1
↑	X	X	1	1	1	1	0
↑	1	1	X	0	1	1	0
X	X	X	X	X	0	1	0



Capacitance

Pin	Cap [pF]
C	0.004
D	0.009
E	0.006
SD	0.009
SE	0.006
SN	0.010

Area

0.705 mils^2
455 µm^2

Power

2.15 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay C => Q	0.60	2.23	0.84	2.43	0.70	1.82	0.81	1.99
Delay C => QN	0.80	2.35	0.98	2.48	0.82	1.92	1.04	2.09
Delay SN => Q	0.60	2.27	1.02	2.70	n.a.	n.a.	n.a.	n.a.
Delay SN => QN	n.a.	n.a.	n.a.	n.a.	0.24	1.33	0.65	1.76
Slew C => Q	0.17	4.07	0.17	4.02	0.13	2.33	0.14	2.33
Slew C => QN	0.10	4.03	0.10	4.02	0.17	2.36	0.17	2.34
Slew SN => Q	0.17	4.09	0.17	4.05	n.a.	n.a.	n.a.	n.a.
Slew SN => QN	n.a.	n.a.	n.a.	n.a.	0.17	2.38	0.17	2.35

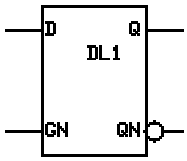
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
D => C	0.181	0.211	0	0
E => C	0.189	0.587	0	0
SD => C	0	0.002	0	0
SE => C	0.171	0.418	0	0
SN => C	0	n.a.	0.326	n.a.

	Min Width	
	High	**Low**
C	0.376	0.326
SN	n.a.	0.380

DL1 is a transparent D-latch with 1x drive strength. The Q output follows the D input when GN is low. The Q output is independent of D when GN is high and retains the value of D just prior to the rising edge on GN.

Truth Table

D	GN	Q	QN
0	0	0	1
1	0	1	0



Capacitance

Pin	Cap [pF]
D	0.004
GN	0.007

Area

0.31 mils^2
200 µm^2

Power

1.19 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay D => Q	0.40	2.04	0.52	2.16	0.44	1.48	0.79	1.84
Delay D => QN	0.35	2.00	0.71	2.35	0.31	1.37	0.43	1.49
Delay GN => Q	0.41	2.05	0.71	2.35	0.39	1.44	0.75	1.80
Delay GN => QN	0.31	1.96	0.67	2.31	0.32	1.38	0.61	1.68
Slew D => Q	0.10	4.23	0.10	4.23	0.07	2.37	0.07	2.38
Slew D => QN	0.11	4.24	0.11	4.23	0.09	2.39	0.09	2.38
Slew GN => Q	0.10	4.23	0.10	4.23	0.07	2.38	0.07	2.39
Slew GN => QN	0.11	4.24	0.11	4.24	0.08	2.39	0.09	2.39

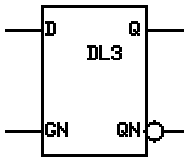
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
D => GN	0.219	0.415	0	0

	Min Width	
	High	**Low**
GN	n.a.	0.258

DL3 is a transparent D-latch with 3x drive strength. The Q output follows the D input when GN is low. The Q output is independent of D when GN is high and retains the value of D just prior to the rising edge on GN.

Truth Table

D	GN	Q	QN
0	0	0	1
1	0	1	0



Capacitance

Pin	Cap [pF]
D	0.004
GN	0.007

Area

0.31 mils^2
200 µm^2

Power

2.65 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay D => Q	0.50	2.04	0.62	2.16	0.54	1.57	0.90	1.93
Delay D => QN	0.40	1.95	0.76	2.31	0.35	1.40	0.47	1.53
Delay GN => Q	0.51	2.05	0.81	2.34	0.49	1.52	0.85	1.88
Delay GN => QN	0.35	1.90	0.71	2.26	0.36	1.42	0.66	1.71
Slew D => Q	0.10	4.01	0.10	4.01	0.09	2.31	0.09	2.31
Slew D => QN	0.11	4.04	0.11	4.01	0.10	2.31	0.11	2.32
Slew GN => Q	0.10	4.02	0.10	4.00	0.09	2.30	0.09	2.31
Slew GN => QN	0.11	4.03	0.11	4.03	0.10	2.32	0.10	2.30

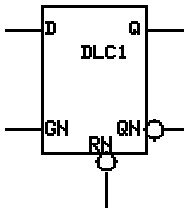
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
D => GN	0.273	0.464	0	0

	Min Width	
	High	**Low**
GN	n.a.	0.258

DLC1 is a transparent D-latch with an active low asynchronous CLEAR and 1x drive strength. The Q output follows the D input when GN is low. The Q output is independent of D when GN is high and retains the value of D just prior to the rising edge on GN.

Truth Table

D	GN	RN	Q	QN
0	0	1	0	1
X	X	0	0	1
1	0	1	1	0



Capacitance

Pin	Cap [pF]
D	0.007
GN	0.006
RN	0.010

Area

0.339 mils^2
219 µm^2

Power

1.36 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay D => Q	0.35	1.99	0.28	1.92	0.48	1.53	0.90	1.95
Delay D => QN	0.36	2.01	0.78	2.43	0.28	1.35	0.21	1.28
Delay GN => Q	0.38	2.02	0.68	2.32	0.43	1.48	0.79	1.84
Delay GN => QN	0.31	1.96	0.67	2.31	0.31	1.38	0.61	1.68
Delay RN => Q	0.35	1.99	0.38	2.02	0.18	1.26	0.57	1.66
Delay RN => QN	0.37	2.01	0.77	2.40	0.28	1.34	0.27	1.34
Slew D => Q	0.10	4.23	0.10	4.23	0.08	2.39	0.08	2.38
Slew D => QN	0.11	4.25	0.11	4.24	0.09	2.38	0.09	2.38
Slew GN => Q	0.10	4.23	0.10	4.24	0.08	2.38	0.08	2.39
Slew GN => QN	0.11	4.25	0.11	4.25	0.09	2.39	0.09	2.39
Slew RN => Q	0.10	4.24	0.10	4.24	0.10	2.39	0.14	2.38
Slew RN => QN	0.11	4.24	0.12	4.24	0.09	2.38	0.09	2.38

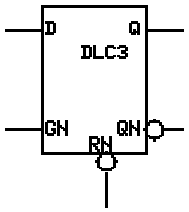
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
D => GN	0.132	0.442	0	0
RN => GN	0	n.a.	0	n.a.

	Min Width	
	High	**Low**
GN	n.a.	0.258
RN	n.a.	0.265

DLC3 is a transparent D-latch with an active low asynchronous CLEAR and 3x drive strength. The Q output follows the D input when GN is low. The Q output is independent of D when GN is high and retains the value of D just prior to the rising edge on GN.

Truth Table

D	GN	RN	Q	QN
0	0	1	0	1
X	X	0	0	1
1	0	1	1	0



Capacitance

Pin	Cap [pF]
D	0.007
GN	0.006
RN	0.010

Area

0.339 mils^2
219 µm^2

Power

2.47 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay D => Q	0.43	1.97	0.36	1.90	0.58	1.62	1.00	2.04
Delay D => QN	0.40	1.96	0.82	2.38	0.33	1.38	0.26	1.31
Delay GN => Q	0.46	2.00	0.76	2.30	0.52	1.56	0.89	1.93
Delay GN => QN	0.35	1.90	0.71	2.26	0.35	1.41	0.65	1.71
Delay RN => Q	0.43	1.97	0.46	2.00	0.22	1.30	0.63	1.70
Delay RN => QN	0.48	2.01	0.89	2.42	0.32	1.38	0.31	1.37
Slew D => Q	0.09	4.00	0.09	4.01	0.09	2.29	0.09	2.31
Slew D => QN	0.11	4.03	0.11	4.02	0.10	2.31	0.10	2.31
Slew GN => Q	0.09	4.02	0.09	4.01	0.09	2.29	0.09	2.29
Slew GN => QN	0.10	4.03	0.11	4.03	0.10	2.31	0.10	2.31
Slew RN => Q	0.09	4.00	0.10	4.00	0.11	2.30	0.16	2.30
Slew RN => QN	0.11	4.02	0.11	4.02	0.10	2.31	0.10	2.30

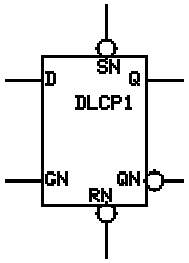
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
D => GN	0.171	0.489	0	0
RN => GN	0	n.a.	0	n.a.

	Min Width	
	High	**Low**
GN	n.a.	0.258
RN	n.a.	0.265

DLCP1 is a transparent D-latch with an active low asynchronous PRESET and CLEAR and 1x drive strength. The Q output follows the D input when GN is low. The Q output is independent of D when GN is high and retains the value of D just prior to the rising edge on GN.

Truth Table

D	GN	RN	SN	Q	QN
0	0	1	1	0	1
X	X	0	0	0	0
X	X	0	1	0	1
X	X	1	0	1	0
1	0	1	1	1	0



Capacitance

Pin	Cap [pF]
D	0.007
GN	0.006
RN	0.012
SN	0.006

Area

0.367 mils^2
237 µm^2

Power

1.41 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay D => Q	0.40	2.04	0.35	1.99	0.45	1.50	0.86	1.91
Delay D => QN	0.33	1.97	0.74	2.38	0.33	1.41	0.28	1.35
Delay GN => Q	0.43	2.08	0.74	2.37	0.40	1.46	0.75	1.80
Delay GN => QN	0.28	1.93	0.63	2.28	0.36	1.44	0.66	1.74
Delay RN => Q	0.40	2.04	0.43	2.07	0.19	1.28	0.58	1.69
Delay RN => QN	0.33	1.98	0.71	2.35	0.33	1.40	0.34	1.41
Delay SN => Q	0.27	1.93	0.65	2.30	0.23	1.29	0.23	1.28
Delay SN => QN	0.12	1.78	0.10	1.75	0.17	1.23	0.54	1.62
Slew D => Q	0.10	4.22	0.10	4.23	0.08	2.36	0.09	2.38
Slew D => QN	0.11	4.24	0.11	4.24	0.10	2.37	0.10	2.38
Slew GN => Q	0.09	4.22	0.10	4.24	0.08	2.38	0.09	2.39
Slew GN => QN	0.11	4.25	0.11	4.25	0.10	2.37	0.10	2.38
Slew RN => Q	0.12	4.30	0.15	4.30	0.11	2.39	0.14	2.39
Slew RN => QN	0.11	4.24	0.11	4.24	0.10	2.38	0.09	2.37
Slew SN => Q	0.12	4.24	0.13	4.23	0.08	2.39	0.09	2.37
Slew SN => QN	0.10	4.29	0.14	4.25	0.09	2.40	0.14	2.39

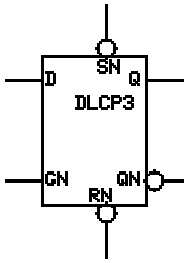
	Setup		Hold	
	rise	fall	rise	fall
D => GN	0.178	0.391	0	0
RN => GN	0	n.a.	0	n.a.
SN => GN	0	n.a.	0	n.a.

	Min Width	
	High	Low
GN	n.a.	0.258
RN	n.a.	0.265
SN	n.a.	0.275

DLCP3 is a transparent D-latch with an active low asynchronous PRESET and CLEAR and 3x drive strength. The Q output follows the D input when GN is low. The Q output is independent of D when GN is high and retains the value of D just prior to the rising edge on GN.

Truth Table

D	GN	RN	SN	Q	QN
0	0	1	1	0	1
X	X	0	0	0	0
X	X	0	1	0	1
X	X	1	0	1	0
1	0	1	1	1	0



Capacitance

Pin	Cap [pF]
D	0.007
GN	0.006
RN	0.012
SN	0.006

Area

0.367 mils^2
237 µm^2

Power

2.83 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay D => Q	0.48	2.02	0.43	1.97	0.53	1.57	0.94	1.99
Delay D => QN	0.35	1.91	0.76	2.32	0.37	1.44	0.32	1.39
Delay GN => Q	0.51	2.05	0.81	2.36	0.48	1.53	0.83	1.88
Delay GN => QN	0.31	1.87	0.65	2.21	0.41	1.47	0.71	1.77
Delay RN => Q	0.48	2.02	0.51	2.06	0.23	1.33	0.64	1.74
Delay RN => QN	0.41	1.97	0.82	2.36	0.37	1.44	0.38	1.44
Delay SN => Q	0.35	1.91	0.75	2.30	0.32	1.36	0.36	1.39
Delay SN => QN	0.14	1.71	0.16	1.72	0.20	1.27	0.60	1.68
Slew D => Q	0.09	4.01	0.09	4.01	0.10	2.30	0.10	2.30
Slew D => QN	0.10	4.03	0.11	4.03	0.11	2.31	0.12	2.31
Slew GN => Q	0.10	4.01	0.09	4.02	0.10	2.32	0.09	2.32
Slew GN => QN	0.11	4.04	0.11	4.04	0.10	2.32	0.10	2.30
Slew RN => Q	0.11	4.04	0.14	4.06	0.12	2.32	0.15	2.32
Slew RN => QN	0.11	4.02	0.12	4.02	0.10	2.30	0.11	2.29
Slew SN => Q	0.11	4.02	0.11	4.02	0.10	2.31	0.10	2.31
Slew SN => QN	0.10	4.08	0.15	4.04	0.11	2.32	0.15	2.32

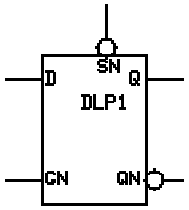
	Setup		Hold	
	rise	fall	rise	fall
D => GN	0.226	0.426	0	0
RN => GN	0	n.a.	0	n.a.
SN => GN	0	n.a.	0	n.a.

	Min Width	
	High	Low
GN	n.a.	0.258
RN	n.a.	0.265
SN	n.a.	0.275

DLP1 is a transparent D-latch with an active low asynchronous PRESET and 1x drive strength. The Q output follows the D input when GN is low. The Q output is independent of D when GN is high and retains the value of D just prior to the rising edge on GN.

Truth Table

D	GN	SN	Q	QN
0	0	1	0	1
X	X	0	1	0
1	0	1	1	0



Capacitance

Pin	Cap [pF]
D	0.004
GN	0.007
SN	0.006

Area

0.31 mils^2
200 µm^2

Power

1.35 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay D => Q	0.46	2.10	0.60	2.24	0.41	1.46	0.75	1.80
Delay D => QN	0.32	1.97	0.67	2.32	0.36	1.43	0.50	1.57
Delay GN => Q	0.47	2.11	0.77	2.41	0.37	1.41	0.72	1.77
Delay GN => QN	0.29	1.93	0.64	2.28	0.38	1.45	0.68	1.74
Delay SN => Q	0.31	1.96	0.69	2.34	0.20	1.24	0.17	1.22
Delay SN => QN	0.11	1.76	0.09	1.74	0.16	1.22	0.53	1.60
Slew D => Q	0.10	4.24	0.10	4.22	0.07	2.37	0.07	2.38
Slew D => QN	0.11	4.24	0.11	4.22	0.10	2.39	0.10	2.39
Slew GN => Q	0.10	4.24	0.10	4.22	0.07	2.37	0.07	2.37
Slew GN => QN	0.11	4.24	0.11	4.24	0.10	2.39	0.10	2.39
Slew SN => Q	0.13	4.24	0.12	4.24	0.07	2.38	0.07	2.38
Slew SN => QN	0.10	4.24	0.14	4.25	0.09	2.39	0.12	2.39

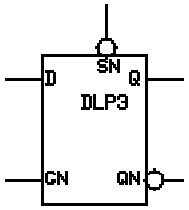
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
D => GN	0.275	0.366	0	0
SN => GN	0	n.a.	0.014	n.a.

	Min Width	
	High	**Low**
GN	n.a.	0.258
SN	n.a.	0.275

DLP3 is a transparent D-latch with an active low asynchronous PRESET and 3x drive strength. The Q output follows the D input when GN is low. The Q output is independent of D when GN is high and retains the value of D just prior to the rising edge on GN.

Truth Table

D	GN	SN	Q	QN
0	0	1	0	1
X	X	0	1	0
1	0	1	1	0



Capacitance

Pin	Cap [pF]
D	0.004
GN	0.007
SN	0.006

Area

0.31 mils^2
200 µm^2

Power

2.9 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay D => Q	0.56	2.10	0.70	2.24	0.50	1.53	0.85	1.88
Delay D => QN	0.35	1.91	0.71	2.26	0.41	1.46	0.54	1.60
Delay GN => Q	0.57	2.11	0.87	2.41	0.46	1.49	0.81	1.84
Delay GN => QN	0.31	1.87	0.66	2.22	0.42	1.48	0.72	1.77
Delay SN => Q	0.41	1.96	0.82	2.35	0.28	1.31	0.31	1.33
Delay SN => QN	0.13	1.69	0.15	1.71	0.20	1.25	0.59	1.65
Slew D => Q	0.10	4.01	0.10	4.01	0.09	2.29	0.09	2.31
Slew D => QN	0.11	4.03	0.11	4.04	0.11	2.32	0.12	2.32
Slew GN => Q	0.10	4.01	0.10	4.01	0.09	2.29	0.09	2.30
Slew GN => QN	0.10	4.03	0.11	4.03	0.11	2.31	0.11	2.30
Slew SN => Q	0.12	4.01	0.12	4.01	0.10	2.32	0.08	2.29
Slew SN => QN	0.09	4.03	0.13	4.02	0.10	2.31	0.14	2.31

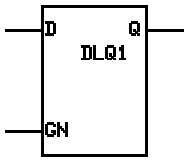
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
D => GN	0.336	0.402	0	0
SN => GN	0	n.a.	0	n.a.

	Min Width	
	High	**Low**
GN	n.a.	0.258
SN	n.a.	0.275

DLQ1 is a transparent D-latch with output Q only and 1x drive strength. The Q output follows the D input when GN is low. The Q output is independent of D when GN is high and retains the value of D just prior to the rising edge on GN.

Truth Table

D	GN	Q
0	0	0
1	0	1



Capacitance

Pin	Cap [pF]
D	0.004
GN	0.007

Area

0.282 mils^2
182 µm^2

Power

0.85 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay D => Q	0.36	2.01	0.48	2.12	0.40	1.44	0.75	1.80
Delay GN => Q	0.37	2.02	0.67	2.32	0.35	1.40	0.71	1.75
Slew D => Q	0.10	4.29	0.10	4.24	0.07	2.38	0.07	2.36
Slew GN => Q	0.10	4.27	0.10	4.27	0.07	2.37	0.07	2.39

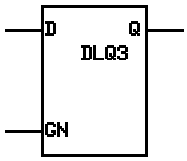
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
D => GN	0.197	0.386	0	0

	Min Width	
	High	**Low**
GN	n.a.	0.258

DLQ3 is a transparent D-latch with output Q only and 3x drive strength. The Q output follows the D input when GN is low. The Q output is independent of D when GN is high and retains the value of D just prior to the rising edge on GN.

Truth Table

D	GN	Q
0	0	0
1	0	1



Capacitance

Pin	Cap [pF]
D	0.004
GN	0.007

Area

0.282 mils^2
182 µm^2

Power

1.37 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay D => Q	0.39	1.96	0.51	2.06	0.44	1.48	0.80	1.83
Delay GN => Q	0.40	1.95	0.70	2.26	0.40	1.43	0.75	1.79
Slew D => Q	0.10	4.02	0.10	4.02	0.09	2.31	0.09	2.30
Slew GN => Q	0.10	4.07	0.10	4.05	0.09	2.31	0.09	2.30

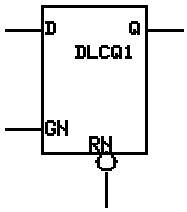
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
D => GN	0.206	0.395	0	0

	Min Width	
	High	**Low**
GN	n.a.	0.258

DLCQ1 is a transparent D-latch with output Q only, an active low asynchronous CLEAR and 1x drive strength. The Q output follows the D input when GN is low. The Q output is independent of D when GN is high and retains the value of D just prior to the rising edge on GN.

Truth Table

D	GN	RN	Q
0	0	1	0
X	X	0	0
1	0	1	1



Capacitance

Pin	Cap [pF]
D	0.004
GN	0.006
RN	0.005

Area

0.282 mils^2
182 µm^2

Power

0.96 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay D => Q	0.35	2.00	0.47	2.11	0.44	1.50	0.79	1.85
Delay GN => Q	0.36	2.01	0.66	2.33	0.40	1.46	0.76	1.82
Delay RN => Q	0.10	1.75	0.05	1.70	0.19	1.26	0.57	1.66
Slew D => Q	0.10	4.30	0.10	4.25	0.08	2.38	0.08	2.38
Slew GN => Q	0.10	4.24	0.10	4.29	0.08	2.37	0.08	2.38
Slew RN => Q	0.10	4.28	0.13	4.23	0.10	2.39	0.14	2.38

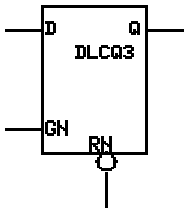
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
D => GN	0.192	0.409	0	0
RN => GN	0	n.a.	0.287	n.a.

	Min Width	
	High	**Low**
GN	n.a.	0.258
RN	n.a.	0.265

DLCQ3 is a transparent D-latch with output Q only, an active low asynchronous CLEAR and 3x drive strength. The Q output follows the D input when GN is low. The Q output is independent of D when GN is high and retains the value of D just prior to the rising edge on GN.

Truth Table

D	GN	RN	Q
0	0	1	0
X	X	0	0
1	0	1	1



Capacitance

Pin	Cap [pF]
D	0.004
GN	0.006
RN	0.005

Area

0.282 mils^2
182 µm^2

Power

1.37 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay D => Q	0.37	1.93	0.49	2.05	0.48	1.53	0.84	1.89
Delay GN => Q	0.39	1.95	0.68	2.25	0.44	1.49	0.80	1.85
Delay RN => Q	0.12	1.68	0.11	1.67	0.23	1.29	0.63	1.69
Slew D => Q	0.09	4.04	0.09	4.08	0.10	2.31	0.09	2.31
Slew GN => Q	0.09	4.06	0.09	4.08	0.10	2.31	0.10	2.30
Slew RN => Q	0.09	4.08	0.13	4.04	0.11	2.31	0.15	2.30

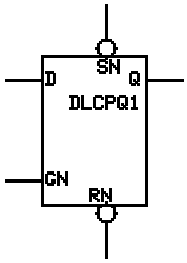
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
D => GN	0.2	0.416	0	0
RN => GN	0	n.a.	0.261	n.a.

	Min Width	
	High	**Low**
GN	n.a.	0.258
RN	n.a.	0.265

DLCPQ1 is a transparent D-latch with output Q only, an active low asynchronous CLEAR and PRESET and 1x drive strength. The Q output follows the D input when GN is low. The Q output is independent of D when GN is high and retains the value of D just prior to the rising edge on GN.

Truth Table

D	GN	RN	SN	Q
0	0	1	1	0
X	X	0	X	0
X	X	1	0	1
1	0	1	1	1



Capacitance

Pin	Cap [pF]
D	0.004
GN	0.006
RN	0.006
SN	0.006

Area

0.31 mils^2
200 µm^2

Power

0.52 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay D => Q	0.41	2.06	0.54	2.19	0.42	1.48	0.77	1.82
Delay GN => Q	0.42	2.07	0.72	2.37	0.38	1.44	0.74	1.79
Delay RN => Q	0.13	1.80	0.16	1.83	0.19	1.29	0.58	1.69
Delay SN => Q	0.24	1.91	0.60	2.26	0.21	1.27	0.17	1.23
Slew D => Q	0.10	4.24	0.10	4.24	0.08	2.38	0.08	2.38
Slew GN => Q	0.11	4.26	0.11	4.26	0.09	2.39	0.08	2.37
Slew RN => Q	0.12	4.31	0.15	4.30	0.11	2.39	0.15	2.38
Slew SN => Q	0.13	4.28	0.12	4.30	0.08	2.39	0.09	2.38

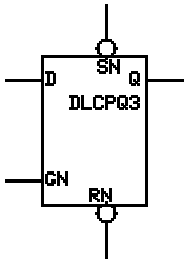
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
D => GN	0.246	0.366	0	0
RN => GN	0	n.a.	0.259	n.a.
SN => GN	0	n.a.	0.013	n.a.

	Min Width	
	High	**Low**
GN	n.a.	0.258
RN	n.a.	0.265
SN	n.a.	0.275

DLCPQ3 is a transparent D-latch with output Q only, an active low asynchronous CLEAR and PRESET and 3x drive strength. The Q output follows the D input when GN is low. The Q output is independent of D when GN is high and retains the value of D just prior to the rising edge on GN.

Truth Table

D	GN	RN	SN	Q
0	0	1	1	0
X	X	0	X	0
X	X	1	0	1
1	0	1	1	1



Capacitance

Pin	Cap [pF]
D	0.004
GN	0.006
RN	0.006
SN	0.006

Area

0.31 mils^2
200 µm^2

Power

1.2 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay D => Q	0.43	1.99	0.57	2.13	0.47	1.51	0.81	1.86
Delay GN => Q	0.45	2.00	0.75	2.31	0.43	1.47	0.78	1.82
Delay RN => Q	0.15	1.73	0.22	1.78	0.24	1.32	0.65	1.74
Delay SN => Q	0.26	1.83	0.62	2.20	0.26	1.30	0.22	1.26
Slew D => Q	0.10	4.08	0.10	4.01	0.10	2.31	0.10	2.31
Slew GN => Q	0.10	4.02	0.09	4.08	0.10	2.30	0.10	2.31
Slew RN => Q	0.12	4.04	0.15	4.09	0.12	2.33	0.16	2.32
Slew SN => Q	0.12	4.07	0.12	4.08	0.10	2.30	0.10	2.29

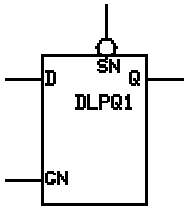
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
D => GN	0.257	0.374	0	0
RN => GN	0	n.a.	0.227	n.a.
SN => GN	0	n.a.	0	n.a.

	Min Width	
	High	**Low**
GN	n.a.	0.258
RN	n.a.	0.265
SN	n.a.	0.275

DLPQ1 is a transparent D-latch with output Q only, an active low asynchronous PRESET and 1x drive strength. The Q output follows the D input when GN is low. The Q output is independent of D when GN is high and retains the value of D just prior to the rising edge on GN.

Truth Table

D	GN	SN	Q
0	0	1	0
X	X	0	1
1	0	1	1



Capacitance

Pin	Cap [pF]
D	0.004
GN	0.007
SN	0.006

Area

0.282 mils^2
182 µm^2

Power

0.88 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay D => Q	0.42	2.06	0.56	2.20	0.38	1.42	0.73	1.77
Delay GN => Q	0.43	2.08	0.73	2.39	0.34	1.39	0.69	1.74
Delay SN => Q	0.26	1.93	0.62	2.29	0.18	1.22	0.11	1.16
Slew D => Q	0.10	4.28	0.10	4.25	0.07	2.38	0.07	2.38
Slew GN => Q	0.10	4.28	0.10	4.29	0.07	2.37	0.07	2.38
Slew SN => Q	0.13	4.29	0.14	4.30	0.08	2.38	0.09	2.38

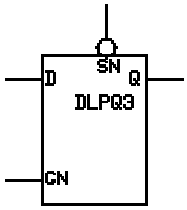
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
D => GN	0.25	0.343	0	0
SN => GN	0	n.a.	0.042	n.a.

	Min Width	
	High	**Low**
GN	n.a.	0.258
SN	n.a.	0.275

DLPQ3 is a transparent D-latch with output Q only, an active low asynchronous PRESET and 3x drive strength. The Q output follows the D input when GN is low. The Q output is independent of D when GN is high and retains the value of D just prior to the rising edge on GN.

Truth Table

D	GN	SN	Q
0	0	1	0
X	X	0	1
1	0	1	1



Capacitance

Pin	Cap [pF]
D	0.004
GN	0.007
SN	0.006

Area

0.282 mils^2
182 µm^2

Power

1.73 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay D => Q	0.45	2.00	0.59	2.15	0.42	1.46	0.77	1.81
Delay GN => Q	0.47	2.02	0.77	2.32	0.39	1.42	0.73	1.77
Delay SN => Q	0.29	1.86	0.66	2.24	0.22	1.26	0.15	1.20
Slew D => Q	0.10	4.04	0.10	4.07	0.09	2.30	0.09	2.31
Slew GN => Q	0.10	4.08	0.10	4.02	0.09	2.31	0.09	2.31
Slew SN => Q	0.13	4.07	0.12	4.06	0.10	2.32	0.09	2.28

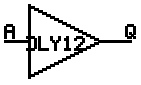
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
D => GN	0.264	0.352	0	0
SN => GN	0	n.a.	0.031	n.a.

	Min Width	
	High	**Low**
GN	n.a.	0.258
SN	n.a.	0.275

DLY12 is a single delay with 2x drive strength.

Truth Table

A	Q
0	0
1	1



Capacitance

Pin	Cap [pF]
A	0.004

Area

0.254 mils^2
164 µm^2

Power

1.74 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**
Delay A => Q	1.53	2.86	1.75	3.08	1.49	2.69	1.88	3.08
Slew A => Q	0.18	3.30	0.17	3.28	0.18	2.42	0.18	2.42

DLY22 is a double delay with 2x drive strength.

Truth Table

A	Q
0	0
1	1

Capacitance

Pin	Cap [pF]
A	0.003

Area

0.339 mils^2
219 µm^2

Power

2.65 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**
Delay A => Q	3.07	4.40	3.29	4.62	3.02	4.23	3.40	4.61
Slew A => Q	0.17	3.26	0.17	3.30	0.19	2.40	0.18	2.42

DLY32 is a triple delay with 2x drive strength.

Truth Table

A	Q
0	0
1	1

Capacitance

Pin	Cap [pF]
A	0.003

Area

0.48 mils^2
310 µm^2

Power

3.45 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**
Delay A => Q	4.63	5.96	4.85	6.17	4.58	5.79	4.97	6.17
Slew A => Q	0.17	3.28	0.17	3.27	0.18	2.42	0.18	2.42

DLY42 is a quadruple delay with 2x drive strength.

Truth Table

A	Q
0	0
1	1

Capacitance

Pin	Cap [pF]
A	0.003

Area

0.621 mils^2
401 µm^2

Power

4.41 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

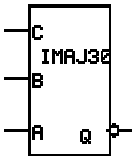
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**
Delay A => Q	6.20	7.52	6.41	7.73	6.14	7.35	6.53	7.73
Slew A => Q	0.17	3.30	0.17	3.30	0.18	2.42	0.18	2.42

IMAJ30 is an inverting majority circuit with 0.5x drive strength providing the logical function Q = NOT (A.B+A.C+B.C)

Truth Table

A	B	C	Q
0	0	X	1
0	X	0	1
X	0	0	1
X	1	1	0
1	X	1	0
1	1	X	0



Capacitance

Pin	Cap [pF]
A	0.011
B	0.010
C	0.004

Area

0.169 mils^2
109 µm^2

Power

0.27 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

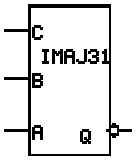
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**
Delay A => Q	0.14	1.76	0.41	1.97	0.08	0.93	0.02	1.02
Delay B => Q	0.14	1.76	0.50	2.09	0.09	0.94	0.13	1.19
Delay C => Q	0.10	1.73	0.42	2.04	0.07	0.91	0.05	1.15
Slew A => Q	0.27	4.32	0.56	4.31	0.15	2.13	0.55	2.21
Slew B => Q	0.27	4.34	0.58	4.34	0.15	2.13	0.52	2.23
Slew C => Q	0.27	4.34	0.57	4.34	0.11	2.09	0.49	2.22

IMAJ31 is an inverting majority circuit with 1x drive strength providing the logical function Q = NOT (A.B+A.C+B.C)

Truth Table

A	B	C	Q
0	0	X	1
0	X	0	1
X	0	0	1
X	1	1	0
1	X	1	0
1	1	X	0



Capacitance

Pin	Cap [pF]
A	0.019
B	0.016
C	0.007

Area

0.169 mils^2
109 µm^2

Power

0.53 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

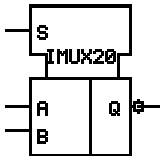
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay A => Q	0.13	1.68	0.38	1.88	0.07	0.90	0.01	0.99
Delay B => Q	0.13	1.68	0.47	2.01	0.08	0.92	0.12	1.16
Delay C => Q	0.09	1.65	0.39	1.97	0.06	0.88	0.04	1.13
Slew A => Q	0.23	4.14	0.52	4.14	0.13	2.06	0.53	2.15
Slew B => Q	0.24	4.17	0.56	4.17	0.14	2.06	0.49	2.16
Slew C => Q	0.24	4.18	0.54	4.17	0.10	2.03	0.45	2.15

IMUX20 is an inverting 2-input to 1-output digital multiplexer with 0.5x drive strength.

Truth Table

A	B	S	Q
0	X	0	1
X	0	1	1
X	1	1	0
1	X	0	0



Capacitance

Pin	Cap [pF]
A	0.005
B	0.005
S	0.008

Area

0.141 mils^2
91 µm^2

Power

0.25 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

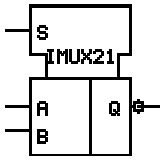
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**
Delay A => Q	0.12	1.74	0.38	1.94	0.07	0.92	-0.00	1.00
Delay B => Q	0.13	1.75	0.38	1.95	0.07	0.91	-0.00	1.00
Delay S => Q	0.19	1.78	0.25	1.82	0.05	0.88	-0.01	1.13
Slew A => Q	0.23	4.28	0.52	4.28	0.12	2.09	0.53	2.17
Slew B => Q	0.23	4.28	0.53	4.28	0.12	2.09	0.52	2.18
Slew S => Q	0.23	4.29	0.23	4.26	0.08	2.08	0.42	2.20

IMUX21 is an inverting 2-input to 1-output digital multiplexer with 1x drive strength.

Truth Table

A	B	S	Q
0	X	0	1
X	0	1	1
X	1	1	0
1	X	0	0



Capacitance

Pin	Cap [pF]
A	0.009
B	0.009
S	0.011

Area

0.141 mils^2
91 µm^2

Power

0.48 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

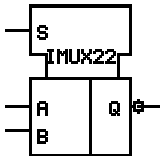
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay A => Q	0.10	1.65	0.35	1.86	0.07	0.90	-0.02	0.98
Delay B => Q	0.11	1.67	0.36	1.87	0.06	0.88	-0.01	0.98
Delay S => Q	0.17	1.70	0.19	1.70	0.04	0.86	-0.03	1.11
Slew A => Q	0.20	4.11	0.51	4.11	0.11	2.04	0.50	2.12
Slew B => Q	0.20	4.12	0.49	4.11	0.10	2.02	0.50	2.12
Slew S => Q	0.20	4.12	0.20	4.11	0.06	2.02	0.40	2.16

IMUX22 is an inverting 2-input to 1-output digital multiplexer with 2x drive strength.

Truth Table

A	B	S	Q
0	X	0	1
X	0	1	1
X	1	1	0
1	X	0	0



Capacitance

Pin	Cap [pF]
A	0.018
B	0.019
S	0.020

Area

0.226 mils^2
146 µm^2

Power

0.93 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

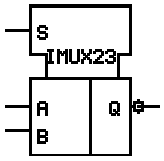
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**
Delay A => Q	0.10	1.65	0.34	1.86	0.06	0.89	-0.03	0.98
Delay B => Q	0.10	1.67	0.35	1.86	0.06	0.88	-0.02	0.97
Delay S => Q	0.16	1.69	0.19	1.70	0.04	0.85	-0.04	1.10
Slew A => Q	0.18	4.10	0.48	4.09	0.10	2.03	0.49	2.12
Slew B => Q	0.18	4.09	0.48	4.10	0.10	2.02	0.50	2.11
Slew S => Q	0.18	4.09	0.18	4.08	0.06	2.02	0.38	2.15

IMUX23 is an inverting 2-input to 1-output digital multiplexer with 3x drive strength.

Truth Table

A	B	S	Q
0	X	0	1
X	0	1	1
X	1	1	0
1	X	0	0



Capacitance

Pin	Cap [pF]
A	0.025
B	0.019
S	0.035

Area

0.226 mils^2
146 µm^2

Power

1.15 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

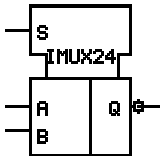
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay A => Q	0.09	1.66	0.38	1.99	0.05	0.88	-0.00	1.13
Delay B => Q	0.11	1.70	0.29	1.88	0.07	0.92	0.12	1.18
Delay S => Q	0.17	1.75	0.27	1.81	0.06	0.90	-0.03	0.97
Slew A => Q	0.18	4.15	0.43	4.13	0.08	2.05	0.46	2.19
Slew B => Q	0.23	4.21	0.57	4.21	0.13	2.11	0.61	2.23
Slew S => Q	0.19	4.17	0.22	4.15	0.10	2.11	0.49	2.18

IMUX24 is an inverting 2-input to 1-output digital multiplexer with 4x drive strength.

Truth Table

A	B	S	Q
0	X	0	1
X	0	1	1
X	1	1	0
1	X	0	0



Capacitance

Pin	Cap [pF]
A	0.030
B	0.022
S	0.045

Area

0.282 mils^2
182 µm^2

Power

1.71 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

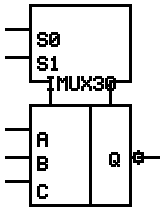
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.004**	**1.28**	**0.004**	**1.28**	**0.004**	**1.28**	**0.004**	**1.28**
Delay A => Q	0.08	1.69	0.38	2.01	0.05	0.88	0.01	1.13
Delay B => Q	0.08	1.69	0.38	2.01	0.05	0.88	0.01	1.13
Delay S => Q	0.18	1.78	0.28	1.84	0.06	0.88	-0.04	0.95
Slew A => Q	0.20	4.23	0.51	4.26	0.08	2.02	0.45	2.15
Slew B => Q	0.20	4.23	0.50	4.24	0.08	2.02	0.45	2.15
Slew S => Q	0.18	4.21	0.22	4.20	0.08	2.01	0.48	2.09

IMUX30 is an inverting 3-input to 1-output digital multiplexer with 0.5x drive strength.

Truth Table

A	B	C	S0	S1	Q
0	X	X	0	0	1
X	0	X	1	0	1
X	X	0	X	1	1
X	X	1	X	1	0
X	1	X	1	0	0
1	X	X	0	0	0



Capacitance

Pin	Cap [pF]
A	0.007
B	0.007
C	0.005
S0	0.009
S1	0.007

Area

0.282 mils^2
182 µm^2

Power

0.46 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

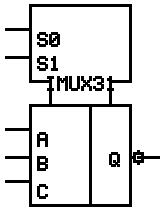
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**
Delay A => Q	0.20	1.35	0.48	1.60	0.14	0.83	0.11	0.92
Delay B => Q	0.21	1.35	0.49	1.60	0.13	0.82	0.11	0.92
Delay C => Q	0.13	1.75	0.38	1.96	0.07	0.92	0.00	1.00
Delay S0 => Q	0.32	1.45	0.44	1.56	0.11	0.79	0.14	1.01
Delay S1 => Q	0.24	1.83	0.30	1.87	0.05	0.87	-0.02	1.12
Slew A => Q	0.49	4.18	0.76	4.20	0.21	1.93	0.59	2.00
Slew B => Q	0.49	4.18	0.76	4.20	0.20	1.93	0.59	1.99
Slew C => Q	0.23	4.31	0.52	4.30	0.13	2.10	0.53	2.18
Slew S0 => Q	0.50	4.18	0.50	4.17	0.17	1.92	0.55	2.03
Slew S1 => Q	0.26	4.30	0.25	4.27	0.08	2.09	0.43	2.22

IMUX31 is an inverting 3-input to 1-output digital multiplexer with 1x drive strength.

Truth Table

A	B	C	S0	S1	Q
0	X	X	0	0	1
X	0	X	1	0	1
X	X	0	X	1	1
X	X	1	X	1	0
X	1	X	1	0	0
1	X	X	0	0	0



Capacitance

Pin	Cap [pF]
A	0.014
B	0.015
C	0.009
S0	0.016
S1	0.011

Area

0.339 mils^2
219 µm^2

Power

0.87 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

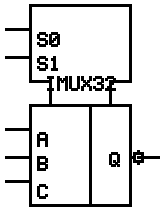
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay A => Q	0.19	1.33	0.46	1.59	0.13	0.82	0.09	0.91
Delay B => Q	0.20	1.34	0.47	1.59	0.12	0.81	0.09	0.91
Delay C => Q	0.12	1.67	0.36	1.87	0.06	0.88	-0.01	0.98
Delay S0 => Q	0.28	1.42	0.38	1.50	0.10	0.78	0.12	1.00
Delay S1 => Q	0.24	1.77	0.34	1.85	0.04	0.84	-0.04	1.10
Slew A => Q	0.45	4.10	0.72	4.11	0.19	1.90	0.59	1.97
Slew B => Q	0.45	4.11	0.72	4.12	0.18	1.90	0.58	1.97
Slew C => Q	0.21	4.13	0.50	4.14	0.10	2.03	0.52	2.11
Slew S0 => Q	0.45	4.11	0.46	4.09	0.15	1.90	0.53	2.01
Slew S1 => Q	0.21	4.12	0.21	4.11	0.06	2.03	0.39	2.17

IMUX32 is an inverting 3-input to 1-output digital multiplexer with 2x drive strength.

Truth Table

A	B	C	S0	S1	Q
0	X	X	0	0	1
X	0	X	1	0	1
X	X	0	X	1	1
X	X	1	X	1	0
X	1	X	1	0	0
1	X	X	0	0	0



Capacitance

Pin	Cap [pF]
A	0.025
B	0.019
C	0.012
S0	0.034
S1	0.022

Area

0.367 mils^2
237 µm^2

Power

1.52 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

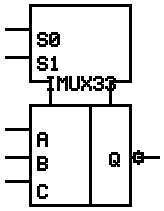
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**
Delay A => Q	0.18	1.31	0.52	1.68	0.12	0.81	0.16	1.03
Delay B => Q	0.20	1.35	0.42	1.57	0.15	0.87	0.26	1.12
Delay C => Q	0.07	1.63	0.37	1.97	0.05	0.81	-0.03	1.05
Delay S0 => Q	0.26	1.40	0.36	1.49	0.14	0.85	0.12	0.95
Delay S1 => Q	0.21	1.77	0.33	1.85	0.05	0.80	-0.10	0.90
Slew A => Q	0.48	4.20	0.75	4.22	0.18	1.94	0.60	2.03
Slew B => Q	0.54	4.28	0.86	4.30	0.23	2.01	0.69	2.09
Slew C => Q	0.15	4.08	0.41	4.11	0.06	1.89	0.38	2.03
Slew S0 => Q	0.49	4.24	0.52	4.23	0.21	2.01	0.61	2.08
Slew S1 => Q	0.19	4.11	0.22	4.11	0.08	1.88	0.47	1.97

IMUX33 is an inverting 3-input to 1-output digital multiplexer with 3x drive strength.

Truth Table

A	B	C	S0	S1	Q
0	X	X	0	0	1
X	0	X	1	0	1
X	X	0	X	1	1
X	X	1	X	1	0
X	1	X	1	0	0
1	X	X	0	0	0



Capacitance

Pin	Cap [pF]
A	0.037
B	0.037
C	0.026
S0	0.037
S1	0.028

Area

0.564 mils^2
364 µm^2

Power

2.41 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

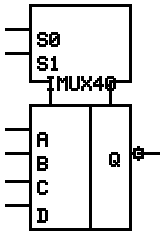
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay A => Q	0.18	1.36	0.45	1.61	0.12	0.79	0.06	0.87
Delay B => Q	0.19	1.38	0.46	1.61	0.11	0.77	0.06	0.87
Delay C => Q	0.11	1.65	0.34	1.84	0.06	0.89	-0.02	0.98
Delay S0 => Q	0.25	1.43	0.33	1.50	0.09	0.75	0.07	0.96
Delay S1 => Q	0.20	1.72	0.31	1.81	0.04	0.84	-0.06	1.09
Slew A => Q	0.42	4.18	0.69	4.20	0.17	1.84	0.57	1.92
Slew B => Q	0.42	4.19	0.69	4.20	0.16	1.83	0.58	1.91
Slew C => Q	0.18	4.08	0.48	4.06	0.10	2.03	0.52	2.11
Slew S0 => Q	0.42	4.19	0.42	4.18	0.14	1.83	0.52	1.95
Slew S1 => Q	0.18	4.07	0.19	4.05	0.05	2.02	0.39	2.17

IMUX40 is an inverting 4-input to 1-output digital multiplexer with 0.5x drive strength.

Truth Table

A	B	C	D	S0	S1	Q
0	X	X	X	0	0	1
X	0	X	X	1	0	1
X	X	0	X	0	1	1
X	X	X	0	1	1	1
X	X	X	1	1	1	0
X	X	1	X	0	1	0
X	1	X	X	1	0	0
1	X	X	X	0	0	0



Capacitance

Pin	Cap [pF]
A	0.007
B	0.007
C	0.007
D	0.007
S0	0.018
S1	0.007

Area

0.339 mils^2
219 µm^2

Power

0.44 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

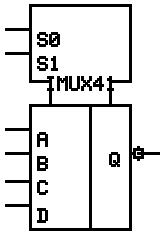
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**
Delay A => Q	0.20	1.35	0.48	1.60	0.13	0.82	0.11	0.92
Delay B => Q	0.21	1.37	0.49	1.61	0.13	0.81	0.11	0.93
Delay C => Q	0.21	1.36	0.49	1.62	0.13	0.82	0.11	0.91
Delay D => Q	0.21	1.36	0.49	1.61	0.13	0.81	0.12	0.91
Delay S0 => Q	0.31	1.45	0.42	1.55	0.11	0.79	0.13	1.01
Delay S1 => Q	0.10	1.15	0.29	1.23	0.03	0.70	-0.08	0.89
Slew A => Q	0.48	4.17	0.75	4.19	0.20	1.91	0.59	1.99
Slew B => Q	0.48	4.18	0.75	4.19	0.20	1.91	0.60	1.98
Slew C => Q	0.49	4.21	0.76	4.22	0.21	1.92	0.60	1.99
Slew D => Q	0.49	4.21	0.76	4.22	0.20	1.91	0.59	1.97
Slew S0 => Q	0.51	4.21	0.49	4.20	0.17	1.92	0.55	2.02
Slew S1 => Q	0.43	4.21	0.37	4.17	0.08	1.91	0.47	2.06

IMUX41 is an inverting 4-input to 1-output digital multiplexer with 1x drive strength.

Truth Table

A	B	C	D	S0	S1	Q
0	X	X	X	0	0	1
X	0	X	X	1	0	1
X	X	0	X	0	1	1
X	X	X	0	1	1	1
X	X	X	1	1	1	0
X	X	1	X	0	1	0
X	1	X	X	1	0	0
1	X	X	X	0	0	0



Capacitance

Pin	Cap [pF]
A	0.013
B	0.013
C	0.013
D	0.013
S0	0.031
S1	0.012

Area

0.395 mils^2
255 µm^2

Power

0.86 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

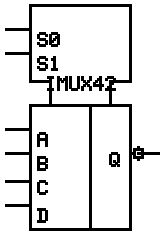
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay A => Q	0.19	1.31	0.46	1.55	0.13	0.83	0.10	0.91
Delay B => Q	0.20	1.33	0.46	1.55	0.12	0.80	0.11	0.91
Delay C => Q	0.19	1.32	0.47	1.56	0.13	0.81	0.10	0.92
Delay D => Q	0.20	1.36	0.47	1.61	0.12	0.79	0.10	0.89
Delay S0 => Q	0.28	1.42	0.36	1.50	0.10	0.78	0.12	1.00
Delay S1 => Q	0.10	1.17	0.25	1.21	0.03	0.69	-0.08	0.87
Slew A => Q	0.44	4.05	0.72	4.07	0.19	1.89	0.59	1.97
Slew B => Q	0.44	4.06	0.73	4.08	0.19	1.89	0.59	1.97
Slew C => Q	0.44	4.06	0.71	4.08	0.18	1.88	0.61	1.96
Slew D => Q	0.45	4.19	0.72	4.20	0.18	1.88	0.60	1.94
Slew S0 => Q	0.46	4.18	0.45	4.17	0.16	1.89	0.54	1.99
Slew S1 => Q	0.38	4.19	0.34	4.14	0.07	1.88	0.42	2.03

IMUX42 is an inverting 4-input to 1-output digital multiplexer with 2x drive strength.

Truth Table

A	B	C	D	S0	S1	Q
0	X	X	X	0	0	1
X	0	X	X	1	0	1
X	X	0	X	0	1	1
X	X	X	0	1	1	1
X	X	X	1	1	1	0
X	X	1	X	0	1	0
X	1	X	X	1	0	0
1	X	X	X	0	0	0



Capacitance

Pin	Cap [pF]
A	0.024
B	0.017
C	0.024
D	0.017
S0	0.071
S1	0.021

Area

0.564 mils^2
364 µm^2

Power

1.56 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**
Delay A => Q	0.17	1.37	0.52	1.72	0.11	0.81	0.14	1.03
Delay B => Q	0.16	1.36	0.51	1.71	0.11	0.77	0.12	0.99
Delay C => Q	0.17	1.31	0.50	1.67	0.11	0.84	0.17	1.07
Delay D => Q	0.17	1.33	0.51	1.71	0.10	0.76	0.12	0.98
Delay S0 => Q	0.27	1.44	0.37	1.53	0.11	0.77	0.05	0.86
Delay S1 => Q	0.09	1.18	0.22	1.22	0.03	0.74	-0.08	0.90
Slew A => Q	0.46	4.23	0.74	4.24	0.16	1.94	0.57	2.05
Slew B => Q	0.45	4.21	0.73	4.22	0.16	1.85	0.55	1.97
Slew C => Q	0.44	4.17	0.74	4.18	0.19	2.00	0.58	2.09
Slew D => Q	0.45	4.26	0.73	4.26	0.16	1.81	0.56	1.92
Slew S0 => Q	0.42	4.21	0.45	4.21	0.16	1.86	0.56	1.93
Slew S1 => Q	0.35	4.26	0.32	4.22	0.07	1.99	0.39	2.15

INV0 is an inverter with 0.5x drive strength.

Truth Table

A	Q
0	1
1	0

Capacitance

Pin	Cap [pF]
A	0.004

Area

0.056 mils^2
36 µm^2

Power

0.17 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

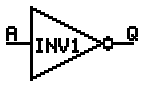
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**
Delay A => Q	0.06	1.89	0.35	2.27	0.04	1.12	-0.01	1.40
Slew A => Q	0.13	4.66	0.40	4.70	0.07	2.51	0.40	2.59

INV1 is an inverter with 1x drive strength.

Truth Table

A	Q
0	1
1	0



Capacitance

Pin	Cap [pF]
A	0.006

Area

0.056 mils^2
36 µm^2

Power

0.34 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

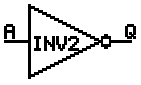
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay A => Q	0.05	1.72	0.29	2.06	0.03	1.06	-0.03	1.34
Slew A => Q	0.09	4.30	0.35	4.25	0.05	2.40	0.35	2.48

INV2 is an inverter with 2x drive strength.

Truth Table

A	Q
0	1
1	0



Capacitance

Pin	Cap [pF]
A	0.009

Area

0.056 mils^2
36 µm^2

Power

0.65 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

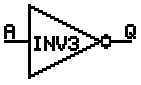
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**
Delay A => Q	0.04	1.62	0.27	1.99	0.03	1.04	-0.04	1.31
Slew A => Q	0.07	4.10	0.33	4.10	0.04	2.33	0.34	2.41

INV3 is an inverter with 3x drive strength.

Truth Table

A	Q
0	1
1	0



Capacitance

Pin	Cap [pF]
A	0.013

Area

0.056 mils^2
36 µm^2

Power

0.96 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

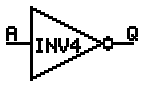
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay A => Q	0.04	1.60	0.25	1.97	0.03	1.03	-0.05	1.30
Slew A => Q	0.06	4.05	0.31	4.06	0.03	2.31	0.33	2.39

INV4 is an inverter with 4x drive strength.

Truth Table

A	Q
0	1
1	0



Capacitance

Pin	Cap [pF]
A	0.018

Area

0.085 mils^2
55 µm^2

Power

1.24 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

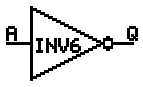
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.004**	**1.28**	**0.004**	**1.28**	**0.004**	**1.28**	**0.004**	**1.28**
Delay A => Q	0.03	1.61	0.24	1.99	0.02	1.03	-0.06	1.31
Slew A => Q	0.05	4.07	0.29	4.09	0.03	2.31	0.30	2.40

INV6 is an inverter with 6x drive strength.

Truth Table

A	Q
0	1
1	0



Capacitance

Pin	Cap [pF]
A	0.025

Area

0.085 mils^2
55 µm^2

Power

1.84 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

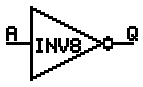
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.006**	**1.92**	**0.006**	**1.92**	**0.006**	**1.92**	**0.006**	**1.92**
Delay A => Q	0.03	1.58	0.23	1.95	0.02	1.02	-0.07	1.30
Slew A => Q	0.05	4.01	0.28	4.06	0.03	2.29	0.29	2.38

INV8 is an inverter with 8x drive strength.

Truth Table

A	Q
0	1
1	0



Capacitance

Pin	Cap [pF]
A	0.034

Area

0.113 mils^2
73 µm^2

Power

2.52 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

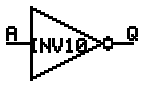
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.008**	**2.56**	**0.008**	**2.56**	**0.008**	**2.56**	**0.008**	**2.56**
Delay A => Q	0.03	1.58	0.24	1.95	0.03	1.02	-0.05	1.30
Slew A => Q	0.06	4.02	0.30	4.05	0.03	2.28	0.32	2.38

INV10 is an inverter with 10x drive strength.

Truth Table

A	Q
0	1
1	0



Capacitance

Pin	Cap [pF]
A	0.043

Area

0.141 mils^2
91 µm^2

Power

3.09 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

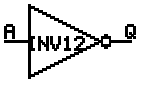
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.01**	**3.2**	**0.01**	**3.2**	**0.01**	**3.2**	**0.01**	**3.2**
Delay A => Q	0.03	1.59	0.24	1.97	0.02	1.02	-0.07	1.30
Slew A => Q	0.05	4.05	0.29	4.07	0.03	2.28	0.30	2.39

INV12 is an inverter with 12x drive strength.

Truth Table

A	Q
0	1
1	0



Capacitance

Pin	Cap [pF]
A	0.051

Area

0.141 mils^2
91 µm^2

Power

3.71 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.012**	**3.84**	**0.012**	**3.84**	**0.012**	**3.84**	**0.012**	**3.84**
Delay A => Q	0.03	1.59	0.23	1.96	0.02	1.02	-0.07	1.30
Slew A => Q	0.05	4.04	0.28	4.06	0.03	2.29	0.30	2.38

INV15 is an inverter with 15x drive strength.

Truth Table

A	Q
0	1
1	0

Capacitance

Pin	Cap [pF]
A	0.064

Area

0.169 mils^2
109 µm^2

Power

4.67 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

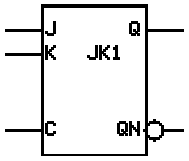
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.015**	**4.8**	**0.015**	**4.8**	**0.015**	**4.8**	**0.015**	**4.8**
Delay A => Q	0.03	1.59	0.24	1.96	0.02	1.02	-0.06	1.30
Slew A => Q	0.05	4.04	0.29	4.06	0.03	2.29	0.30	2.38

JK1 is a JK flip-flop with 1x drive strength. Output changes states on the 0-1 transition of C.

Truth Table

C	J	K	Q	QN
↑	0	1	0	1
↑	1	0	1	0
↑	1	1	~Q	~QN



Capacitance

Pin	Cap [pF]
C	0.004
J	0.005
K	0.005

Area

0.536 mils^2
346 µm^2

Power

1.28 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay C => Q	0.51	2.17	0.69	2.34	0.56	1.64	0.72	1.80
Delay C => QN	0.70	2.34	0.86	2.50	0.62	1.68	0.80	1.86
Slew C => Q	0.12	4.24	0.12	4.25	0.10	2.39	0.11	2.39
Slew C => QN	0.12	4.24	0.11	4.23	0.09	2.38	0.09	2.38

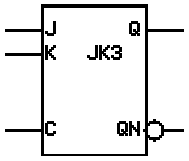
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
J => C	0	0.227	0	0
K => C	0.188	0.301	0	0

	Min Width	
	High	**Low**
C	0.376	0.326

JK3 is a JK flip-flop with 3x drive strength. Output changes states on the 0-1 transition of C.

Truth Table

C	J	K	Q	QN
↑	0	1	0	1
↑	1	0	1	0
↑	1	1	~Q	~QN



Capacitance

Pin	Cap [pF]
C	0.004
J	0.005
K	0.005

Area

0.536 mils^2
346 µm^2

Power

1.88 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay C => Q	0.54	2.10	0.71	2.27	0.59	1.66	0.75	1.82
Delay C => QN	0.79	2.33	0.95	2.48	0.71	1.76	0.88	1.93
Slew C => Q	0.11	4.03	0.11	4.03	0.10	2.31	0.10	2.31
Slew C => QN	0.11	4.02	0.10	4.02	0.10	2.31	0.10	2.31

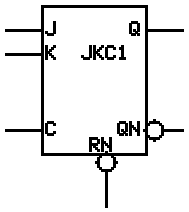
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
J => C	0.199	0.227	0	0
K => C	0.188	0.301	0	0

	Min Width	
	High	**Low**
C	0.376	0.326

JKC1 is a JK flip-flop with asynchronous acitve low CLEAR and 1x drive strength. Output changes states on the 0-1 transition of C.

Truth Table

C	J	K	RN	Q	QN
↑	0	1	1	0	1
↑	1	0	1	1	0
↑	1	1	1	~Q	~QN
X	X	X	0	0	1



Capacitance

Pin	Cap [pF]
C	0.004
J	0.005
K	0.005
RN	0.011

Area

0.564 mils^2
364 µm^2

Power

1.4 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay C => Q	0.49	2.14	0.67	2.32	0.61	1.70	0.77	1.85
Delay C => QN	0.75	2.39	0.91	2.55	0.59	1.66	0.77	1.83
Delay RN => Q	n.a.	n.a.	n.a.	n.a.	0.20	1.27	0.58	1.67
Delay RN => QN	0.38	2.04	0.79	2.43	n.a.	n.a.	n.a.	n.a.
Slew C => Q	0.12	4.25	0.11	4.25	0.11	2.38	0.11	2.38
Slew C => QN	0.11	4.23	0.11	4.24	0.09	2.39	0.09	2.38
Slew RN => Q	n.a.	n.a.	n.a.	n.a.	0.11	2.39	0.15	2.38
Slew RN => QN	0.13	4.25	0.14	4.24	n.a.	n.a.	n.a.	n.a.

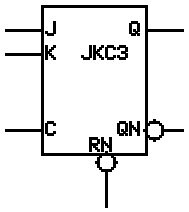
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
J => C	0.202	0.248	0	0
K => C	0.21	0.299	0	0
RN => C	0	n.a.	0.466	n.a.

	Min Width	
	High	**Low**
C	0.376	0.326
RN	n.a.	0.360

JKC3 is a JK flip-flop with asynchronous active low CLEAR and 3x drive strength. Output changes states on the 0-1 transition of C.

Truth Table

C	J	K	RN	Q	QN
↑	0	1	1	0	1
↑	1	0	1	1	0
↑	1	1	1	~Q	~QN
X	X	X	0	0	1



Capacitance

Pin	Cap [pF]
C	0.004
J	0.005
K	0.005
RN	0.011

Area

0.564 mils^2
364 µm^2

Power

2.22 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay C => Q	0.50	2.07	0.68	2.24	0.64	1.72	0.80	1.89
Delay C => QN	0.85	2.38	1.01	2.54	0.67	1.72	0.85	1.89
Delay RN => Q	n.a.	n.a.	n.a.	n.a.	0.23	1.29	0.63	1.71
Delay RN => QN	0.48	2.03	0.90	2.44	n.a.	n.a.	n.a.	n.a.
Slew C => Q	0.10	4.02	0.10	4.03	0.12	2.31	0.11	2.31
Slew C => QN	0.11	4.01	0.10	4.02	0.10	2.31	0.10	2.31
Slew RN => Q	n.a.	n.a.	n.a.	n.a.	0.11	2.31	0.15	2.31
Slew RN => QN	0.13	4.02	0.13	4.02	n.a.	n.a.	n.a.	n.a.

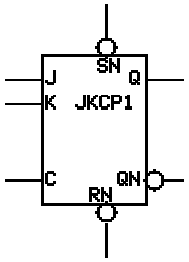
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
J => C	0.202	0.248	0	0
K => C	0.21	0.299	0	0
RN => C	0	n.a.	0.466	n.a.

	Min Width	
	High	**Low**
C	0.376	0.326
RN	n.a.	0.360

JKCP1 is a JK flip-flop with asynchronous active low CLEAR and PRESET and 1x drive strength. Output changes states on the 0-1 transition of C.

Truth Table

C	J	K	RN	SN	Q	QN
↑	0	1	1	1	0	1
↑	1	0	1	1	1	0
↑	1	1	1	1	~Q	~QN
X	X	X	0	0	0	0
X	X	X	0	1	0	1
X	X	X	1	0	1	0



Capacitance

Pin	Cap [pF]
C	0.004
J	0.005
K	0.005
RN	0.015
SN	0.013

Area

0.592 mils^2
382 µm^2

Power

1.6 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay C => Q	0.50	2.16	0.73	2.37	0.60	1.73	0.81	1.92
Delay C => QN	0.70	2.35	0.91	2.54	0.67	1.73	0.83	1.94
Delay RN => Q	0.14	1.82	0.20	1.82	0.20	1.30	0.64	1.74
Delay RN => QN	0.34	1.99	0.73	2.38	n.a.	n.a.	n.a.	n.a.
Delay SN => Q	0.40	2.05	0.83	2.47	n.a.	n.a.	n.a.	n.a.
Delay SN => QN	0.17	1.83	0.23	1.91	0.21	1.35	0.64	1.79
Slew C => Q	0.12	4.25	0.12	4.24	0.12	2.39	0.12	2.39
Slew C => QN	0.11	4.24	0.11	4.24	0.10	2.38	0.10	2.38
Slew RN => Q	0.12	4.30	0.15	4.29	0.10	2.42	0.15	2.40
Slew RN => QN	0.17	4.29	0.17	4.28	n.a.	n.a.	n.a.	n.a.
Slew SN => Q	0.17	4.31	0.17	4.32	n.a.	n.a.	n.a.	n.a.
Slew SN => QN	0.13	4.29	0.16	4.30	0.17	2.42	0.17	2.40

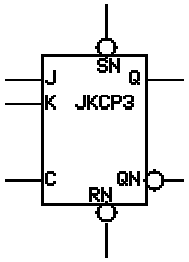
	Setup		Hold	
	rise	fall	rise	fall
J => C	0	0.219	0	0
K => C	0.168	0.338	0	0
RN => C	0	n.a.	0.457	n.a.
SN => C	0	n.a.	0.292	n.a.

	Min Width	
	High	Low
C	0.376	0.326
RN	n.a.	0.360
SN	n.a.	0.380

JKCP3 is a JK flip-flop with asynchronous active low CLEAR and PRESET and 3x drive strength. Output changes states on the 0-1 transition of C.

Truth Table

C	J	K	RN	SN	Q	QN
↑	0	1	1	1	0	1
↑	1	0	1	1	1	0
↑	1	1	1	1	~Q	~QN
X	X	X	0	0	0	0
X	X	X	0	1	0	1
X	X	X	1	0	1	0



Capacitance

Pin	Cap [pF]
C	0.004
J	0.005
K	0.005
RN	0.015
SN	0.013

Area

0.592 mils^2
382 µm^2

Power

2.12 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay C => Q	0.50	2.10	0.73	2.28	0.69	1.76	0.81	1.93
Delay C => QN	0.80	2.37	0.99	2.51	0.70	1.78	0.93	1.98
Delay RN => Q	0.19	1.74	0.20	1.78	0.23	1.33	0.64	1.73
Delay RN => QN	0.41	1.97	0.82	2.37	n.a.	n.a.	n.a.	n.a.
Delay SN => Q	0.49	2.02	0.91	2.45	n.a.	n.a.	n.a.	n.a.
Delay SN => QN	0.19	1.76	0.26	1.83	0.29	1.39	0.71	1.79
Slew C => Q	0.11	4.03	0.11	4.04	0.12	2.31	0.12	2.31
Slew C => QN	0.10	4.02	0.10	4.02	0.12	2.30	0.12	2.31
Slew RN => Q	0.10	4.08	0.15	4.08	0.17	2.31	0.17	2.32
Slew RN => QN	0.12	4.03	0.14	4.01	n.a.	n.a.	n.a.	n.a.
Slew SN => Q	0.12	4.02	0.12	4.07	n.a.	n.a.	n.a.	n.a.
Slew SN => QN	0.12	4.08	0.16	4.07	0.13	2.39	0.17	2.32

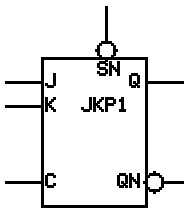
	Setup		Hold	
	rise	fall	rise	fall
J => C	0	0.219	0	0
K => C	0.168	0.338	0	0
RN => C	0	n.a.	0.457	n.a.
SN => C	0	n.a.	0.292	n.a.

	Min Width	
	High	Low
C	0.376	0.326
RN	n.a.	0.360
SN	n.a.	0.380

JKP1 is a JK flip-flop with asynchronous active low PRESET and 1x drive strength. Output changes states on the 0-1 transition of C.

Truth Table

C	J	K	SN	Q	QN
↑	0	1	1	0	1
↑	1	0	1	1	0
↑	1	1	1	~Q	~QN
X	X	X	0	1	0



Capacitance

Pin	Cap [pF]
C	0.004
J	0.005
K	0.005
SN	0.010

Area

0.564 mils^2
364 µm^2

Power

1.37 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay C => Q	0.53	2.18	0.71	2.36	0.57	1.66	0.73	1.81
Delay C => QN	0.67	2.31	0.83	2.47	0.68	1.74	0.85	1.92
Delay SN => Q	0.45	2.09	0.86	2.50	n.a.	n.a.	n.a.	n.a.
Delay SN => QN	n.a.	n.a.	n.a.	n.a.	0.22	1.31	0.62	1.72
Slew C => Q	0.13	4.25	0.12	4.24	0.10	2.38	0.10	2.39
Slew C => QN	0.11	4.24	0.11	4.22	0.10	2.38	0.10	2.39
Slew SN => Q	0.13	4.25	0.14	4.25	n.a.	n.a.	n.a.	n.a.
Slew SN => QN	n.a.	n.a.	n.a.	n.a.	0.11	2.39	0.15	2.39

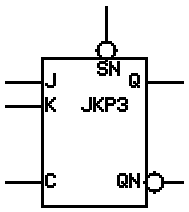
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
J => C	0	0.202	0	0
K => C	0.153	0.34	0	0
SN => C	0	n.a.	0.328	n.a.

	Min Width	
	High	**Low**
C	0.376	0.326
SN	n.a.	0.380

JKP3 is a JK flip-flop with asynchronous active low PRESET and 3x drive strength. Output changes states on the 0-1 transition of C.

Truth Table

C	J	K	SN	Q	QN
↑	0	1	1	0	1
↑	1	0	1	1	0
↑	1	1	1	~Q	~QN
X	X	X	0	1	0



Capacitance

Pin	Cap [pF]
C	0.004
J	0.005
K	0.005
SN	0.010

Area

0.564 mils^2
364 µm^2

Power

2.01 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay C => Q	0.55	2.11	0.73	2.30	0.61	1.68	0.76	1.84
Delay C => QN	0.74	2.28	0.90	2.44	0.76	1.81	0.94	1.99
Delay SN => Q	0.54	2.08	0.96	2.50	n.a.	n.a.	n.a.	n.a.
Delay SN => QN	n.a.	n.a.	n.a.	n.a.	0.26	1.34	0.67	1.76
Slew C => Q	0.11	4.03	0.11	4.03	0.11	2.31	0.11	2.31
Slew C => QN	0.10	4.02	0.10	4.01	0.11	2.31	0.11	2.31
Slew SN => Q	0.12	4.02	0.12	4.03	n.a.	n.a.	n.a.	n.a.
Slew SN => QN	n.a.	n.a.	n.a.	n.a.	0.13	2.31	0.17	2.31

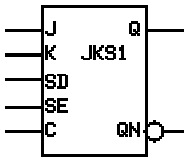
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
J => C	0.26	0.202	0	0
K => C	0.153	0.34	0	0
SN => C	0	n.a.	0.328	n.a.

	Min Width	
	High	**Low**
C	0.376	0.326
SN	n.a.	0.380

JKS1 is a Scan JK flip-flop with 1x drive strength. SCAN ENABLE switches between normal DATA and SCAN DATA input.

Truth Table

C	J	K	SD	SE	Q	QN
↑	0	1	X	0	0	1
↑	X	X	0	1	0	1
↑	X	X	1	1	1	0
↑	1	0	X	0	1	0
↑	1	1	X	0	~Q	~QN



Capacitance

Pin	Cap [pF]
C	0.004
J	0.005
K	0.005
SD	0.010
SE	0.006

Area

0.677 mils^2
437 µm^2

Power

1.51 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay C => Q	0.60	2.19	0.70	2.40	0.61	1.73	0.84	1.93
Delay C => QN	0.74	2.40	0.94	2.64	0.70	1.75	0.88	1.92
Slew C => Q	0.12	4.25	0.12	4.25	0.11	2.39	0.11	2.39
Slew C => QN	0.11	4.24	0.11	4.25	0.10	2.40	0.10	2.39

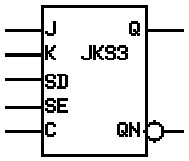
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
J => C	0.321	0.381	0	0
K => C	0.311	0.439	0	0
SD => C	0.041	0	0	0
SE => C	0.143	0.403	0	0

	Min Width	
	High	**Low**
C	0.376	0.326

JKS3 is a Scan JK flip-flop with 3x drive strength. SCAN ENABLE switches between normal DATA and SCAN DATA input.

Truth Table

C	J	K	SD	SE	Q	QN
↑	0	1	X	0	0	1
↑	X	X	0	1	0	1
↑	X	X	1	1	1	0
↑	1	0	X	0	1	0
↑	1	1	X	0	~Q	~QN



Capacitance

Pin	Cap [pF]
C	0.004
J	0.005
K	0.005
SD	0.010
SE	0.006

Area

0.677 mils^2
437 µm^2

Power

2 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay C => Q	0.60	2.17	0.78	2.32	0.66	1.76	0.84	1.95
Delay C => QN	0.83	2.41	1.04	2.61	0.80	1.82	0.93	1.99
Slew C => Q	0.10	4.04	0.11	4.02	0.11	2.31	0.11	2.31
Slew C => QN	0.12	4.03	0.11	4.01	0.11	2.32	0.10	2.32

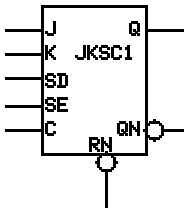
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
J => C	0	0.382	0	0
K => C	0	0.439	0	0
SD => C	0	0.002	0	0
SE => C	0.144	0.403	0	0

	Min Width	
	High	**Low**
C	0.376	0.326

JKSC1 is a Scan JK flip-flop with asynchronous active low CLEAR and 1x drive strength. SCAN ENABLE switches between normal DATA and SCAN DATA input.

Truth Table

C	J	K	RN	SD	SE	Q	QN
↑	0	1	1	X	0	0	1
↑	X	X	1	0	1	0	1
↑	X	X	1	1	1	1	0
↑	1	0	1	X	0	1	0
↑	1	1	1	X	0	~Q	~QN
X	X	X	0	X	X	0	1



Capacitance

Pin	Cap [pF]
C	0.004
J	0.005
K	0.005
RN	0.011
SD	0.010
SE	0.006

Area

0.705 mils^2
455 µm^2

Power

1.57 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay C => Q	0.50	2.20	0.65	2.33	0.70	1.78	0.89	2.00
Delay C => QN	0.80	2.48	1.04	2.67	0.62	1.73	0.75	1.86
Delay RN => Q	n.a.	n.a.	n.a.	n.a.	0.20	1.31	0.65	1.73
Delay RN => QN	0.40	2.06	0.82	2.46	n.a.	n.a.	n.a.	n.a.
Slew C => Q	0.17	4.25	0.13	4.32	0.17	2.44	0.17	2.42
Slew C => QN	0.11	4.27	0.17	4.24	0.17	2.39	0.17	2.40
Slew RN => Q	n.a.	n.a.	n.a.	n.a.	0.11	2.48	0.17	2.48
Slew RN => QN	0.17	4.33	0.17	4.32	n.a.	n.a.	n.a.	n.a.

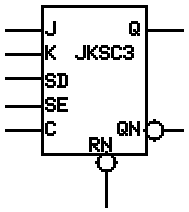
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
J => C	0.192	0.408	0	0
K => C	0	0.437	0	0
RN => C	0	n.a.	0.496	n.a.
SD => C	0	0.002	0	0
SE => C	0.16	0.398	0	0

	Min Width	
	High	**Low**
C	0.376	0.326
RN	n.a.	0.360

JKSC3 is a Scan JK flip-flop with asynchronous active low CLEAR and 3x drive strength. SCAN ENABLE switches between normal DATA and SCAN DATA input.

Truth Table

C	J	K	RN	SD	SE	Q	QN
↑	0	1	1	X	0	0	1
↑	X	X	1	0	1	0	1
↑	X	X	1	1	1	1	0
↑	1	0	1	X	0	1	0
↑	1	1	1	X	0	~Q	~QN
X	X	X	0	X	X	0	1



Capacitance

Pin	Cap [pF]
C	0.004
J	0.005
K	0.005
RN	0.011
SD	0.010
SE	0.006

Area

0.705 mils^2
455 µm^2

Power

2.2 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay C => Q	0.50	2.12	0.72	2.26	0.70	1.80	0.94	2.02
Delay C => QN	0.90	2.45	1.15	2.68	0.70	1.78	0.92	1.94
Delay RN => Q	n.a.	n.a.	n.a.	n.a.	0.22	1.31	0.65	1.75
Delay RN => QN	0.50	2.06	0.91	2.45	n.a.	n.a.	n.a.	n.a.
Slew C => Q	0.17	4.03	0.17	4.09	0.12	2.38	0.17	2.34
Slew C => QN	0.10	4.09	0.17	4.05	0.10	2.34	0.11	2.32
Slew RN => Q	n.a.	n.a.	n.a.	n.a.	0.14	2.34	0.22	2.30
Slew RN => QN	0.17	4.14	0.17	4.14	n.a.	n.a.	n.a.	n.a.

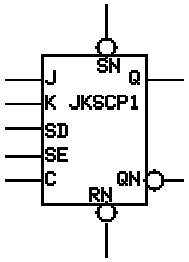
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
J => C	0.311	0.408	0	0
K => C	0.222	0.437	0	0
RN => C	0	n.a.	0.497	n.a.
SD => C	0	0.083	0	0
SE => C	0.16	0.401	0	0

	Min Width	
	High	**Low**
C	0.376	0.326
RN	n.a.	0.360

JKSCP1 is a Scan JK flip-flop with asynchronous active low CLEAR and PRESET and 1x drive strength. SCAN ENABLE switches between normal DATA and SCAN DATA input.

Truth Table

C	J	K	RN	SD	SE	SN	Q	QN
↑	0	1	1	X	0	1	0	1
↑	X	X	1	0	1	1	0	1
↑	X	X	1	1	1	1	1	0
↑	1	0	1	X	0	1	1	0
↑	1	1	1	X	0	1	~Q	~QN
X	X	X	0	X	X	0	0	0
X	X	X	0	X	X	1	0	1
X	X	X	1	X	X	0	1	0



Capacitance

Pin	Cap [pF]
C	0.004
J	0.005
K	0.005
RN	0.015
SD	0.009
SE	0.006
SN	0.013

Area

0.733 mils^2
473 µm^2

Power

1.58 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay C => Q	0.50	2.19	0.66	2.36	0.70	1.78	0.93	2.02
Delay C => QN	0.80	2.44	1.02	2.65	0.70	1.77	0.86	1.93
Delay RN => Q	0.13	1.81	0.20	1.84	0.20	1.30	0.65	1.74
Delay RN => QN	0.32	2.01	0.75	2.41	n.a.	n.a.	n.a.	n.a.
Delay SN => Q	0.40	2.07	0.84	2.47	n.a.	n.a.	n.a.	n.a.
Delay SN => QN	0.19	1.84	0.23	1.90	0.22	1.35	0.64	1.80
Slew C => Q	0.17	4.32	0.17	4.25	0.15	2.44	0.17	2.42
Slew C => QN	0.17	4.30	0.17	4.24	0.10	2.43	0.17	2.41
Slew RN => Q	0.17	4.30	0.17	4.33	0.10	2.46	0.17	2.49
Slew RN => QN	0.17	4.34	0.17	4.32	n.a.	n.a.	n.a.	n.a.
Slew SN => Q	0.17	4.27	0.17	4.31	n.a.	n.a.	n.a.	n.a.
Slew SN => QN	0.17	4.34	0.25	4.32	0.17	2.42	0.18	2.42

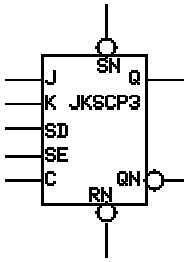
	Setup		Hold	
	rise	fall	rise	fall
J => C	0	0.355	0	0
K => C	0.202	0.495	0	0
RN => C	0	n.a.	0.487	n.a.
SD => C	0.068	0	0	0
SE => C	0.128	0.442	0	0
SN => C	0	n.a.	0.336	n.a.

	Min Width	
	High	Low
C	0.376	0.326
RN	n.a.	0.360
SN	n.a.	0.380

JKSCP3 is a Scan JK flip-flop with asynchronous active low CLEAR and PRESET and 3x drive strength. SCAN ENABLE switches between normal DATA and SCAN DATA input.

Truth Table

C	J	K	RN	SD	SE	SN	Q	QN
↑	0	1	1	X	0	1	0	1
↑	X	X	1	0	1	1	0	1
↑	X	X	1	1	1	1	1	0
↑	1	0	1	X	0	1	1	0
↑	1	1	1	X	0	1	~Q	~QN
X	X	X	0	X	X	0	0	0
X	X	X	0	X	X	1	0	1
X	X	X	1	X	X	0	1	0



Capacitance

Pin	Cap [pF]
C	0.004
J	0.005
K	0.005
RN	0.015
SD	0.009
SE	0.006
SN	0.013

Area

0.733 mils^2
473 µm^2

Power

2.24 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay C => Q	0.56	2.14	0.68	2.27	0.70	1.82	0.94	2.03
Delay C => QN	0.85	2.41	1.04	2.64	0.80	1.84	0.95	1.98
Delay RN => Q	0.20	1.73	0.20	1.79	0.22	1.32	0.64	1.75
Delay RN => QN	0.40	1.99	0.81	2.40	n.a.	n.a.	n.a.	n.a.
Delay SN => Q	0.50	2.03	0.87	2.42	n.a.	n.a.	n.a.	n.a.
Delay SN => QN	0.20	1.77	0.29	1.84	0.30	1.41	0.72	1.81
Slew C => Q	0.17	4.13	0.17	4.10	0.12	2.34	0.12	2.33
Slew C => QN	0.17	4.09	0.10	4.02	0.17	2.32	0.17	2.36
Slew RN => Q	0.17	4.10	0.14	4.12	0.17	2.35	0.18	2.38
Slew RN => QN	0.17	4.08	0.17	4.10	n.a.	n.a.	n.a.	n.a.
Slew SN => Q	0.17	4.13	0.17	4.08	n.a.	n.a.	n.a.	n.a.
Slew SN => QN	0.17	4.08	0.17	4.16	0.17	2.39	0.17	2.40

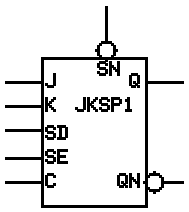
	Setup		Hold	
	rise	fall	rise	fall
J => C	0	0.358	0	0
K => C	0.298	0.495	0	0
RN => C	0	n.a.	0.487	n.a.
SD => C	0	0.002	0	0
SE => C	0.128	0.456	0	0
SN => C	0	n.a.	0.336	n.a.

	Min Width	
	High	Low
C	0.376	0.326
RN	n.a.	0.360
SN	n.a.	0.380

JKSP1 is a Scan JK flip-flop with asynchronous active low PRESET and 1x drive strength. SCAN ENABLE switches between normal DATA and SCAN DATA input.

Truth Table

C	J	K	SD	SE	SN	Q	QN
↑	0	1	X	0	1	0	1
↑	X	X	0	1	1	0	1
↑	X	X	1	1	1	1	0
↑	1	0	X	0	1	1	0
↑	1	1	X	0	1	~Q	~QN
X	X	X	X	X	0	1	0



Capacitance

Pin	Cap [pF]
C	0.004
J	0.005
K	0.005
SD	0.009
SE	0.006
SN	0.010

Area

0.705 mils^2
455 µm^2

Power

1.71 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay C => Q	0.60	2.24	0.75	2.37	0.60	1.74	0.84	1.94
Delay C => QN	0.70	2.37	0.94	2.60	0.70	1.79	0.86	1.94
Delay SN => Q	0.47	2.12	0.90	2.55	n.a.	n.a.	n.a.	n.a.
Delay SN => QN	n.a.	n.a.	n.a.	n.a.	0.20	1.33	0.64	1.78
Slew C => Q	0.17	4.32	0.17	4.29	0.11	2.39	0.11	2.39
Slew C => QN	0.11	4.25	0.11	4.24	0.10	2.45	0.10	2.45
Slew SN => Q	0.17	4.36	0.17	4.32	n.a.	n.a.	n.a.	n.a.
Slew SN => QN	n.a.	n.a.	n.a.	n.a.	0.17	2.46	0.17	2.42

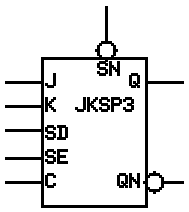
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
J => C	0.416	0.336	0	0
K => C	0.122	0.496	0	0
SD => C	0	0.032	0	0
SE => C	0.115	0.458	0	0
SN => C	0	n.a.	0.372	n.a.

	Min Width	
	High	**Low**
C	0.376	0.326
SN	n.a.	0.380

JKSP3 is a Scan JK flip-flop with asynchronous active low PRESET and 3x drive strength. SCAN ENABLE switches between normal DATA and SCAN DATA input.

Truth Table

C	J	K	SD	SE	SN	Q	QN
↑	0	1	X	0	1	0	1
↑	X	X	0	1	1	0	1
↑	X	X	1	1	1	1	0
↑	1	0	X	0	1	1	0
↑	1	1	X	0	1	~Q	~QN
X	X	X	X	X	0	1	0



Capacitance

Pin	Cap [pF]
C	0.004
J	0.005
K	0.005
SD	0.009
SE	0.006
SN	0.010

Area

0.705 mils^2
455 µm^2

Power

1.96 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay C => Q	0.60	2.18	0.76	2.32	0.68	1.75	0.85	1.99
Delay C => QN	0.80	2.34	1.04	2.59	0.80	1.87	0.96	2.02
Delay SN => Q	0.51	2.09	1.00	2.51	n.a.	n.a.	n.a.	n.a.
Delay SN => QN	n.a.	n.a.	n.a.	n.a.	0.30	1.37	0.72	1.79
Slew C => Q	0.11	4.13	0.15	4.06	0.12	2.31	0.12	2.31
Slew C => QN	0.10	4.02	0.11	4.02	0.11	2.40	0.17	2.35
Slew SN => Q	0.17	4.12	0.17	4.07	n.a.	n.a.	n.a.	n.a.
Slew SN => QN	n.a.	n.a.	n.a.	n.a.	0.17	2.39	0.17	2.40

	Setup		Hold	
	rise	**fall**	**rise**	**fall**
J => C	0.416	0.335	0	0
K => C	0	0.496	0	0
SD => C	0	0.002	0	0
SE => C	0.115	0.014	0	0
SN => C	0	n.a.	0.372	n.a.

	Min Width	
	High	**Low**
C	0.376	0.326
SN	n.a.	0.380

TIE0 is the tie-down to the logic low-level for all macro inputs.

Truth Table

Q
0

Area

0 mils^2
0 µm^2

TIE1 is the tie-up to the logic high-level for all macro inputs.

Truth Table

Q
1

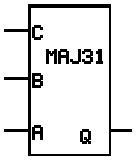
Area

0 mils^2
0 µm^2

MAJ31 is a majority circuit with 1x drive strength providing the logical function Q = (A.B+A.C+B.C)

Truth Table

A	B	C	Q
0	0	X	0
0	X	0	0
X	0	0	0
X	1	1	1
1	X	1	1
1	1	X	1



Capacitance

Pin	Cap [pF]
A	0.012
B	0.011
C	0.004

Area

0.169 mils^2
109 µm^2

Power

0.55 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

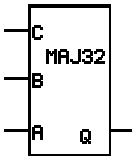
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay A => Q	0.19	1.65	0.24	1.71	0.25	1.20	0.56	1.52
Delay B => Q	0.17	1.64	0.22	1.68	0.22	1.20	0.52	1.50
Delay C => Q	0.17	1.64	0.25	1.71	0.20	1.17	0.56	1.54
Slew A => Q	0.10	3.79	0.13	3.79	0.10	2.03	0.14	2.01
Slew B => Q	0.10	3.78	0.13	3.74	0.10	2.03	0.13	2.04
Slew C => Q	0.10	3.78	0.13	3.79	0.11	2.03	0.15	2.03

MAJ32 is a majority circuit with 2x drive strength providing the logical function Q = (A.B+A.C+B.C)

Truth Table

A	B	C	Q
0	0	X	0
0	X	0	0
X	0	0	0
X	1	1	1
1	X	1	1
1	1	X	1



Capacitance

Pin	Cap [pF]
A	0.019
B	0.016
C	0.007

Area

0.197 mils^2
127 µm^2

Power

1 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

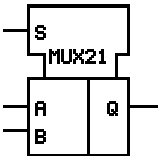
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**
Delay A => Q	0.16	1.74	0.16	1.75	0.21	1.27	0.47	1.55
Delay B => Q	0.17	1.75	0.27	1.85	0.21	1.27	0.57	1.63
Delay C => Q	0.14	1.72	0.19	1.77	0.17	1.23	0.50	1.58
Slew A => Q	0.10	4.14	0.14	4.12	0.10	2.34	0.14	2.32
Slew B => Q	0.10	4.13	0.14	4.13	0.10	2.34	0.13	2.33
Slew C => Q	0.10	4.14	0.14	4.14	0.10	2.34	0.14	2.33

MUX21 is a 2-input to 1-output digital multiplexer with 1x drive strength.

Truth Table

A	B	S	Q
0	X	0	0
X	0	1	0
X	1	1	1
1	X	0	1



Capacitance

Pin	Cap [pF]
A	0.005
B	0.005
S	0.008

Area

0.169 mils^2
109 µm^2

Power

0.49 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

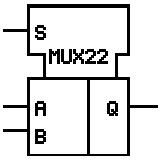
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay A => Q	0.17	1.82	0.16	1.82	0.22	1.30	0.49	1.59
Delay B => Q	0.16	1.82	0.16	1.82	0.23	1.31	0.49	1.59
Delay S => Q	0.14	1.79	0.17	1.83	0.29	1.37	0.35	1.42
Slew A => Q	0.12	4.29	0.15	4.30	0.11	2.40	0.15	2.40
Slew B => Q	0.12	4.31	0.15	4.31	0.11	2.40	0.15	2.39
Slew S => Q	0.11	4.25	0.15	4.28	0.11	2.38	0.10	2.39

MUX22 is a 2-input to 1-output digital multiplexer with 2x drive strength.

Truth Table

A	B	S	Q
0	X	0	0
X	0	1	0
X	1	1	1
1	X	0	1



Capacitance

Pin	Cap [pF]
A	0.009
B	0.009
S	0.011

Area

0.169 mils^2
109 µm^2

Power

0.94 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

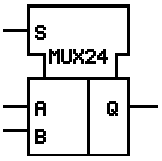
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**
Delay A => Q	0.15	1.74	0.13	1.72	0.19	1.24	0.45	1.52
Delay B => Q	0.14	1.72	0.13	1.72	0.20	1.25	0.46	1.53
Delay S => Q	0.12	1.70	0.14	1.72	0.26	1.31	0.27	1.32
Slew A => Q	0.10	4.13	0.13	4.13	0.09	2.33	0.14	2.33
Slew B => Q	0.10	4.10	0.13	4.14	0.09	2.33	0.13	2.33
Slew S => Q	0.09	4.13	0.13	4.11	0.09	2.33	0.09	2.32

MUX24 is a 2-input to 1-output digital multiplexer with 4x drive strength.

Truth Table

A	B	S	Q
0	X	0	0
X	0	1	0
X	1	1	1
1	X	0	1



Capacitance

Pin	Cap [pF]
A	0.017
B	0.019
S	0.020

Area

0.282 mils^2
182 µm^2

Power

1.62 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

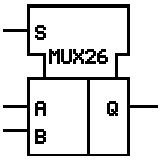
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.004**	**1.28**	**0.004**	**1.28**	**0.004**	**1.28**	**0.004**	**1.28**
Delay A => Q	0.10	1.69	0.11	1.70	0.14	1.18	0.45	1.51
Delay B => Q	0.15	1.73	0.15	1.74	0.20	1.27	0.46	1.55
Delay S => Q	0.12	1.70	0.20	1.78	0.25	1.30	0.28	1.34
Slew A => Q	0.07	4.10	0.10	4.11	0.06	2.33	0.10	2.32
Slew B => Q	0.08	4.11	0.11	4.07	0.08	2.30	0.13	2.32
Slew S => Q	0.07	4.04	0.11	4.04	0.08	2.30	0.07	2.31

MUX26 is a 2-input to 1-output digital multiplexer with 6x drive strength.

Truth Table

A	B	S	Q
0	X	0	0
X	0	1	0
X	1	1	1
1	X	0	1



Capacitance

Pin	Cap [pF]
A	0.025
B	0.019
S	0.035

Area

0.282 mils^2
182 µm^2

Power

2.44 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

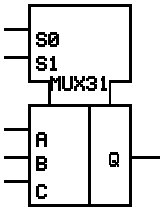
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.006**	**1.92**	**0.006**	**1.92**	**0.006**	**1.92**	**0.006**	**1.92**
Delay A => Q	0.11	1.70	0.14	1.73	0.15	1.15	0.47	1.49
Delay B => Q	0.14	1.72	0.26	1.82	0.18	1.19	0.38	1.43
Delay S => Q	0.13	1.71	0.10	1.69	0.24	1.24	0.34	1.33
Slew A => Q	0.07	4.11	0.11	4.11	0.07	2.20	0.11	2.18
Slew B => Q	0.08	4.08	0.11	4.11	0.07	2.19	0.12	2.19
Slew S => Q	0.07	4.09	0.11	4.03	0.07	2.19	0.07	2.18

MUX31 is a 3-input to 1-output digital multiplexer with 1x drive strength.

Truth Table

A	B	C	S0	S1	Q
0	X	X	0	0	0
X	0	X	1	0	0
X	X	0	X	1	0
X	X	1	X	1	1
X	1	X	1	0	1
1	X	X	0	0	1



Capacitance

Pin	Cap [pF]
A	0.007
B	0.007
C	0.005
S0	0.009
S1	0.007

Area

0.31 mils^2
200 µm^2

Power

0.7 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

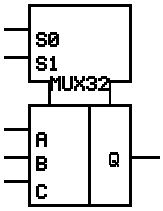
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay A => Q	0.26	1.92	0.27	1.94	0.29	1.44	0.57	1.74
Delay B => Q	0.24	1.91	0.27	1.94	0.31	1.46	0.57	1.74
Delay C => Q	0.17	1.83	0.18	1.84	0.23	1.32	0.51	1.61
Delay S0 => Q	0.22	1.88	0.31	1.97	0.41	1.56	0.53	1.67
Delay S1 => Q	0.14	1.80	0.17	1.81	0.34	1.43	0.40	1.48
Slew A => Q	0.14	4.29	0.17	4.31	0.15	2.40	0.19	2.41
Slew B => Q	0.14	4.32	0.17	4.31	0.15	2.40	0.19	2.41
Slew C => Q	0.13	4.29	0.17	4.28	0.12	2.40	0.17	2.39
Slew S0 => Q	0.13	4.32	0.17	4.32	0.15	2.41	0.15	2.40
Slew S1 => Q	0.12	4.29	0.16	4.30	0.12	2.41	0.12	2.40

MUX32 is a 3-input to 1-output digital multiplexer with 2x drive strength.

Truth Table

A	B	C	S0	S1	Q
0	X	X	0	0	0
X	0	X	1	0	0
X	X	0	X	1	0
X	X	1	X	1	1
X	1	X	1	0	1
1	X	X	0	0	1



Capacitance

Pin	Cap [pF]
A	0.014
B	0.015
C	0.007
S0	0.016
S1	0.012

Area

0.367 mils^2
237 µm^2

Power

1.33 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

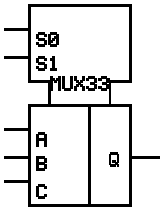
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**
Delay A => Q	0.23	1.89	0.24	1.91	0.27	1.46	0.55	1.75
Delay B => Q	0.22	1.88	0.24	1.91	0.28	1.47	0.55	1.75
Delay C => Q	0.13	1.78	0.22	1.86	0.18	1.28	0.39	1.53
Delay S0 => Q	0.19	1.86	0.27	1.94	0.37	1.55	0.47	1.64
Delay S1 => Q	0.11	1.77	0.05	1.71	0.30	1.40	0.41	1.51
Slew A => Q	0.10	4.30	0.14	4.29	0.12	2.46	0.15	2.45
Slew B => Q	0.10	4.29	0.14	4.29	0.12	2.46	0.15	2.45
Slew C => Q	0.09	4.27	0.12	4.30	0.08	2.46	0.14	2.46
Slew S0 => Q	0.10	4.28	0.13	4.29	0.12	2.46	0.12	2.45
Slew S1 => Q	0.08	4.29	0.11	4.31	0.07	2.45	0.08	2.45

MUX33 is a 3-input to 1-output digital multiplexer with 3x drive strength.

Truth Table

A	B	C	S0	S1	Q
0	X	X	0	0	0
X	0	X	1	0	0
X	X	0	X	1	0
X	X	1	X	1	1
X	1	X	1	0	1
1	X	X	0	0	1



Capacitance

Pin	Cap [pF]
A	0.024
B	0.019
C	0.012
S0	0.034
S1	0.024

Area

0.451 mils^2
291 µm^2

Power

2.24 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

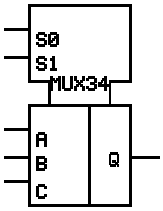
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay A => Q	0.21	1.75	0.30	1.86	0.25	1.35	0.60	1.71
Delay B => Q	0.25	1.81	0.41	1.96	0.28	1.39	0.49	1.63
Delay C => Q	0.11	1.64	0.12	1.66	0.14	1.16	0.45	1.49
Delay S0 => Q	0.23	1.78	0.26	1.82	0.33	1.44	0.43	1.53
Delay S1 => Q	0.11	1.65	0.04	1.59	0.24	1.25	0.25	1.27
Slew A => Q	0.11	4.01	0.14	4.04	0.12	2.29	0.17	2.29
Slew B => Q	0.11	4.04	0.15	4.03	0.13	2.29	0.19	2.30
Slew C => Q	0.09	4.00	0.12	4.01	0.07	2.28	0.12	2.27
Slew S0 => Q	0.11	4.03	0.14	4.03	0.13	2.28	0.13	2.27
Slew S1 => Q	0.08	4.00	0.13	4.03	0.07	2.28	0.09	2.27

MUX34 is a 3-input to 1-output digital multiplexer with 4x drive strength.

Truth Table

A	B	C	S0	S1	Q
0	X	X	0	0	0
X	0	X	1	0	0
X	X	0	X	1	0
X	X	1	X	1	1
X	1	X	1	0	1
1	X	X	0	0	1



Capacitance

Pin	Cap [pF]
A	0.037
B	0.037
C	0.026
S0	0.037
S1	0.028

Area

0.621 mils^2
401 µm^2

Power

3.07 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

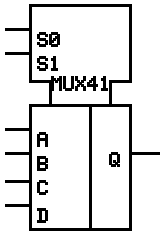
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.004**	**1.28**	**0.004**	**1.28**	**0.004**	**1.28**	**0.004**	**1.28**
Delay A => Q	0.19	1.74	0.17	1.74	0.23	1.31	0.49	1.61
Delay B => Q	0.17	1.73	0.17	1.74	0.24	1.32	0.50	1.61
Delay C => Q	0.12	1.67	0.10	1.66	0.17	1.19	0.41	1.47
Delay S0 => Q	0.15	1.70	0.19	1.75	0.29	1.38	0.38	1.46
Delay S1 => Q	0.08	1.63	0.06	1.61	0.26	1.29	0.38	1.40
Slew A => Q	0.08	4.02	0.11	4.03	0.09	2.29	0.14	2.28
Slew B => Q	0.08	4.00	0.11	4.02	0.09	2.28	0.13	2.28
Slew C => Q	0.08	4.03	0.11	4.01	0.07	2.29	0.11	2.28
Slew S0 => Q	0.08	4.02	0.11	4.03	0.10	2.28	0.09	2.28
Slew S1 => Q	0.06	4.03	0.10	4.03	0.07	2.29	0.06	2.28

MUX41 is a 4-input to 1-output digital multiplexer with 1x drive strength.

Truth Table

A	B	C	D	S0	S1	Q
0	X	X	X	0	0	0
X	0	X	X	1	0	0
X	X	0	X	0	1	0
X	X	X	0	1	1	0
X	X	X	1	1	1	1
X	X	1	X	0	1	1
X	1	X	X	1	0	1
1	X	X	X	0	0	1



Capacitance

Pin	Cap [pF]
A	0.007
B	0.007
C	0.007
D	0.007
S0	0.018
S1	0.007

Area

0.367 mils^2
237 µm^2

Power

0.68 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

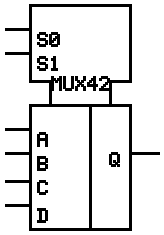
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay A => Q	0.24	1.90	0.27	1.94	0.29	1.44	0.58	1.73
Delay B => Q	0.23	1.90	0.26	1.93	0.29	1.44	0.56	1.73
Delay C => Q	0.24	1.91	0.27	1.94	0.30	1.45	0.59	1.75
Delay D => Q	0.24	1.90	0.28	1.94	0.30	1.45	0.57	1.74
Delay S0 => Q	0.21	1.87	0.29	1.96	0.40	1.55	0.51	1.66
Delay S1 => Q	0.12	1.79	0.09	1.75	0.17	1.31	0.34	1.46
Slew A => Q	0.12	4.30	0.15	4.29	0.13	2.40	0.17	2.39
Slew B => Q	0.13	4.25	0.16	4.27	0.14	2.40	0.17	2.39
Slew C => Q	0.12	4.30	0.16	4.30	0.15	2.41	0.18	2.41
Slew D => Q	0.12	4.27	0.16	4.28	0.14	2.41	0.18	2.41
Slew S0 => Q	0.13	4.29	0.16	4.31	0.14	2.41	0.15	2.41
Slew S1 => Q	0.11	4.29	0.13	4.25	0.13	2.42	0.11	2.39

MUX42 is a 4-input to 1-output digital multiplexer with 2x drive strength.

Truth Table

A	B	C	D	S0	S1	Q
0	X	X	X	0	0	0
X	0	X	X	1	0	0
X	X	0	X	0	1	0
X	X	X	0	1	1	0
X	X	X	1	1	1	1
X	X	1	X	0	1	1
X	1	X	X	1	0	1
1	X	X	X	0	0	1



Capacitance

Pin	Cap [pF]
A	0.012
B	0.013
C	0.013
D	0.013
S0	0.031
S1	0.012

Area

0.423 mils^2
273 µm^2

Power

1.27 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

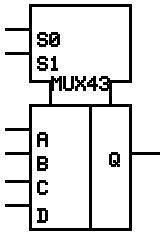
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**
Delay A => Q	0.21	1.82	0.23	1.83	0.28	1.37	0.53	1.67
Delay B => Q	0.21	1.80	0.23	1.84	0.26	1.38	0.53	1.68
Delay C => Q	0.21	1.81	0.23	1.85	0.28	1.37	0.53	1.67
Delay D => Q	0.20	1.80	0.22	1.84	0.27	1.39	0.54	1.68
Delay S0 => Q	0.18	1.77	0.25	1.85	0.35	1.46	0.44	1.55
Delay S1 => Q	0.10	1.70	0.07	1.66	0.16	1.27	0.33	1.41
Slew A => Q	0.10	4.12	0.14	4.12	0.12	2.34	0.16	2.34
Slew B => Q	0.11	4.10	0.14	4.11	0.12	2.34	0.15	2.34
Slew C => Q	0.11	4.12	0.14	4.12	0.12	2.32	0.17	2.34
Slew D => Q	0.11	4.13	0.14	4.12	0.13	2.35	0.15	2.34
Slew S0 => Q	0.10	4.13	0.14	4.14	0.13	2.34	0.12	2.34
Slew S1 => Q	0.09	4.12	0.11	4.05	0.11	2.34	0.10	2.33

MUX43 is a 4-input to 1-output digital multiplexer with 3x drive strength.

Truth Table

A	B	C	D	S0	S1	Q
0	X	X	X	0	0	0
X	0	X	X	1	0	0
X	X	0	X	0	1	0
X	X	X	0	1	1	0
X	X	X	1	1	1	1
X	X	1	X	0	1	1
X	1	X	X	1	0	1
1	X	X	X	0	0	1



Capacitance

Pin	Cap [pF]
A	0.024
B	0.017
C	0.024
D	0.017
S0	0.071
S1	0.021

Area

0.592 mils^2
382 µm^2

Power

2.08 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay A => Q	0.20	1.75	0.26	1.83	0.22	1.35	0.56	1.72
Delay B => Q	0.17	1.74	0.24	1.80	0.22	1.32	0.56	1.69
Delay C => Q	0.20	1.75	0.30	1.82	0.20	1.34	0.57	1.69
Delay D => Q	0.20	1.75	0.22	1.78	0.21	1.34	0.58	1.72
Delay S0 => Q	0.20	1.76	0.21	1.77	0.32	1.43	0.42	1.52
Delay S1 => Q	0.09	1.67	0.02	1.62	0.14	1.25	0.29	1.37
Slew A => Q	0.09	4.05	0.13	4.07	0.11	2.32	0.15	2.31
Slew B => Q	0.09	4.08	0.13	4.08	0.10	2.32	0.14	2.32
Slew C => Q	0.13	4.18	0.17	4.10	0.04	2.38	0.17	2.29
Slew D => Q	0.17	4.04	0.13	4.11	0.10	2.31	0.17	2.42
Slew S0 => Q	0.14	4.08	0.17	4.08	0.17	2.32	0.11	2.36
Slew S1 => Q	0.09	4.07	0.11	4.04	0.10	2.31	0.09	2.32

NAND20 is a 2-input NAND gate with 0.5x drive strength.

Truth Table

A	B	Q
0	X	1
X	0	1
1	1	0

Capacitance

Pin	Cap [pF]
A	0.003
B	0.004

Area

0.085 mils^2
55 µm^2

Power

0.18 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**
Delay A => Q	0.07	1.92	0.42	2.29	0.04	0.87	-0.10	1.11
Delay B => Q	0.10	1.95	0.51	2.32	0.04	0.88	-0.13	0.96
Slew A => Q	0.14	4.72	0.38	4.68	0.07	2.05	0.39	2.20
Slew B => Q	0.20	4.73	0.42	4.71	0.07	2.06	0.40	2.14

NAND21 is a 2-input NAND gate with 1x drive strength.

Truth Table

A	B	Q
0	X	1
X	0	1
1	1	0

Capacitance

Pin	Cap [pF]
A	0.005
B	0.007

Area

0.085 mils^2
55 µm^2

Power

0.35 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay A => Q	0.06	1.73	0.38	2.08	0.03	0.85	-0.11	1.08
Delay B => Q	0.08	1.75	0.47	2.12	0.04	0.86	-0.14	0.94
Slew A => Q	0.10	4.30	0.34	4.25	0.05	1.99	0.36	2.15
Slew B => Q	0.16	4.34	0.39	4.31	0.05	2.00	0.39	2.09

NAND22 is a 2-input NAND gate with 2x drive strength.

Truth Table

A	B	Q
0	X	1
X	0	1
1	1	0

Capacitance

Pin	Cap [pF]
A	0.008
B	0.013

Area

0.085 mils^2
55 µm^2

Power

0.7 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**
Delay A => Q	0.05	1.62	0.35	2.00	0.03	0.83	-0.11	1.08
Delay B => Q	0.07	1.64	0.43	2.04	0.03	0.84	-0.15	0.93
Slew A => Q	0.08	4.08	0.32	4.10	0.04	1.96	0.34	2.12
Slew B => Q	0.13	4.14	0.36	4.13	0.04	1.96	0.37	2.06

NAND23 is a 2-input NAND gate with 3x drive strength.

Truth Table

A	B	Q
0	X	1
X	0	1
1	1	0

Capacitance

Pin	Cap [pF]
A	0.013
B	0.020

Area

0.141 mils^2
91 µm^2

Power

1 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay A => Q	0.04	1.67	0.34	2.03	0.03	0.83	-0.13	1.08
Delay B => Q	0.08	1.70	0.46	2.07	0.04	0.85	-0.15	0.94
Slew A => Q	0.07	4.19	0.30	4.15	0.04	1.97	0.33	2.13
Slew B => Q	0.15	4.20	0.38	4.19	0.04	1.98	0.39	2.07

NAND24 is a 2-input NAND gate with 4x drive strength.

Truth Table

A	B	Q
0	X	1
X	0	1
1	1	0

Capacitance

Pin	Cap [pF]
A	0.017
B	0.026

Area

0.169 mils^2
109 µm^2

Power

1.38 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.004**	**1.28**	**0.004**	**1.28**	**0.004**	**1.28**	**0.004**	**1.28**
Delay A => Q	0.04	1.63	0.34	2.00	0.03	0.83	-0.12	1.07
Delay B => Q	0.07	1.64	0.43	2.04	0.03	0.84	-0.16	0.92
Slew A => Q	0.07	4.07	0.31	4.09	0.04	1.96	0.34	2.12
Slew B => Q	0.12	4.12	0.35	4.12	0.04	1.96	0.36	2.06

NAND26 is a 2-input NAND gate with 6x drive strength.

Truth Table

A	B	Q
0	X	1
X	0	1
1	1	0

Capacitance

Pin	Cap [pF]
A	0.025
B	0.039

Area

0.254 mils^2
164 µm^2

Power

2.04 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.006**	**1.92**	**0.006**	**1.92**	**0.006**	**1.92**	**0.006**	**1.92**
Delay A => Q	0.04	1.65	0.34	2.01	0.03	0.84	-0.12	1.08
Delay B => Q	0.07	1.67	0.44	2.03	0.04	0.85	-0.15	0.93
Slew A => Q	0.07	4.13	0.31	4.09	0.04	1.95	0.34	2.12
Slew B => Q	0.14	4.14	0.37	4.15	0.04	1.97	0.38	2.06

NAND28 is a 2-input NAND gate with 8x drive strength.

Truth Table

A	B	Q
0	X	1
X	0	1
1	1	0

Capacitance

Pin	Cap [pF]
A	0.034
B	0.052

Area

0.282 mils^2
182 µm^2

Power

2.73 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.008**	**2.56**	**0.008**	**2.56**	**0.008**	**2.56**	**0.008**	**2.56**
Delay A => Q	0.04	1.64	0.34	1.99	0.03	0.83	-0.13	1.07
Delay B => Q	0.06	1.65	0.43	2.04	0.03	0.84	-0.16	0.92
Slew A => Q	0.07	4.11	0.30	4.09	0.04	1.95	0.34	2.12
Slew B => Q	0.12	4.14	0.34	4.12	0.04	1.96	0.35	2.06

NAND30 is a 3-input NAND gate with 0.5x drive strength.

Truth Table

A	B	C	Q
0	X	X	1
X	0	X	1
X	X	0	1
1	1	1	0

Capacitance

Pin	Cap [pF]
A	0.003
B	0.004
C	0.005

Area

0.113 mils^2
73 µm^2

Power

0.21 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**
Delay A => Q	0.11	1.94	0.50	2.32	0.04	0.80	-0.10	1.01
Delay B => Q	0.15	1.98	0.59	2.36	0.06	0.81	-0.11	0.91
Delay C => Q	0.19	2.04	0.66	2.42	0.07	0.82	-0.15	0.80
Slew A => Q	0.20	4.78	0.42	4.72	0.10	1.93	0.43	2.09
Slew B => Q	0.29	4.80	0.49	4.80	0.10	1.93	0.45	2.07
Slew C => Q	0.38	4.90	0.56	4.90	0.10	1.92	0.43	2.01

NAND31 is a 3-input NAND gate with 1x drive strength.

Truth Table

A	B	C	Q
0	X	X	1
X	0	X	1
X	X	0	1
1	1	1	0

Capacitance

Pin	Cap [pF]
A	0.005
B	0.005
C	0.009

Area

0.113 mils^2
73 µm^2

Power

0.41 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay A => Q	0.09	1.74	0.45	2.13	0.04	0.78	-0.11	1.00
Delay B => Q	0.13	1.80	0.54	2.17	0.05	0.80	-0.12	0.90
Delay C => Q	0.16	1.84	0.61	2.21	0.06	0.80	-0.16	0.78
Slew A => Q	0.15	4.34	0.38	4.35	0.08	1.89	0.41	2.06
Slew B => Q	0.24	4.40	0.45	4.38	0.09	1.89	0.45	2.04
Slew C => Q	0.31	4.48	0.52	4.47	0.09	1.88	0.42	1.99

NAND32 is a 3-input NAND gate with 2x drive strength.

Truth Table

A	B	C	Q
0	X	X	1
X	0	X	1
X	X	0	1
1	1	1	0

Capacitance

Pin	Cap [pF]
A	0.011
B	0.011
C	0.018

Area

0.197 mils^2
127 µm^2

Power

0.78 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**
Delay A => Q	0.07	1.76	0.43	2.12	0.03	0.78	-0.13	0.99
Delay B => Q	0.11	1.79	0.53	2.16	0.05	0.79	-0.14	0.89
Delay C => Q	0.15	1.82	0.59	2.19	0.05	0.80	-0.17	0.77
Slew A => Q	0.13	4.37	0.36	4.32	0.07	1.88	0.38	2.05
Slew B => Q	0.21	4.38	0.42	4.37	0.07	1.87	0.43	2.02
Slew C => Q	0.29	4.46	0.49	4.45	0.08	1.87	0.41	1.98

NAND33 is a 3-input NAND gate with 3x drive strength.

Truth Table

A	B	C	Q
0	X	X	1
X	0	X	1
X	X	0	1
1	1	1	0

Capacitance

Pin	Cap [pF]
A	0.013
B	0.013
C	0.024

Area

0.197 mils^2
127 µm^2

Power

1.19 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay A => Q	0.07	1.66	0.42	2.01	0.04	0.77	-0.12	0.99
Delay B => Q	0.10	1.68	0.50	2.04	0.05	0.78	-0.13	0.89
Delay C => Q	0.13	1.71	0.57	2.08	0.05	0.79	-0.17	0.77
Slew A => Q	0.13	4.15	0.36	4.11	0.07	1.86	0.39	2.03
Slew B => Q	0.19	4.16	0.41	4.14	0.07	1.86	0.43	2.01
Slew C => Q	0.26	4.21	0.47	4.20	0.07	1.86	0.41	1.96

NAND34 is a 3-input NAND gate with 4x drive strength.

Truth Table

A	B	C	Q
0	X	X	1
X	0	X	1
X	X	0	1
1	1	1	0

Capacitance

Pin	Cap [pF]
A	0.018
B	0.018
C	0.032

Area

0.254 mils^2
164 µm^2

Power

1.59 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.004**	**1.28**	**0.004**	**1.28**	**0.004**	**1.28**	**0.004**	**1.28**
Delay A => Q	0.07	1.63	0.42	2.00	0.04	0.78	-0.11	1.00
Delay B => Q	0.10	1.65	0.50	2.04	0.05	0.79	-0.13	0.90
Delay C => Q	0.13	1.69	0.57	2.06	0.05	0.80	-0.17	0.77
Slew A => Q	0.13	4.09	0.37	4.07	0.07	1.86	0.39	2.04
Slew B => Q	0.19	4.11	0.42	4.11	0.07	1.87	0.43	2.02
Slew C => Q	0.26	4.19	0.47	4.18	0.07	1.87	0.41	1.97

NAND40 is a 4-input NAND gate with 0.5x drive strength.

Truth Table

A	B	C	D	Q
0	X	X	X	1
X	0	X	X	1
X	X	0	X	1
X	X	X	0	1
1	1	1	1	0

Capacitance

Pin	Cap [pF]
A	0.004
B	0.004
C	0.004
D	0.006

Area

0.141 mils^2
91 µm^2

Power

0.24 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**
Delay A => Q	0.14	1.99	0.55	2.34	0.05	0.77	-0.10	0.96
Delay B => Q	0.20	2.04	0.65	2.42	0.07	0.79	-0.09	0.89
Delay C => Q	0.26	2.10	0.73	2.49	0.08	0.80	-0.11	0.80
Delay D => Q	0.30	2.15	0.80	2.55	0.09	0.81	-0.14	0.72
Slew A => Q	0.26	4.85	0.47	4.79	0.13	1.89	0.46	2.08
Slew B => Q	0.38	4.91	0.57	4.89	0.14	1.89	0.50	2.06
Slew C => Q	0.49	5.02	0.66	5.02	0.14	1.90	0.49	2.00
Slew D => Q	0.61	5.14	0.75	5.13	0.14	1.89	0.44	1.97

NAND41 is a 4-input NAND gate with 1x drive strength.

Truth Table

A	B	C	D	Q
0	X	X	X	1
X	0	X	X	1
X	X	0	X	1
X	X	X	0	1
1	1	1	1	0

Capacitance

Pin	Cap [pF]
A	0.006
B	0.006
C	0.006
D	0.011

Area

0.141 mils^2
91 µm^2

Power

0.46 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay A => Q	0.11	1.80	0.51	2.16	0.04	0.76	-0.10	0.95
Delay B => Q	0.17	1.82	0.60	2.21	0.06	0.77	-0.10	0.88
Delay C => Q	0.21	1.88	0.67	2.26	0.07	0.79	-0.12	0.79
Delay D => Q	0.25	1.92	0.73	2.32	0.08	0.79	-0.15	0.70
Slew A => Q	0.21	4.44	0.43	4.41	0.12	1.86	0.44	2.04
Slew B => Q	0.31	4.46	0.51	4.46	0.12	1.87	0.49	2.03
Slew C => Q	0.41	4.58	0.59	4.57	0.12	1.86	0.48	1.96
Slew D => Q	0.50	4.67	0.66	4.66	0.12	1.85	0.43	1.95

NAND42 is a 4-input NAND gate with 2x drive strength.

Truth Table

A	B	C	D	Q
0	X	X	X	1
X	0	X	X	1
X	X	0	X	1
X	X	X	0	1
1	1	1	1	0

Capacitance

Pin	Cap [pF]
A	0.020
B	0.012
C	0.011
D	0.011

Area

0.226 mils^2
146 µm^2

Power

1.23 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**
Delay A => Q	0.21	1.81	0.68	2.17	0.07	0.79	-0.17	0.70
Delay B => Q	0.18	1.79	0.62	2.15	0.06	0.78	-0.14	0.78
Delay C => Q	0.14	1.75	0.55	2.10	0.05	0.77	-0.13	0.87
Delay D => Q	0.09	1.67	0.46	2.07	0.04	0.75	-0.13	0.95
Slew A => Q	0.42	4.43	0.59	4.42	0.10	1.85	0.40	1.93
Slew B => Q	0.33	4.35	0.52	4.33	0.10	1.84	0.47	1.97
Slew C => Q	0.24	4.26	0.44	4.26	0.10	1.85	0.47	2.02
Slew D => Q	0.15	4.18	0.37	4.22	0.09	1.85	0.41	2.04

NAND43 is a 4-input NAND gate with 3x drive strength.

Truth Table

A	B	C	D	Q
0	X	X	X	1
X	0	X	X	1
X	X	0	X	1
X	X	X	0	1
1	1	1	1	0

Capacitance

Pin	Cap [pF]
A	0.029
B	0.017
C	0.016
D	0.017

Area

0.31 mils^2
200 µm^2

Power

1.84 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay A => Q	0.22	1.83	0.69	2.20	0.07	0.77	-0.18	0.68
Delay B => Q	0.18	1.81	0.63	2.17	0.07	0.77	-0.15	0.77
Delay C => Q	0.14	1.76	0.56	2.12	0.05	0.75	-0.13	0.86
Delay D => Q	0.09	1.71	0.47	2.09	0.04	0.74	-0.14	0.94
Slew A => Q	0.42	4.49	0.59	4.48	0.10	1.81	0.39	1.90
Slew B => Q	0.34	4.41	0.52	4.39	0.10	1.82	0.46	1.94
Slew C => Q	0.24	4.32	0.44	4.31	0.10	1.81	0.46	1.98
Slew D => Q	0.15	4.25	0.37	4.21	0.09	1.81	0.40	2.01

NOR20 is a 2-input NOR gate with 0.5x drive strength.

Truth Table

A	B	Q
0	0	1
X	1	0
1	X	0

Capacitance

Pin	Cap [pF]
A	0.004
B	0.004

Area

0.085 mils^2
55 µm^2

Power

0.22 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

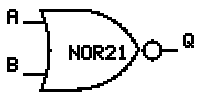
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**
Delay A => Q	0.09	1.70	0.23	1.90	0.08	1.17	0.20	1.45
Delay B => Q	0.07	1.69	0.29	1.99	0.06	1.15	0.09	1.42
Slew A => Q	0.17	4.25	0.51	4.22	0.14	2.59	0.54	2.64
Slew B => Q	0.17	4.22	0.47	4.24	0.08	2.54	0.41	2.59

NOR21 is a 2-input NOR gate with 1x drive strength.

Truth Table

A	B	Q
0	0	1
X	1	0
1	X	0



Capacitance

Pin	Cap [pF]
A	0.007
B	0.007

Area

0.085 mils^2
55 µm^2

Power

0.43 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay A => Q	0.08	1.63	0.20	1.81	0.07	1.11	0.17	1.39
Delay B => Q	0.06	1.61	0.26	1.92	0.05	1.08	0.06	1.36
Slew A => Q	0.14	4.06	0.48	4.07	0.11	2.44	0.51	2.50
Slew B => Q	0.13	4.07	0.41	4.07	0.06	2.40	0.36	2.46

NOR22 is a 2-input NOR gate with 2x drive strength.

Truth Table

A	B	Q
0	0	1
X	1	0
1	X	0

Capacitance

Pin	Cap [pF]
A	0.014
B	0.014

Area

0.113 mils^2
73 µm^2

Power

0.83 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**
Delay A => Q	0.07	1.59	0.19	1.77	0.06	1.07	0.15	1.36
Delay B => Q	0.05	1.58	0.25	1.89	0.05	1.05	0.06	1.34
Slew A => Q	0.13	4.00	0.46	4.01	0.10	2.36	0.49	2.42
Slew B => Q	0.12	3.96	0.40	3.98	0.06	2.35	0.36	2.41

NOR23 is a 2-input NOR gate with 3x drive strength.

Truth Table

A	B	Q
0	0	1
X	1	0
1	X	0

Capacitance

Pin	Cap [pF]
A	0.021
B	0.020

Area

0.141 mils^2
91 µm^2

Power

1.2 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay A => Q	0.07	1.60	0.18	1.78	0.06	1.06	0.14	1.35
Delay B => Q	0.05	1.58	0.24	1.90	0.04	1.04	0.04	1.33
Slew A => Q	0.12	4.00	0.44	4.01	0.09	2.33	0.48	2.40
Slew B => Q	0.11	3.97	0.37	3.99	0.05	2.32	0.34	2.39

NOR24 is a 2-input NOR gate with 4x drive strength.

Truth Table

A	B	Q
0	0	1
X	1	0
1	X	0

Capacitance

Pin	Cap [pF]
A	0.028
B	0.027

Area

0.169 mils^2
109 µm^2

Power

1.53 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.004**	**1.28**	**0.004**	**1.28**	**0.004**	**1.28**	**0.004**	**1.28**
Delay A => Q	0.06	1.58	0.16	1.76	0.05	1.06	0.13	1.34
Delay B => Q	0.04	1.57	0.21	1.88	0.04	1.04	0.01	1.32
Slew A => Q	0.10	3.96	0.42	3.96	0.07	2.33	0.46	2.38
Slew B => Q	0.09	3.93	0.34	3.97	0.03	2.29	0.31	2.36

NOR30 is a 3-input NOR gate with 0.5x drive strength.

Truth Table

A	B	C	Q
0	0	0	1
X	X	1	0
X	1	X	0
1	X	X	0

Capacitance

Pin	Cap [pF]
A	0.006
B	0.006
C	0.006

Area

0.113 mils^2
73 µm^2

Power

0.27 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

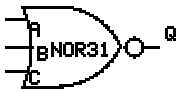
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**
Delay A => Q	0.13	1.69	0.37	1.98	0.12	1.20	0.24	1.48
Delay B => Q	0.17	1.73	0.34	1.93	0.15	1.23	0.33	1.51
Delay C => Q	0.19	1.75	0.27	1.83	0.17	1.26	0.39	1.55
Slew A => Q	0.36	4.29	0.66	4.30	0.18	2.65	0.52	2.67
Slew B => Q	0.37	4.31	0.70	4.31	0.25	2.69	0.62	2.72
Slew C => Q	0.37	4.28	0.70	4.31	0.31	2.75	0.73	2.80

NOR31 is a 3-input NOR gate with 1x drive strength.

Truth Table

A	B	C	Q
0	0	0	1
X	X	1	0
X	1	X	0
1	X	X	0



Capacitance

Pin	Cap [pF]
A	0.010
B	0.010
C	0.010

Area

0.113 mils^2
73 µm^2

Power

0.42 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay A => Q	0.07	1.59	0.26	1.88	0.07	1.10	0.13	1.39
Delay B => Q	0.11	1.63	0.24	1.82	0.10	1.13	0.23	1.42
Delay C => Q	0.12	1.65	0.17	1.73	0.11	1.16	0.30	1.45
Slew A => Q	0.20	4.04	0.49	4.05	0.08	2.42	0.39	2.47
Slew B => Q	0.21	4.07	0.57	4.07	0.14	2.47	0.52	2.51
Slew C => Q	0.22	4.06	0.58	4.05	0.20	2.53	0.64	2.58

NOR32 is a 3-input NOR gate with 2x drive strength.

Truth Table

A	B	C	Q
0	0	0	1
X	X	1	0
X	1	X	0
1	X	X	0

Capacitance

Pin	Cap [pF]
A	0.019
B	0.019
C	0.019

Area

0.141 mils^2
91 µm^2

Power

1.07 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**
Delay A => Q	0.11	1.62	0.15	1.70	0.10	1.12	0.28	1.42
Delay B => Q	0.09	1.60	0.22	1.79	0.09	1.09	0.21	1.39
Delay C => Q	0.05	1.56	0.23	1.85	0.06	1.07	0.10	1.36
Slew A => Q	0.19	3.99	0.56	4.00	0.18	2.45	0.62	2.50
Slew B => Q	0.19	3.99	0.53	4.00	0.12	2.39	0.49	2.44
Slew C => Q	0.17	3.97	0.45	3.98	0.06	2.35	0.35	2.40

NOR33 is a 3-input NOR gate with 3x drive strength.

Truth Table

A	B	C	Q
0	0	0	1
X	X	1	0
X	1	X	0
1	X	X	0

Capacitance

Pin	Cap [pF]
A	0.029
B	0.028
C	0.028

Area

0.197 mils^2
127 µm^2

Power

1.57 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay A => Q	0.10	1.61	0.14	1.68	0.10	1.13	0.28	1.42
Delay B => Q	0.09	1.59	0.20	1.78	0.09	1.10	0.20	1.39
Delay C => Q	0.05	1.55	0.22	1.84	0.05	1.08	0.09	1.36
Slew A => Q	0.17	3.97	0.55	3.96	0.17	2.47	0.61	2.51
Slew B => Q	0.17	3.96	0.53	3.97	0.12	2.40	0.49	2.45
Slew C => Q	0.15	3.94	0.42	3.96	0.05	2.35	0.33	2.41

NOR40 is a 4-input NOR gate with 0.5x drive strength.

Truth Table

A	B	C	D	Q
0	0	0	0	1
X	X	X	1	0
X	X	1	X	0
X	1	X	X	0
1	X	X	X	0

Capacitance

Pin	Cap [pF]
A	0.007
B	0.007
C	0.007
D	0.007

Area

0.113 mils^2
73 µm^2

Power

0.42 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

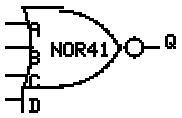
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**
Delay A => Q	0.22	1.76	0.24	1.80	0.21	1.34	0.48	1.62
Delay B => Q	0.20	1.75	0.28	1.85	0.20	1.30	0.43	1.58
Delay C => Q	0.17	1.71	0.32	1.90	0.17	1.26	0.36	1.54
Delay D => Q	0.08	1.62	0.30	1.89	0.10	1.19	0.24	1.49
Slew A => Q	0.40	4.25	0.72	4.26	0.42	2.88	0.83	2.90
Slew B => Q	0.40	4.27	0.75	4.29	0.34	2.80	0.73	2.82
Slew C => Q	0.40	4.26	0.74	4.28	0.26	2.70	0.61	2.73
Slew D => Q	0.34	4.28	0.64	4.28	0.15	2.59	0.45	2.65

NOR41 is a 4-input NOR gate with 1x drive strength.

Truth Table

A	B	C	D	Q
0	0	0	0	1
X	X	X	1	0
X	X	1	X	0
X	1	X	X	0
1	X	X	X	0



Capacitance

Pin	Cap [pF]
A	0.012
B	0.012
C	0.012
D	0.012

Area

0.141 mils^2
91 µm^2

Power

0.75 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

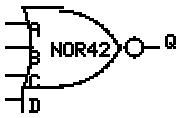
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay A => Q	0.19	1.70	0.20	1.73	0.18	1.25	0.43	1.54
Delay B => Q	0.17	1.69	0.24	1.79	0.16	1.21	0.38	1.50
Delay C => Q	0.13	1.65	0.28	1.83	0.13	1.16	0.30	1.46
Delay D => Q	0.07	1.58	0.27	1.85	0.09	1.12	0.19	1.42
Slew A => Q	0.33	4.11	0.68	4.16	0.34	2.69	0.78	2.72
Slew B => Q	0.33	4.13	0.69	4.14	0.27	2.60	0.67	2.64
Slew C => Q	0.32	4.13	0.68	4.15	0.19	2.51	0.55	2.55
Slew D => Q	0.28	4.15	0.58	4.14	0.11	2.46	0.40	2.50

NOR42 is a 4-input NOR gate with 2x drive strength.

Truth Table

A	B	C	D	Q
0	0	0	0	1
X	X	X	1	0
X	X	1	X	0
X	1	X	X	0
1	X	X	X	0



Capacitance

Pin	Cap [pF]
A	0.024
B	0.025
C	0.025
D	0.025

Area

0.254 mils^2
164 µm^2

Power

1.51 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

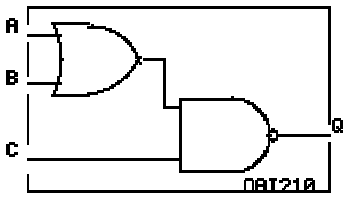
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**
Delay A => Q	0.18	1.65	0.18	1.68	0.17	1.25	0.43	1.54
Delay B => Q	0.16	1.64	0.23	1.73	0.16	1.21	0.38	1.50
Delay C => Q	0.12	1.60	0.26	1.79	0.13	1.16	0.30	1.46
Delay D => Q	0.07	1.54	0.25	1.81	0.09	1.12	0.19	1.42
Slew A => Q	0.31	4.03	0.67	4.04	0.34	2.69	0.77	2.71
Slew B => Q	0.31	3.99	0.68	4.04	0.27	2.59	0.66	2.63
Slew C => Q	0.31	4.01	0.67	4.04	0.19	2.51	0.54	2.55
Slew D => Q	0.26	4.03	0.57	4.02	0.10	2.46	0.38	2.48

OAI210 is an OR / NAND circuit with 0.5x drive strength providing the logical function Q = NOT [(A+B).C].

Truth Table

A	B	C	Q
0	0	X	1
X	X	0	1
X	1	1	0
1	X	1	0



Capacitance

Pin	Cap [pF]
A	0.006
B	0.005
C	0.004

Area

0.113 mils^2
73 µm^2

Power

0.25 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

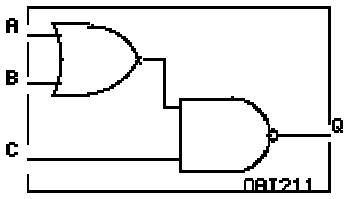
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**
Delay A => Q	0.14	1.75	0.40	1.96	0.07	0.91	0.00	1.00
Delay B => Q	0.12	1.73	0.47	2.06	0.06	0.89	-0.06	0.99
Delay C => Q	0.09	1.91	0.47	2.30	0.06	0.90	-0.01	1.13
Slew A => Q	0.25	4.31	0.55	4.29	0.11	2.09	0.53	2.16
Slew B => Q	0.25	4.30	0.49	4.29	0.07	2.06	0.42	2.12
Slew C => Q	0.25	4.83	0.54	4.83	0.11	2.09	0.46	2.23

OAI211 is an OR / NAND circuit with 1x drive strength providing the logical function Q = NOT [(A+B).C].

Truth Table

A	B	C	Q
0	0	X	1
X	X	0	1
X	1	1	0
1	X	1	0



Capacitance

Pin	Cap [pF]
A	0.010
B	0.009
C	0.005

Area

0.113 mils^2
73 µm^2

Power

0.49 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

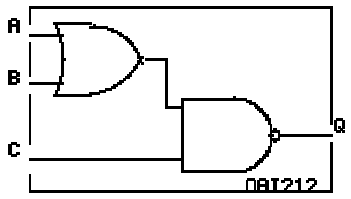
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay A => Q	0.12	1.68	0.38	1.88	0.07	0.89	-0.01	0.98
Delay B => Q	0.10	1.66	0.45	1.99	0.05	0.87	-0.07	0.97
Delay C => Q	0.07	1.74	0.43	2.10	0.05	0.87	-0.02	1.11
Slew A => Q	0.22	4.13	0.52	4.13	0.10	2.03	0.52	2.10
Slew B => Q	0.22	4.14	0.46	4.12	0.06	1.99	0.40	2.07
Slew C => Q	0.21	4.42	0.51	4.36	0.10	2.02	0.44	2.17

OAI212 is an OR / NAND circuit with 2x drive strength providing the logical function Q = NOT [(A+B).C].

Truth Table

A	B	C	Q
0	0	X	1
X	X	0	1
X	1	1	0
1	X	1	0



Capacitance

Pin	Cap [pF]
A	0.017
B	0.016
C	0.008

Area

0.113 mils^2
73 µm^2

Power

0.98 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

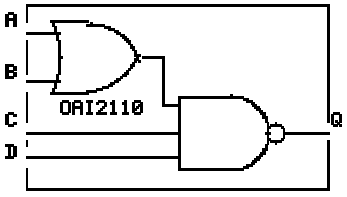
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**
Delay A => Q	0.12	1.65	0.35	1.84	0.07	0.90	0.01	1.02
Delay B => Q	0.10	1.63	0.43	1.96	0.06	0.89	-0.05	1.00
Delay C => Q	0.07	1.66	0.42	2.02	0.05	0.89	-0.01	1.13
Slew A => Q	0.21	4.07	0.53	4.08	0.10	2.07	0.52	2.15
Slew B => Q	0.22	4.09	0.46	4.06	0.07	2.04	0.41	2.12
Slew C => Q	0.20	4.26	0.51	4.16	0.10	2.08	0.44	2.22

OAI2110 is an OR / NAND circuit with 0.5x drive strength providing the logical function Q = NOT [(A+B).C.D].

Truth Table

A	B	C	D	Q
0	0	X	X	1
X	X	0	X	1
X	X	X	0	1
X	1	1	1	0
1	X	1	1	0



Capacitance

Pin	Cap [pF]
A	0.005
B	0.005
C	0.004
D	0.005

Area

0.141 mils^2
91 µm^2

Power

0.26 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

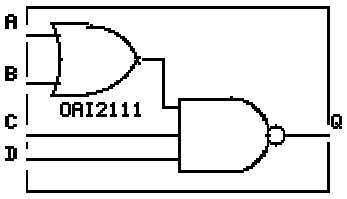
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**
Delay A => Q	0.13	1.74	0.38	1.96	0.06	0.82	0.04	1.04
Delay B => Q	0.11	1.74	0.45	2.06	0.05	0.81	-0.03	1.03
Delay C => Q	0.24	2.06	0.69	2.44	0.09	0.85	-0.03	0.95
Delay D => Q	0.27	2.09	0.75	2.48	0.10	0.86	-0.08	0.83
Slew A => Q	0.23	4.30	0.51	4.27	0.15	1.98	0.59	2.12
Slew B => Q	0.23	4.28	0.46	4.30	0.11	1.95	0.44	2.08
Slew C => Q	0.49	5.00	0.71	5.00	0.16	1.99	0.56	2.09
Slew D => Q	0.58	5.08	0.76	5.08	0.15	1.98	0.50	2.06

OAI2111 is an OR / NAND circuit with 1x drive strength providing the logical function Q = NOT [(A+B).C.D].

Truth Table

A	B	C	D	Q
0	0	X	X	1
X	X	0	X	1
X	X	X	0	1
X	1	1	1	0
1	X	1	1	0



Capacitance

Pin	Cap [pF]
A	0.008
B	0.008
C	0.006
D	0.009

Area

0.141 mils^2
91 µm^2

Power

0.48 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

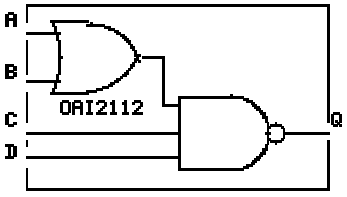
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay A => Q	0.10	1.67	0.33	1.87	0.06	0.82	0.03	1.04
Delay B => Q	0.09	1.65	0.41	1.98	0.04	0.80	-0.04	1.03
Delay C => Q	0.18	1.84	0.61	2.23	0.08	0.84	-0.05	0.94
Delay D => Q	0.21	1.89	0.67	2.25	0.08	0.84	-0.10	0.82
Slew A => Q	0.18	4.10	0.48	4.10	0.13	1.97	0.56	2.10
Slew B => Q	0.18	4.12	0.42	4.11	0.09	1.93	0.41	2.07
Slew C => Q	0.38	4.53	0.61	4.54	0.13	1.96	0.53	2.08
Slew D => Q	0.45	4.60	0.66	4.60	0.13	1.96	0.49	2.04

OAI2112 is an OR / NAND circuit with 2x drive strength providing the logical function Q = NOT [(A+B).C.D].

Truth Table

A	B	C	D	Q
0	0	X	X	1
X	X	0	X	1
X	X	X	0	1
X	1	1	1	0
1	X	1	1	0



Capacitance

Pin	Cap [pF]
A	0.015
B	0.015
C	0.011
D	0.017

Area

0.226 mils^2
146 µm^2

Power

0.9 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

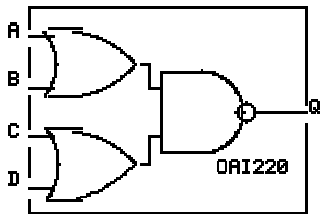
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**
Delay A => Q	0.09	1.66	0.31	1.86	0.05	0.80	0.01	1.03
Delay B => Q	0.07	1.64	0.38	1.97	0.04	0.79	-0.08	1.01
Delay C => Q	0.16	1.77	0.57	2.15	0.07	0.82	-0.07	0.92
Delay D => Q	0.18	1.80	0.63	2.16	0.07	0.82	-0.12	0.80
Slew A => Q	0.14	4.06	0.43	4.06	0.11	1.92	0.52	2.06
Slew B => Q	0.14	4.04	0.37	4.07	0.07	1.89	0.37	2.04
Slew C => Q	0.32	4.35	0.56	4.35	0.11	1.93	0.51	2.05
Slew D => Q	0.39	4.41	0.60	4.41	0.11	1.92	0.47	2.00

OAI220 is an OR / NAND circuit with 0.5x drive strength providing the logical function Q = NOT [(A+B).(C+D)].

Truth Table

A	B	C	D	Q
0	0	X	X	1
X	X	0	0	1
X	1	X	1	0
X	1	1	X	0
1	X	X	1	0
1	X	1	X	0



Capacitance

Pin	Cap [pF]
A	0.004
B	0.004
C	0.005
D	0.005

Area

0.141 mils^2
91 µm^2

Power

0.21 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

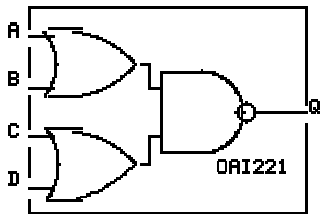
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**
Delay A => Q	0.09	1.71	0.41	2.04	0.06	0.90	0.05	1.15
Delay B => Q	0.11	1.72	0.33	1.93	0.08	0.92	0.12	1.16
Delay C => Q	0.17	1.79	0.55	2.12	0.09	0.93	0.01	1.02
Delay D => Q	0.18	1.81	0.47	2.02	0.10	0.94	0.07	1.04
Slew A => Q	0.26	4.31	0.55	4.30	0.12	2.09	0.45	2.21
Slew B => Q	0.26	4.32	0.59	4.34	0.15	2.13	0.56	2.23
Slew C => Q	0.40	4.43	0.66	4.43	0.12	2.10	0.50	2.17
Slew D => Q	0.40	4.44	0.69	4.44	0.15	2.14	0.57	2.20

OAI221 is an OR / NAND circuit with 1x drive strength providing the logical function Q = NOT [(A+B).(C+D)].

Truth Table

A	B	C	D	Q
0	0	X	X	1
X	X	0	0	1
X	1	X	1	0
X	1	1	X	0
1	X	X	1	0
1	X	1	X	0



Capacitance

Pin	Cap [pF]
A	0.007
B	0.007
C	0.009
D	0.009

Area

0.141 mils^2
91 µm^2

Power

0.4 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

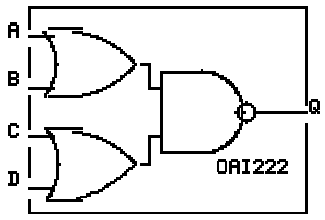
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay A => Q	0.08	1.63	0.38	1.96	0.06	0.88	0.03	1.12
Delay B => Q	0.09	1.65	0.31	1.85	0.07	0.90	0.11	1.14
Delay C => Q	0.14	1.69	0.51	2.03	0.08	0.90	-0.01	1.00
Delay D => Q	0.16	1.71	0.43	1.93	0.09	0.91	0.05	1.01
Slew A => Q	0.23	4.13	0.53	4.13	0.10	2.03	0.43	2.15
Slew B => Q	0.23	4.16	0.57	4.17	0.14	2.07	0.54	2.18
Slew C => Q	0.34	4.24	0.61	4.24	0.10	2.03	0.47	2.11
Slew D => Q	0.35	4.25	0.66	4.26	0.14	2.06	0.56	2.13

OAI222 is an OR / NAND circuit with 2x drive strength providing the logical function Q = NOT [(A+B).(C+D)].

Truth Table

A	B	C	D	Q
0	0	X	X	1
X	X	0	0	1
X	1	X	1	0
X	1	1	X	0
1	X	X	1	0
1	X	1	X	0



Capacitance

Pin	Cap [pF]
A	0.013
B	0.013
C	0.018
D	0.016

Area

0.141 mils^2
91 µm^2

Power

0.76 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

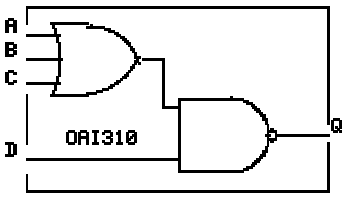
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**
Delay A => Q	0.07	1.60	0.36	1.94	0.06	0.90	0.03	1.14
Delay B => Q	0.08	1.62	0.27	1.81	0.07	0.96	0.13	1.21
Delay C => Q	0.12	1.68	0.46	2.00	0.07	0.96	-0.01	1.05
Delay D => Q	0.14	1.70	0.39	1.91	0.09	0.98	0.05	1.08
Slew A => Q	0.21	4.09	0.52	4.11	0.09	2.08	0.41	2.20
Slew B => Q	0.21	4.08	0.58	4.11	0.14	2.23	0.53	2.31
Slew C => Q	0.30	4.22	0.57	4.20	0.10	2.17	0.45	2.24
Slew D => Q	0.30	4.22	0.62	4.23	0.13	2.23	0.56	2.29

OAI310 is an OR / NAND circuit with 0.5x drive strength providing the logical function Q = NOT [(A+B+C).D].

Truth Table

A	B	C	D	Q
0	0	0	X	1
X	X	X	0	1
X	X	1	1	0
X	1	X	1	0
1	X	X	1	0



Capacitance

Pin	Cap [pF]
A	0.006
B	0.006
C	0.007
D	0.004

Area

0.141 mils^2
91 µm^2

Power

0.33 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

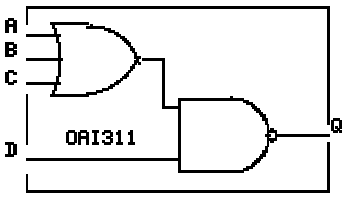
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**
Delay A => Q	0.19	1.75	0.37	1.86	0.11	0.97	0.11	1.06
Delay B => Q	0.17	1.74	0.44	1.95	0.10	0.94	0.07	1.04
Delay C => Q	0.13	1.70	0.47	2.00	0.08	0.92	-0.00	1.01
Delay D => Q	0.12	1.95	0.53	2.34	0.09	0.94	0.10	1.18
Slew A => Q	0.34	4.26	0.68	4.26	0.20	2.18	0.64	2.25
Slew B => Q	0.34	4.26	0.62	4.26	0.15	2.12	0.55	2.20
Slew C => Q	0.34	4.26	0.58	4.26	0.09	2.08	0.42	2.13
Slew D => Q	0.48	4.99	0.81	5.06	0.20	2.18	0.56	2.31

OAI311 is an OR / NAND circuit with 1x drive strength providing the logical function Q = NOT [(A+B+C).D].

Truth Table

A	B	C	D	Q
0	0	0	X	1
X	X	X	0	1
X	X	1	1	0
X	1	X	1	0
1	X	X	1	0



Capacitance

Pin	Cap [pF]
A	0.012
B	0.012
C	0.011
D	0.005

Area

0.141 mils^2
91 µm^2

Power

0.62 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

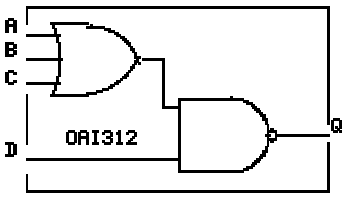
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay A => Q	0.17	1.70	0.34	1.80	0.10	0.94	0.09	1.03
Delay B => Q	0.15	1.68	0.41	1.89	0.09	0.91	0.05	1.01
Delay C => Q	0.11	1.64	0.44	1.95	0.07	0.88	-0.03	0.99
Delay D => Q	0.09	1.76	0.48	2.14	0.08	0.92	0.09	1.15
Slew A => Q	0.29	4.13	0.64	4.14	0.17	2.11	0.62	2.19
Slew B => Q	0.29	4.13	0.58	4.14	0.12	2.06	0.51	2.13
Slew C => Q	0.28	4.13	0.52	4.11	0.07	2.01	0.40	2.08
Slew D => Q	0.41	4.61	0.76	4.58	0.17	2.12	0.54	2.25

OAI312 is an OR / NAND circuit with 2x drive strength providing the logical function Q = NOT [(A+B+C).D].

Truth Table

A	B	C	D	Q
0	0	0	X	1
X	X	X	0	1
X	X	1	1	0
X	1	X	1	0
1	X	X	1	0



Capacitance

Pin	Cap [pF]
A	0.023
B	0.022
C	0.022
D	0.009

Area

0.169 mils^2
109 µm^2

Power

1.18 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

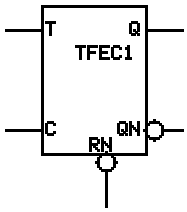
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**
Delay A => Q	0.15	1.72	0.33	1.83	0.09	0.92	0.07	1.02
Delay B => Q	0.14	1.70	0.39	1.91	0.08	0.90	0.02	1.00
Delay C => Q	0.09	1.66	0.42	1.97	0.05	0.86	-0.06	0.97
Delay D => Q	0.07	1.67	0.45	2.05	0.07	0.91	0.08	1.14
Slew A => Q	0.26	4.19	0.61	4.21	0.16	2.08	0.60	2.17
Slew B => Q	0.26	4.19	0.54	4.21	0.11	2.03	0.51	2.11
Slew C => Q	0.24	4.19	0.47	4.19	0.06	1.98	0.37	2.05
Slew D => Q	0.37	4.40	0.73	4.38	0.15	2.09	0.52	2.23

TFEC1 is a Toggle flip-flop with 1x drive strength and active high toggle enable. CLEAR is asynchronous and active low.

Truth Table

C	RN	T	Q	QN
↑	1	1	~Q	~QN
X	0	X	0	1



Capacitance

Pin	Cap [pF]
C	0.004
RN	0.011
T	0.006

Area

0.536 mils^2
346 µm^2

Power

1.41 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay C => Q	0.49	2.14	0.66	2.31	0.60	1.69	0.76	1.85
Delay C => QN	0.78	2.43	0.94	2.59	0.64	1.74	0.81	1.91
Delay RN => Q	n.a.	n.a.	n.a.	n.a.	0.26	1.39	0.68	1.82
Delay RN => QN	0.48	2.12	0.91	2.55	n.a.	n.a.	n.a.	n.a.
Slew C => Q	0.11	4.23	0.12	4.25	0.10	2.39	0.10	2.39
Slew C => QN	0.13	4.22	0.13	4.23	0.10	2.37	0.10	2.37
Slew RN => Q	n.a.	n.a.	n.a.	n.a.	0.14	2.39	0.18	2.38
Slew RN => QN	0.17	4.25	0.17	4.25	n.a.	n.a.	n.a.	n.a.

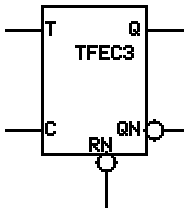
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
RN => C	0	n.a.	0.465	n.a.
T => C	0.108	0	0	0

	Min Width	
	High	**Low**
C	0.376	0.326
RN	n.a.	0.360

TFEC3 is a Toggle flip-flop with 3x drive strength and active high toggle enable. CLEAR is asynchronous and active low.

Truth Table

C	RN	T	Q	QN
↑	1	1	~Q	~QN
X	0	X	0	1



Capacitance

Pin	Cap [pF]
C	0.004
RN	0.011
T	0.006

Area

0.536 mils^2
346 µm^2

Power

1.86 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay C => Q	0.50	2.06	0.68	2.23	0.64	1.71	0.80	1.87
Delay C => QN	0.88	2.42	1.03	2.58	0.72	1.80	0.90	1.97
Delay RN => Q	n.a.	n.a.	n.a.	n.a.	0.30	1.43	0.72	1.85
Delay RN => QN	0.58	2.13	1.01	2.55	n.a.	n.a.	n.a.	n.a.
Slew C => Q	0.10	4.00	0.10	4.04	0.11	2.31	0.11	2.31
Slew C => QN	0.12	4.01	0.12	4.02	0.11	2.32	0.11	2.32
Slew RN => Q	n.a.	n.a.	n.a.	n.a.	0.15	2.32	0.18	2.31
Slew RN => QN	0.17	4.03	0.15	4.01	n.a.	n.a.	n.a.	n.a.

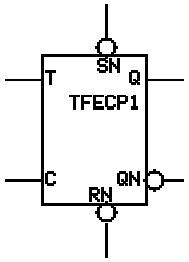
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
RN => C	0	n.a.	0.466	n.a.
T => C	0.105	0	0	0

	Min Width	
	High	**Low**
C	0.376	0.326
RN	n.a.	0.360

TFECP1 is a Toggle flip-flop with 1x drive strength and active high toggle enable. PRESET and CLEAR are asynchronous and active low.

Truth Table

C	RN	SN	T	Q	QN
↑	1	1	1	~Q	~QN
X	0	0	X	0	0
X	0	1	X	0	1
X	1	0	X	1	0



Capacitance

Pin	Cap [pF]
C	0.004
RN	0.015
SN	0.014
T	0.005

Area

0.564 mils^2
364 µm^2

Power

1.46 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay C => Q	0.50	2.15	0.68	2.33	0.62	1.70	0.77	1.86
Delay C => QN	0.74	2.39	0.90	2.55	0.69	1.79	0.88	1.98
Delay RN => Q	0.17	1.87	0.28	1.96	0.28	1.44	0.70	1.87
Delay RN => QN	0.42	2.07	0.84	2.49	n.a.	n.a.	n.a.	n.a.
Delay SN => Q	0.47	2.11	0.88	2.52	n.a.	n.a.	n.a.	n.a.
Delay SN => QN	0.20	1.91	0.33	2.02	0.31	1.51	0.73	1.93
Slew C => Q	0.12	4.26	0.11	4.25	0.11	2.39	0.11	2.39
Slew C => QN	0.13	4.24	0.12	4.24	0.12	2.39	0.11	2.39
Slew RN => Q	0.14	4.28	0.19	4.30	0.14	2.42	0.18	2.41
Slew RN => QN	0.17	4.25	0.17	4.25	n.a.	n.a.	n.a.	n.a.
Slew SN => Q	0.15	4.25	0.15	4.24	n.a.	n.a.	n.a.	n.a.
Slew SN => QN	0.17	4.29	0.19	4.31	0.16	2.44	0.19	2.45

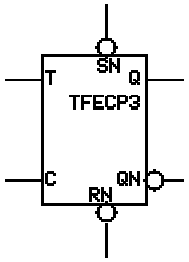
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
RN => C	0	n.a.	0.457	n.a.
SN => C	0	n.a.	0.291	n.a.
T => C	0.14	0	0	0

	Min Width	
	High	**Low**
C	0.376	0.326
RN	n.a.	0.360
SN	n.a.	0.380

TFECP3 is a Toggle flip-flop with 3x drive strength and active high toggle enable. PRESET and CLEAR are asynchronous and active low.

Truth Table

C	RN	SN	T	Q	QN
↑	1	1	1	~Q	~QN
X	0	0	X	0	0
X	0	1	X	0	1
X	1	0	X	1	0



Capacitance

Pin	Cap [pF]
C	0.004
RN	0.015
SN	0.014
T	0.005

Area

0.564 mils^2
364 µm^2

Power

2.07 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay C => Q	0.52	2.08	0.70	2.26	0.65	1.72	0.81	1.89
Delay C => QN	0.81	2.36	0.97	2.53	0.77	1.86	0.95	2.04
Delay RN => Q	0.19	1.80	0.31	1.91	0.31	1.48	0.74	1.91
Delay RN => QN	0.49	2.05	0.92	2.47	n.a.	n.a.	n.a.	n.a.
Delay SN => Q	0.55	2.10	0.97	2.52	n.a.	n.a.	n.a.	n.a.
Delay SN => QN	0.21	1.83	0.36	1.96	0.35	1.54	0.78	1.98
Slew C => Q	0.11	4.02	0.10	4.01	0.12	2.31	0.11	2.31
Slew C => QN	0.11	4.03	0.12	4.01	0.12	2.30	0.12	2.32
Slew RN => Q	0.13	4.08	0.17	4.08	0.15	2.35	0.18	2.36
Slew RN => QN	0.15	4.01	0.15	4.01	n.a.	n.a.	n.a.	n.a.
Slew SN => Q	0.14	4.02	0.14	4.02	n.a.	n.a.	n.a.	n.a.
Slew SN => QN	0.15	4.03	0.18	4.08	0.16	2.38	0.19	2.38

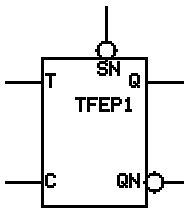
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
RN => C	0	n.a.	0.457	n.a.
SN => C	0	n.a.	0.291	n.a.
T => C	0.138	0	0	0

	Min Width	
	High	**Low**
C	0.376	0.326
RN	n.a.	0.360
SN	n.a.	0.380

TFEP1 is a Toggle flip-flop with 1x drive strength and active high toggle enable. PRESET is asynchronous and active low.

Truth Table

C	SN	T	Q	QN
↑	1	1	~Q	~QN
X	0	X	1	0



Capacitance

Pin	Cap [pF]
C	0.004
SN	0.010
T	0.005

Area

0.536 mils^2
346 µm^2

Power

1.29 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay C => Q	0.52	2.16	0.70	2.34	0.56	1.63	0.72	1.80
Delay C => QN	0.68	2.33	0.84	2.50	0.71	1.81	0.89	1.99
Delay SN => Q	0.53	2.18	0.96	2.59	n.a.	n.a.	n.a.	n.a.
Delay SN => QN	n.a.	n.a.	n.a.	n.a.	0.30	1.45	0.72	1.87
Slew C => Q	0.12	4.24	0.12	4.24	0.10	2.37	0.10	2.39
Slew C => QN	0.12	4.24	0.12	4.24	0.12	2.39	0.12	2.37
Slew SN => Q	0.16	4.25	0.16	4.24	n.a.	n.a.	n.a.	n.a.
Slew SN => QN	n.a.	n.a.	n.a.	n.a.	0.16	2.39	0.19	2.39

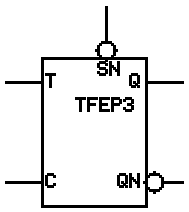
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
SN => C	0	n.a.	0.328	n.a.
T => C	0.122	0	0	0

	Min Width	
	High	**Low**
C	0.376	0.326
SN	n.a.	0.380

TFEP3 is a Toggle flip-flop with 3x drive strength and active high toggle enable. PRESET is asynchronous and active low.

Truth Table

C	SN	T	Q	QN
↑	1	1	~Q	~QN
X	0	X	1	0



Capacitance

Pin	Cap [pF]
C	0.004
SN	0.010
T	0.005

Area

0.536 mils^2
346 µm^2

Power

1.88 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay C => Q	0.55	2.10	0.73	2.28	0.60	1.66	0.76	1.83
Delay C => QN	0.75	2.31	0.91	2.47	0.80	1.89	0.97	2.06
Delay SN => Q	0.64	2.18	1.07	2.60	n.a.	n.a.	n.a.	n.a.
Delay SN => QN	n.a.	n.a.	n.a.	n.a.	0.34	1.48	0.77	1.91
Slew C => Q	0.10	4.01	0.11	4.03	0.11	2.31	0.11	2.30
Slew C => QN	0.11	4.01	0.11	4.01	0.12	2.31	0.12	2.31
Slew SN => Q	0.15	4.02	0.15	4.02	n.a.	n.a.	n.a.	n.a.
Slew SN => QN	n.a.	n.a.	n.a.	n.a.	0.15	2.31	0.19	2.32

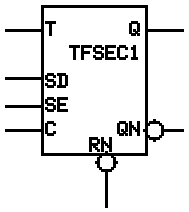
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
SN => C	0	n.a.	0.328	n.a.
T => C	0.121	0	0	0

	Min Width	
	High	**Low**
C	0.376	0.326
SN	n.a.	0.380

TFSEC1 is a Scan Toggle flip-flop with 1x drive strength and active high toggle enable. SCAN ENABLE switches between normal DATA input and SCAN DATA input. CLEAR is asynchronous and active low.

Truth Table

C	RN	SD	SE	T	Q	QN
↑	1	0	1	X	0	1
↑	1	X	0	1	~Q	~QN
↑	1	1	1	X	1	0
X	0	X	X	X	0	1



Capacitance

Pin	Cap [pF]
C	0.004
RN	0.011
SD	0.010
SE	0.006
T	0.006

Area

0.677 mils^2
437 µm^2

Power

1.51 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay C => Q	0.52	2.23	0.68	2.40	0.70	1.82	0.94	2.05
Delay C => QN	0.87	2.55	1.04	2.73	0.70	1.86	0.88	2.01
Delay RN => Q	n.a.	n.a.	n.a.	n.a.	0.29	1.45	0.72	1.88
Delay RN => QN	0.52	2.17	0.95	2.60	n.a.	n.a.	n.a.	n.a.
Slew C => Q	0.13	4.25	0.13	4.25	0.13	2.39	0.13	2.39
Slew C => QN	0.15	4.25	0.15	4.24	0.13	2.42	0.12	2.42
Slew RN => Q	n.a.	n.a.	n.a.	n.a.	0.16	2.44	0.18	2.46
Slew RN => QN	0.18	4.29	0.18	4.31	n.a.	n.a.	n.a.	n.a.

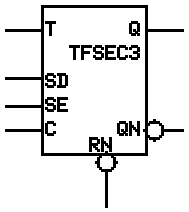
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
RN => C	0	n.a.	0.495	n.a.
SD => C	0.033	0.093	0	0
SE => C	0	0.385	0	0
T => C	0	0.002	0	0

	Min Width	
	High	**Low**
C	0.376	0.326
RN	n.a.	0.360

TFSEC3 is a Scan Toggle flip-flop with 3x drive strength and active high toggle enable. SCAN ENABLE switches between normal DATA input and SCAN DATA input. CLEAR is asynchronous and active low.

Truth Table

C	RN	SD	SE	T	Q	QN
↑	1	0	1	X	0	1
↑	1	X	0	1	~Q	~QN
↑	1	1	1	X	1	0
X	0	X	X	X	0	1



Capacitance

Pin	Cap [pF]
C	0.004
RN	0.011
SD	0.010
SE	0.006
T	0.006

Area

0.677 mils^2
437 µm^2

Power

2.08 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay C => Q	0.60	2.16	0.77	2.29	0.73	1.88	0.94	2.03
Delay C => QN	0.96	2.54	1.14	2.74	0.80	1.96	0.98	2.09
Delay RN => Q	n.a.	n.a.	n.a.	n.a.	0.33	1.49	0.78	1.94
Delay RN => QN	0.62	2.17	1.08	2.60	n.a.	n.a.	n.a.	n.a.
Slew C => Q	0.12	4.04	0.12	4.03	0.14	2.32	0.13	2.32
Slew C => QN	0.14	4.01	0.14	4.02	0.13	2.35	0.14	2.35
Slew RN => Q	n.a.	n.a.	n.a.	n.a.	0.16	2.34	0.20	2.35
Slew RN => QN	0.17	4.09	0.17	4.02	n.a.	n.a.	n.a.	n.a.

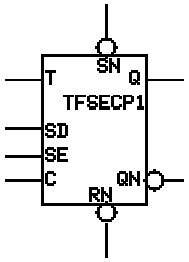
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
RN => C	0	n.a.	0.495	n.a.
SD => C	0	0.094	0	0
SE => C	0.16	0.384	0	0
T => C	0	0.002	0	0

	Min Width	
	High	**Low**
C	0.376	0.326
RN	n.a.	0.360

TFSECP1 is a Scan Toggle flip-flop with 1x drive strength and active high toggle enable. SCAN ENABLE switches between normal DATA input and SCAN DATA input. CLEAR and PRESET are asynchronous and active low.

Truth Table

C	RN	SD	SE	SN	T	Q	QN
↑	1	0	1	1	X	0	1
↑	1	X	0	1	1	~Q	~QN
↑	1	1	1	1	X	1	0
X	0	X	X	0	X	0	0
X	0	X	X	1	X	0	1
X	1	X	X	0	X	1	0



Capacitance

Pin	Cap [pF]
C	0.004
RN	0.015
SD	0.010
SE	0.006
SN	0.014
T	0.005

Area

0.705 mils^2
455 µm^2

Power

1.52 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay C => Q	0.60	2.22	0.73	2.40	0.70	1.83	0.94	2.08
Delay C => QN	0.80	2.50	1.04	2.72	0.79	1.94	0.94	2.05
Delay RN => Q	0.20	1.89	0.30	2.02	0.30	1.51	0.73	1.92
Delay RN => QN	0.41	2.11	0.91	2.55	n.a.	n.a.	n.a.	n.a.
Delay SN => Q	0.50	2.15	0.89	2.59	n.a.	n.a.	n.a.	n.a.
Delay SN => QN	0.20	1.94	0.36	2.06	0.32	1.58	0.77	1.98
Slew C => Q	0.14	4.25	0.13	4.26	0.13	2.40	0.13	2.38
Slew C => QN	0.14	4.25	0.14	4.25	0.14	2.44	0.14	2.43
Slew RN => Q	0.14	4.31	0.20	4.30	0.17	2.48	0.25	2.48
Slew RN => QN	0.17	4.30	0.17	4.32	n.a.	n.a.	n.a.	n.a.
Slew SN => Q	0.17	4.29	0.17	4.33	n.a.	n.a.	n.a.	n.a.
Slew SN => QN	0.18	4.31	0.21	4.31	0.18	2.51	0.21	2.50

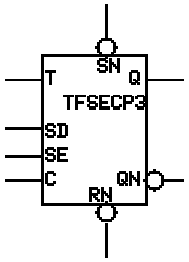
	Setup		Hold	
	rise	fall	rise	fall
RN => C	0	n.a.	0.485	n.a.
SD => C	0	0.043	0	0
SE => C	0	0.441	0	0
SN => C	0	n.a.	0.342	n.a.
T => C	0	0.002	0	0

	Min Width	
	High	Low
C	0.376	0.326
RN	n.a.	0.360
SN	n.a.	0.380

TFSECP3 is a Scan Toggle flip-flop with 3x drive strength and active high toggle enable. SCAN ENABLE switches between normal DATA input and SCAN DATA input. CLEAR and PRESET are asynchronous and active low.

Truth Table

C	RN	SD	SE	SN	T	Q	QN
↑	1	0	1	1	X	0	1
↑	1	X	0	1	1	~Q	~QN
↑	1	1	1	1	X	1	0
X	0	X	X	0	X	0	0
X	0	X	X	1	X	0	1
X	1	X	X	0	X	1	0



Capacitance

Pin	Cap [pF]
C	0.004
RN	0.015
SD	0.010
SE	0.006
SN	0.014
T	0.005

Area

0.705 mils^2
455 µm^2

Power

2.15 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay C => Q	0.60	2.16	0.75	2.31	0.75	1.87	0.94	2.08
Delay C => QN	0.90	2.46	1.13	2.69	0.82	1.98	0.95	2.12
Delay RN => Q	0.20	1.87	0.30	1.94	0.34	1.54	0.81	1.97
Delay RN => QN	0.50	2.09	1.00	2.54	n.a.	n.a.	n.a.	n.a.
Delay SN => Q	0.60	2.16	1.01	2.56	n.a.	n.a.	n.a.	n.a.
Delay SN => QN	0.20	1.87	0.39	1.99	0.40	1.60	0.81	2.04
Slew C => Q	0.13	4.03	0.12	4.04	0.14	2.32	0.13	2.32
Slew C => QN	0.13	4.02	0.13	4.02	0.14	2.36	0.15	2.35
Slew RN => Q	0.14	4.10	0.20	4.09	0.18	2.42	0.20	2.41
Slew RN => QN	0.17	4.04	0.17	4.09	n.a.	n.a.	n.a.	n.a.
Slew SN => Q	0.17	4.07	0.17	4.11	n.a.	n.a.	n.a.	n.a.
Slew SN => QN	0.17	4.08	0.19	4.07	0.18	2.43	0.33	2.44

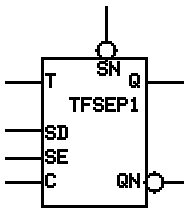
	Setup		Hold	
	rise	fall	rise	fall
RN => C	0	n.a.	0.485	n.a.
SD => C	0	0.053	0	0
SE => C	0	0.439	0	0
SN => C	0	n.a.	0.342	n.a.
T => C	0	0.002	0	0

	Min Width	
	High	Low
C	0.376	0.326
RN	n.a.	0.360
SN	n.a.	0.380

TFSEP1 is a Scan Toggle flip-flop with 1x drive strength and active high toggle enable. SCAN ENABLE switches between normal DATA input and SCAN DATA input. PRESET is asynchronous and active low.

Truth Table

C	SD	SE	SN	T	Q	QN
↑	0	1	1	X	0	1
↑	X	0	1	1	~Q	~QN
↑	1	1	1	X	1	0
X	X	X	0	X	1	0



Capacitance

Pin	Cap [pF]
C	0.004
SD	0.009
SE	0.006
SN	0.010
T	0.005

Area

0.677 mils^2
437 µm^2

Power

1.47 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay C => Q	0.60	2.28	0.75	2.42	0.68	1.77	0.85	2.02
Delay C => QN	0.74	2.45	0.94	2.63	0.80	1.94	0.97	2.13
Delay SN => Q	0.58	2.25	0.98	2.69	n.a.	n.a.	n.a.	n.a.
Delay SN => QN	n.a.	n.a.	n.a.	n.a.	0.31	1.50	0.73	1.93
Slew C => Q	0.14	4.27	0.14	4.26	0.12	2.40	0.12	2.39
Slew C => QN	0.14	4.25	0.14	4.24	0.13	2.43	0.14	2.43
Slew SN => Q	0.26	4.33	0.17	4.30	n.a.	n.a.	n.a.	n.a.
Slew SN => QN	n.a.	n.a.	n.a.	n.a.	0.17	2.46	0.20	2.43

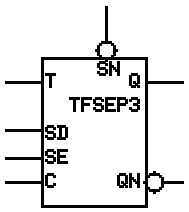
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
SD => C	0	0.046	0	0
SE => C	0.114	0.447	0	0
SN => C	0	n.a.	0.377	n.a.
T => C	0	0.002	0	0

	Min Width	
	High	**Low**
C	0.376	0.326
SN	n.a.	0.380

TFSEP3 is a Scan Toggle flip-flop with 3x drive strength and active high toggle enable. SCAN ENABLE switches between normal DATA input and SCAN DATA input. PRESET is asynchronous and active low.

Truth Table

C	SD	SE	SN	T	Q	QN
↑	0	1	1	X	0	1
↑	X	0	1	1	~Q	~QN
↑	1	1	1	X	1	0
X	X	X	0	X	1	0



Capacitance

Pin	Cap [pF]
C	0.004
SD	0.009
SE	0.006
SN	0.010
T	0.005

Area

0.677 mils^2
437 µm^2

Power

2.2 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay C => Q	0.60	2.21	0.76	2.37	0.70	1.83	0.94	2.00
Delay C => QN	0.80	2.42	1.04	2.64	0.90	1.99	1.06	2.17
Delay SN => Q	0.69	2.23	1.11	2.67	n.a.	n.a.	n.a.	n.a.
Delay SN => QN	n.a.	n.a.	n.a.	n.a.	0.38	1.53	0.80	1.95
Slew C => Q	0.13	4.04	0.13	4.03	0.13	2.32	0.13	2.31
Slew C => QN	0.13	4.01	0.13	4.02	0.15	2.37	0.14	2.35
Slew SN => Q	0.17	4.09	0.17	4.07	n.a.	n.a.	n.a.	n.a.
Slew SN => QN	n.a.	n.a.	n.a.	n.a.	0.17	2.37	0.20	2.35

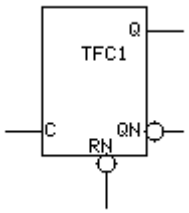
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
SD => C	0.067	0.046	0	0
SE => C	0.114	0.446	0	0
SN => C	0	n.a.	0.377	n.a.
T => C	0	0.002	0	0

	Min Width	
	High	**Low**
C	0.376	0.326
SN	n.a.	0.380

TFC1 is a Toggle flip-flop with 1x drive strength. CLEAR is asynchronous and active low.

Truth Table

C	RN	Q	QN
↑	1	~Q	~QN
X	0	0	1



Capacitance

Pin	Cap [pF]
C	0.004
RN	0.013

Area

0.451 mils^2
291 µm^2

Power

1.27 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay C => Q	0.47	2.11	0.64	2.29	0.58	1.65	0.74	1.81
Delay C => QN	0.71	2.35	0.87	2.50	0.58	1.64	0.75	1.81
Delay RN => Q	n.a.	n.a.	n.a.	n.a.	0.16	1.22	0.53	1.61
Delay RN => QN	0.38	2.04	0.77	2.43	n.a.	n.a.	n.a.	n.a.
Slew C => Q	0.11	4.24	0.11	4.24	0.09	2.38	0.09	2.39
Slew C => QN	0.11	4.24	0.11	4.23	0.08	2.39	0.08	2.39
Slew RN => Q	n.a.	n.a.	n.a.	n.a.	0.08	2.38	0.12	2.38
Slew RN => QN	0.15	4.23	0.15	4.25	n.a.	n.a.	n.a.	n.a.

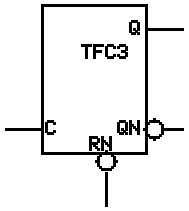
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
RN => C	0	n.a.	0.464	n.a.

	Min Width	
	High	**Low**
C	0.376	0.326
RN	n.a.	0.360

TFC3 is a Toggle flip-flop with 3x drive strength. CLEAR is asynchronous and active low.

Truth Table

C	RN	Q	QN
↑	1	~Q	~QN
X	0	0	1



Capacitance

Pin	Cap [pF]
C	0.004
RN	0.013

Area

0.451 mils^2
291 µm^2

Power

1.92 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay C => Q	0.49	2.05	0.67	2.22	0.62	1.69	0.78	1.84
Delay C => QN	0.81	2.34	0.97	2.50	0.66	1.71	0.83	1.88
Delay RN => Q	n.a.	n.a.	n.a.	n.a.	0.20	1.25	0.60	1.65
Delay RN => QN	0.48	2.05	0.89	2.45	n.a.	n.a.	n.a.	n.a.
Slew C => Q	0.10	4.03	0.10	4.03	0.11	2.31	0.11	2.30
Slew C => QN	0.10	4.01	0.10	4.01	0.09	2.30	0.09	2.30
Slew RN => Q	n.a.	n.a.	n.a.	n.a.	0.10	2.30	0.14	2.30
Slew RN => QN	0.14	4.02	0.14	4.02	n.a.	n.a.	n.a.	n.a.

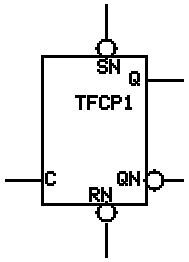
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
RN => C	0	n.a.	0.465	n.a.

	Min Width	
	High	**Low**
C	0.376	0.326
RN	n.a.	0.360

TFCP1 is a Toggle flip-flop with 1x drive strength. PRESET and CLEAR are asynchronous and active low.

Truth Table

C	RN	SN	Q	QN
↑	1	1	~Q	~QN
X	0	0	0	0
X	0	1	0	1
X	1	0	1	0



Capacitance

Pin	Cap [pF]
C	0.004
RN	0.015
SN	0.012

Area

0.48 mils^2
310 µm^2

Power

1.27 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay C => Q	0.48	2.13	0.66	2.31	0.59	1.67	0.75	1.83
Delay C => QN	0.69	2.33	0.85	2.49	0.63	1.70	0.81	1.87
Delay RN => Q	0.12	1.78	0.11	1.76	0.17	1.23	0.54	1.62
Delay RN => QN	0.34	2.01	0.72	2.38	n.a.	n.a.	n.a.	n.a.
Delay SN => Q	0.42	2.06	0.82	2.46	n.a.	n.a.	n.a.	n.a.
Delay SN => QN	0.19	1.87	0.29	1.96	0.28	1.44	0.69	1.85
Slew C => Q	0.11	4.25	0.11	4.24	0.10	2.39	0.10	2.39
Slew C => QN	0.11	4.23	0.11	4.24	0.09	2.39	0.10	2.39
Slew RN => Q	0.10	4.30	0.14	4.29	0.09	2.38	0.13	2.39
Slew RN => QN	0.15	4.24	0.15	4.24	n.a.	n.a.	n.a.	n.a.
Slew SN => Q	0.12	4.24	0.12	4.24	n.a.	n.a.	n.a.	n.a.
Slew SN => QN	0.15	4.29	0.18	4.27	0.14	2.41	0.18	2.40

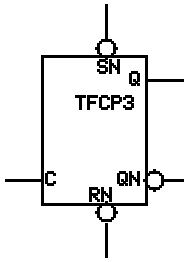
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
RN => C	0	n.a.	0.455	n.a.
SN => C	0	n.a.	0.297	n.a.

	Min Width	
	High	**Low**
C	0.376	0.326
RN	n.a.	0.360
SN	n.a.	0.380

TFCP3 is a Toggle flip-flop with 3x drive strength. PRESET and CLEAR are asynchronous and active low.

Truth Table

C	RN	SN	Q	QN
↑	1	1	~Q	~QN
X	0	0	0	0
X	0	1	0	1
X	1	0	1	0



Capacitance

Pin	Cap [pF]
C	0.004
RN	0.015
SN	0.012

Area

0.48 mils^2
310 µm^2

Power

1.93 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay C => Q	0.51	2.07	0.69	2.25	0.64	1.70	0.79	1.86
Delay C => QN	0.76	2.30	0.92	2.46	0.71	1.76	0.89	1.94
Delay RN => Q	0.14	1.71	0.17	1.73	0.21	1.27	0.61	1.68
Delay RN => QN	0.42	1.99	0.82	2.38	n.a.	n.a.	n.a.	n.a.
Delay SN => Q	0.50	2.05	0.92	2.46	n.a.	n.a.	n.a.	n.a.
Delay SN => QN	0.20	1.80	0.32	1.90	0.32	1.47	0.74	1.90
Slew C => Q	0.10	4.02	0.10	4.02	0.11	2.31	0.11	2.30
Slew C => QN	0.10	4.01	0.10	4.02	0.10	2.31	0.10	2.31
Slew RN => Q	0.10	4.06	0.14	4.08	0.10	2.30	0.14	2.31
Slew RN => QN	0.14	4.02	0.14	4.01	n.a.	n.a.	n.a.	n.a.
Slew SN => Q	0.11	4.01	0.11	4.01	n.a.	n.a.	n.a.	n.a.
Slew SN => QN	0.14	4.07	0.16	4.07	0.14	2.32	0.18	2.35

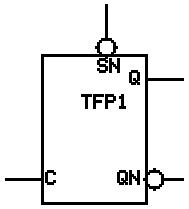
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
RN => C	0	n.a.	0.455	n.a.
SN => C	0	n.a.	0.297	n.a.

	Min Width	
	High	**Low**
C	0.376	0.326
RN	n.a.	0.360
SN	n.a.	0.380

TFP1 is a Toggle flip-flop with 1x drive strength. PRESET is asynchronous and active low.

Truth Table

C	SN	Q	QN
↑	1	~Q	~QN
X	0	1	0



Capacitance

Pin	Cap [pF]
C	0.004
SN	0.012

Area

0.451 mils^2
291 µm^2

Power

1.19 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay C => Q	0.50	2.14	0.68	2.32	0.54	1.60	0.70	1.76
Delay C => QN	0.63	2.27	0.79	2.43	0.65	1.71	0.82	1.89
Delay SN => Q	0.47	2.11	0.88	2.52	n.a.	n.a.	n.a.	n.a.
Delay SN => QN	n.a.	n.a.	n.a.	n.a.	0.27	1.39	0.68	1.80
Slew C => Q	0.11	4.25	0.11	4.25	0.09	2.36	0.09	2.39
Slew C => QN	0.11	4.23	0.11	4.24	0.09	2.38	0.09	2.39
Slew SN => Q	0.12	4.25	0.12	4.25	n.a.	n.a.	n.a.	n.a.
Slew SN => QN	n.a.	n.a.	n.a.	n.a.	0.14	2.37	0.17	2.38

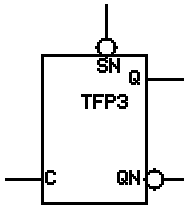
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
SN => C	0	n.a.	0.335	n.a.

	Min Width	
	High	**Low**
C	0.376	0.326
SN	n.a.	0.380

TFP3 is a Toggle flip-flop with 3x drive strength. PRESET is asynchronous and active low.

Truth Table

C	SN	Q	QN
↑	1	~Q	~QN
X	0	1	0



Capacitance

Pin	Cap [pF]
C	0.004
SN	0.012

Area

0.451 mils^2
291 µm^2

Power

1.89 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay C => Q	0.53	2.09	0.71	2.26	0.58	1.64	0.74	1.80
Delay C => QN	0.70	2.25	0.86	2.41	0.73	1.78	0.91	1.96
Delay SN => Q	0.57	2.10	1.00	2.53	n.a.	n.a.	n.a.	n.a.
Delay SN => QN	n.a.	n.a.	n.a.	n.a.	0.31	1.42	0.72	1.84
Slew C => Q	0.10	4.03	0.10	4.03	0.10	2.31	0.10	2.31
Slew C => QN	0.09	4.01	0.10	4.01	0.10	2.31	0.10	2.31
Slew SN => Q	0.12	4.02	0.12	4.02	n.a.	n.a.	n.a.	n.a.
Slew SN => QN	n.a.	n.a.	n.a.	n.a.	0.14	2.30	0.17	2.30

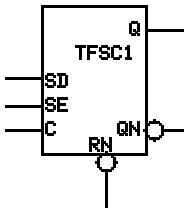
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
SN => C	0	n.a.	0.335	n.a.

	Min Width	
	High	**Low**
C	0.376	0.326
SN	n.a.	0.380

TFSC1 is Scan Toggle flip-flop with 1x drive strength. SCAN ENABLE switches between normal DATA input and SCAN DATA input. CLEAR is asynchronous and active low.

Truth Table

C	RN	SD	SE	Q	QN
↑	1	0	1	0	1
↑	1	X	0	~Q	~QN
↑	1	1	1	1	0
X	0	X	X	0	1



Capacitance

Pin	Cap [pF]
C	0.004
RN	0.013
SD	0.009
SE	0.006

Area

0.536 mils^2
346 µm^2

Power

1.32 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay C => Q	0.48	2.13	0.65	2.30	0.60	1.67	0.76	1.82
Delay C => QN	0.78	2.44	0.94	2.60	0.66	1.77	0.83	1.94
Delay RN => Q	n.a.	n.a.	n.a.	n.a.	0.17	1.24	0.55	1.63
Delay RN => QN	0.43	2.12	0.83	2.52	n.a.	n.a.	n.a.	n.a.
Slew C => Q	0.13	4.25	0.12	4.26	0.10	2.39	0.11	2.39
Slew C => QN	0.13	4.24	0.14	4.25	0.11	2.37	0.12	2.39
Slew RN => Q	n.a.	n.a.	n.a.	n.a.	0.10	2.40	0.14	2.39
Slew RN => QN	0.18	4.25	0.18	4.25	n.a.	n.a.	n.a.	n.a.

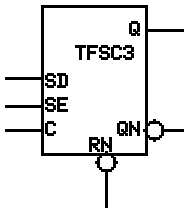
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
RN => C	0	n.a.	0.466	n.a.
SD => C	0.068	0	0	0
SE => C	0	0	0	0

	Min Width	
	High	**Low**
C	0.376	0.326
RN	n.a.	0.360

TFSC3 is Scan Toggle flip-flop with 3x drive strength. SCAN ENABLE switches between normal DATA input and SCAN DATA input. CLEAR is asynchronous and active low.

Truth Table

C	RN	SD	SE	Q	QN
↑	1	0	1	0	1
↑	1	X	0	~Q	~QN
↑	1	1	1	1	0
X	0	X	X	0	1



Capacitance

Pin	Cap [pF]
C	0.004
RN	0.013
SD	0.009
SE	0.006

Area

0.564 mils^2
364 µm^2

Power

1.89 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay C => Q	0.50	2.05	0.67	2.22	0.63	1.69	0.78	1.85
Delay C => QN	0.88	2.43	1.03	2.58	0.73	1.83	0.90	2.00
Delay RN => Q	n.a.	n.a.	n.a.	n.a.	0.20	1.26	0.60	1.67
Delay RN => QN	0.52	2.12	0.94	2.52	n.a.	n.a.	n.a.	n.a.
Slew C => Q	0.10	4.03	0.10	4.03	0.11	2.31	0.11	2.31
Slew C => QN	0.12	4.00	0.12	4.01	0.12	2.33	0.12	2.31
Slew RN => Q	n.a.	n.a.	n.a.	n.a.	0.11	2.30	0.15	2.31
Slew RN => QN	0.16	4.02	0.16	4.02	n.a.	n.a.	n.a.	n.a.

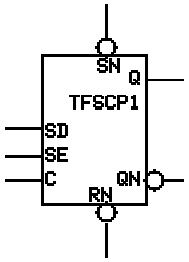
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
RN => C	0	n.a.	0.466	n.a.
SD => C	0.067	0.123	0	0
SE => C	0	0	0	0

	Min Width	
	High	**Low**
C	0.376	0.326
RN	n.a.	0.360

TFSCP1 is a Scan Toggle flip-flop with 1x drive strength. SCAN ENABLE switches between normal DATA input and SCAN DATA input. PRESET and CLEAR are asynchronous and active low.

Truth Table

C	RN	SD	SE	SN	Q	QN
↑	1	0	1	1	0	1
↑	1	X	0	1	~Q	~QN
↑	1	1	1	1	1	0
X	0	X	X	0	0	0
X	0	X	X	1	0	1
X	1	X	X	0	1	0



Capacitance

Pin	Cap [pF]
C	0.004
RN	0.015
SD	0.009
SE	0.006
SN	0.012

Area

0.564 mils^2
364 µm^2

Power

1.4 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay C => Q	0.50	2.15	0.74	2.35	0.60	1.69	0.81	1.87
Delay C => QN	0.71	2.39	0.91	2.58	0.70	1.82	0.94	2.04
Delay RN => Q	0.13	1.78	0.13	1.79	0.20	1.26	0.63	1.70
Delay RN => QN	0.37	2.08	0.75	2.45	n.a.	n.a.	n.a.	n.a.
Delay SN => Q	0.50	2.09	0.89	2.53	n.a.	n.a.	n.a.	n.a.
Delay SN => QN	0.20	1.94	0.34	2.05	0.31	1.56	0.78	2.00
Slew C => Q	0.13	4.27	0.12	4.26	0.12	2.40	0.11	2.39
Slew C => QN	0.14	4.24	0.14	4.25	0.13	2.40	0.13	2.40
Slew RN => Q	0.12	4.31	0.15	4.30	0.10	2.40	0.15	2.39
Slew RN => QN	0.17	4.25	0.17	4.25	n.a.	n.a.	n.a.	n.a.
Slew SN => Q	0.14	4.24	0.13	4.28	n.a.	n.a.	n.a.	n.a.
Slew SN => QN	0.17	4.30	0.20	4.29	0.17	2.46	0.20	2.45

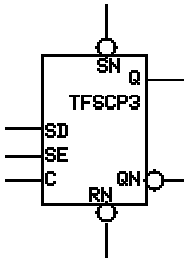
	Setup		Hold	
	rise	fall	rise	fall
RN => C	0	n.a.	0.457	n.a.
SD => C	0.095	0.102	0	0
SE => C	0	0	0	0
SN => C	0	n.a.	0.292	n.a.

	Min Width	
	High	Low
C	0.376	0.326
RN	n.a.	0.360
SN	n.a.	0.380

TFSCP3 is a Scan Toggle flip-flop with 3x drive strength. SCAN ENABLE switches between normal DATA input and SCAN DATA input. PRESET and CLEAR are asynchronous and active low.

Truth Table

C	RN	SD	SE	SN	Q	QN
↑	1	0	1	1	0	1
↑	1	X	0	1	~Q	~QN
↑	1	1	1	1	1	0
X	0	X	X	0	0	0
X	0	X	X	1	0	1
X	1	X	X	0	1	0



Capacitance

Pin	Cap [pF]
C	0.004
RN	0.015
SD	0.009
SE	0.006
SN	0.012

Area

0.592 mils^2
382 µm^2

Power

2.06 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay C => Q	0.50	2.08	0.74	2.28	0.64	1.73	0.81	1.91
Delay C => QN	0.80	2.37	1.01	2.56	0.80	1.90	1.03	2.12
Delay RN => Q	0.14	1.72	0.20	1.75	0.21	1.28	0.62	1.68
Delay RN => QN	0.44	2.05	0.84	2.44	n.a.	n.a.	n.a.	n.a.
Delay SN => Q	0.58	2.09	1.01	2.54	n.a.	n.a.	n.a.	n.a.
Delay SN => QN	0.21	1.83	0.39	1.99	0.40	1.57	0.81	2.03
Slew C => Q	0.10	4.04	0.10	4.02	0.12	2.31	0.11	2.30
Slew C => QN	0.13	4.01	0.13	4.01	0.13	2.32	0.13	2.32
Slew RN => Q	0.10	4.06	0.14	4.08	0.10	2.33	0.15	2.32
Slew RN => QN	0.15	4.02	0.16	4.02	n.a.	n.a.	n.a.	n.a.
Slew SN => Q	0.17	4.03	0.14	4.03	n.a.	n.a.	n.a.	n.a.
Slew SN => QN	0.15	4.08	0.18	4.07	0.17	2.39	0.19	2.39

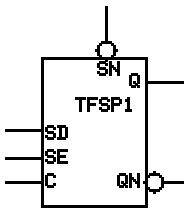
	Setup		Hold	
	rise	fall	rise	fall
RN => C	0	n.a.	0.457	n.a.
SD => C	0.094	0	0	0
SE => C	0	0	0	0
SN => C	0	n.a.	0.291	n.a.

	Min Width	
	High	Low
C	0.376	0.326
RN	n.a.	0.360
SN	n.a.	0.380

TFSP1 is a Scan Toggle flip-flop with 1x drive strength. SCAN ENABLE switches between normal DATA input and SCAN DATA input. PRESET is asynchronous and active low.

Truth Table

C	SD	SE	SN	Q	QN
↑	0	1	1	0	1
↑	X	0	1	~Q	~QN
↑	1	1	1	1	0
X	X	X	0	1	0



Capacitance

Pin	Cap [pF]
C	0.004
SD	0.009
SE	0.006
SN	0.012

Area

0.536 mils^2
346 µm^2

Power

1.42 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay C => Q	0.51	2.15	0.69	2.33	0.55	1.62	0.71	1.78
Delay C => QN	0.68	2.34	0.84	2.50	0.72	1.83	0.90	2.02
Delay SN => Q	0.54	2.18	0.97	2.60	n.a.	n.a.	n.a.	n.a.
Delay SN => QN	n.a.	n.a.	n.a.	n.a.	0.32	1.47	0.74	1.90
Slew C => Q	0.12	4.26	0.12	4.25	0.10	2.39	0.10	2.40
Slew C => QN	0.13	4.23	0.13	4.24	0.12	2.39	0.13	2.39
Slew SN => Q	0.13	4.26	0.14	4.25	n.a.	n.a.	n.a.	n.a.
Slew SN => QN	n.a.	n.a.	n.a.	n.a.	0.16	2.40	0.20	2.41

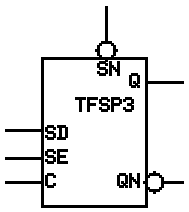
	Setup		Hold	
	rise	**fall**	**rise**	**fall**
SD => C	0.097	0.09	0	0
SE => C	0	0	0	0
SN => C	0	n.a.	0.328	n.a.

	Min Width	
	High	**Low**
C	0.376	0.326
SN	n.a.	0.380

TFSP3 is a Scan Toggle flip-flop with 3x drive strength. SCAN ENABLE switches between normal DATA input and SCAN DATA input. PRESET is asynchronous and active low.

Truth Table

C	SD	SE	SN	Q	QN
↑	0	1	1	0	1
↑	X	0	1	~Q	~QN
↑	1	1	1	1	0
X	X	X	0	1	0



Capacitance

Pin	Cap [pF]
C	0.004
SD	0.009
SE	0.006
SN	0.012

Area

0.564 mils^2
364 µm^2

Power

2.02 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**	**0.003**	**0.96**
Delay C => Q	0.53	2.09	0.71	2.27	0.58	1.64	0.74	1.80
Delay C => QN	0.75	2.31	0.91	2.47	0.80	1.91	0.98	2.09
Delay SN => Q	0.64	2.17	1.07	2.61	n.a.	n.a.	n.a.	n.a.
Delay SN => QN	n.a.	n.a.	n.a.	n.a.	0.36	1.50	0.79	1.93
Slew C => Q	0.11	4.02	0.10	4.03	0.10	2.31	0.10	2.31
Slew C => QN	0.12	4.01	0.12	4.01	0.12	2.33	0.14	2.32
Slew SN => Q	0.12	4.03	0.12	4.03	n.a.	n.a.	n.a.	n.a.
Slew SN => QN	n.a.	n.a.	n.a.	n.a.	0.16	2.33	0.19	2.33

	Setup		Hold	
	rise	**fall**	**rise**	**fall**
SD => C	0.097	0	0	0
SE => C	0	0	0	0
SN => C	0	n.a.	0.328	n.a.

	Min Width	
	High	**Low**
C	0.376	0.326
SN	n.a.	0.380

XOR20 is a 2-input EXCLUSIVE-OR (XOR) gate with 0.5x drive strength.

Truth Table

A	B	Q
0	0	0
0	1	1
1	0	1
1	1	0

Capacitance

Pin	Cap [pF]
A	0.009
B	0.010

Area

0.197 mils^2
127 µm^2

Power

0.35 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**
Delay A => Q	0.25	1.83	0.42	2.00	0.07	0.92	0.11	1.17
Delay B => Q	0.19	1.81	0.32	1.92	0.08	0.93	0.02	1.02
Slew A => Q	0.26	4.30	0.26	4.30	0.16	2.13	0.60	2.25
Slew B => Q	0.20	4.23	0.23	4.24	0.16	2.14	0.56	2.21

XOR21 is a 2-input EXCLUSIVE-OR (XOR) gate with 1x drive strength.

Truth Table

A	B	Q
0	0	0
0	1	1
1	0	1
1	1	0

Capacitance

Pin	Cap [pF]
A	0.013
B	0.015

Area

0.197 mils^2
127 µm^2

Power

0.61 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay A => Q	0.21	1.74	0.37	1.89	0.07	0.89	0.09	1.14
Delay B => Q	0.16	1.71	0.28	1.81	0.07	0.91	0.01	0.99
Slew A => Q	0.22	4.12	0.22	4.11	0.14	2.07	0.58	2.19
Slew B => Q	0.17	4.09	0.20	4.10	0.14	2.07	0.54	2.13

XOR22 is a 2-input EXCLUSIVE-OR (XOR) gate with 2x drive strength.

Truth Table

A	B	Q
0	0	0
0	1	1
1	0	1
1	1	0

Capacitance

Pin	Cap [pF]
A	0.025
B	0.026

Area

0.31 mils^2
200 µm^2

Power

1.14 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**
Delay A => Q	0.19	1.72	0.34	1.86	0.06	0.89	0.07	1.13
Delay B => Q	0.13	1.69	0.23	1.76	0.06	0.90	0.00	0.99
Slew A => Q	0.20	4.10	0.18	4.10	0.12	2.05	0.56	2.16
Slew B => Q	0.13	4.05	0.16	4.06	0.12	2.04	0.52	2.13

XOR30 is a 3-input EXCLUSIVE-OR (XOR) gate with 0.5x drive strength.

Truth Table

A	B	C	Q
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Capacitance

Pin	Cap [pF]
A	0.007
B	0.009
C	0.007

Area

0.31 mils^2
200 µm^2

Power

0.47 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**
Delay A => Q	0.56	2.37	0.59	2.41	0.52	1.42	0.56	1.46
Delay B => Q	0.57	2.38	0.52	2.35	0.50	1.39	0.50	1.40
Delay C => Q	0.22	2.04	0.25	2.05	0.07	0.92	0.00	1.01
Slew A => Q	0.28	4.71	0.31	4.73	0.22	2.11	0.23	2.11
Slew B => Q	0.27	4.71	0.31	4.72	0.22	2.10	0.23	2.10
Slew C => Q	0.18	4.72	0.21	4.70	0.12	2.10	0.53	2.17

XOR31 is a 3-input EXCLUSIVE-OR (XOR) gate with 1x drive strength.

Truth Table

A	B	C	Q
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Capacitance

Pin	Cap [pF]
A	0.007
B	0.009
C	0.012

Area

0.31 mils^2
200 µm^2

Power

0.72 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay A => Q	0.54	2.18	0.57	2.21	0.46	1.31	0.51	1.35
Delay B => Q	0.55	2.19	0.50	2.15	0.46	1.32	0.46	1.30
Delay C => Q	0.16	1.81	0.16	1.80	0.07	0.90	-0.01	0.98
Slew A => Q	0.25	4.30	0.28	4.32	0.17	2.03	0.17	2.03
Slew B => Q	0.25	4.33	0.28	4.32	0.17	2.03	0.17	2.03
Slew C => Q	0.14	4.33	0.17	4.29	0.10	2.04	0.52	2.12

XOR40 is a 4-input EXCLUSIVE-OR (XOR) gate with 0.5x drive strength.

Truth Table

A	B	C	D	Q
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Capacitance

Pin	Cap [pF]
A	0.007
B	0.008
C	0.007
D	0.008

Area

0.423 mils^2
273 µm^2

Power

0.49 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

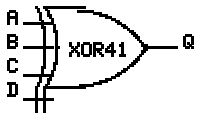
AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**
Delay A => Q	0.62	2.21	0.58	2.17	0.45	1.57	0.44	1.57
Delay B => Q	0.62	2.21	0.65	2.24	0.43	1.55	0.46	1.51
Delay C => Q	0.58	2.19	0.54	2.15	0.45	1.57	0.46	1.60
Delay D => Q	0.58	2.19	0.61	2.21	0.43	1.55	0.43	1.54
Slew A => Q	0.26	4.29	0.25	4.29	0.23	2.55	0.24	2.56
Slew B => Q	0.25	4.29	0.25	4.29	0.24	2.56	0.24	2.53
Slew C => Q	0.27	4.28	0.29	4.29	0.21	2.55	0.21	2.55
Slew D => Q	0.27	4.29	0.30	4.29	0.21	2.56	0.20	2.55

XOR41 is a 4-input EXCLUSIVE-OR (XOR) gate with 1x drive strength.

Truth Table

A	B	C	D	Q
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0



Capacitance

Pin	Cap [pF]
A	0.007
B	0.008
C	0.008
D	0.008

Area

0.423 mils^2
273 µm^2

Power

0.79 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay A => Q	0.69	2.21	0.65	2.17	0.50	1.46	0.46	1.48
Delay B => Q	0.68	2.21	0.71	2.24	0.50	1.44	0.53	1.43
Delay C => Q	0.65	2.19	0.61	2.15	0.46	1.48	0.46	1.52
Delay D => Q	0.64	2.18	0.68	2.22	0.46	1.46	0.49	1.47
Slew A => Q	0.21	4.12	0.25	4.13	0.26	2.41	0.25	2.42
Slew B => Q	0.22	4.12	0.24	4.12	0.26	2.41	0.25	2.41
Slew C => Q	0.24	4.13	0.28	4.13	0.23	2.42	0.23	2.42
Slew D => Q	0.24	4.14	0.27	4.12	0.23	2.40	0.24	2.39

XNR20 is a 2-input EXCLUSIVE-NOR (XNOR) gate with 0.5x drive strength.

Truth Table

A	B	Q
0	0	1
0	1	0
1	0	0
1	1	1

Capacitance

Pin	Cap [pF]
A	0.008
B	0.009

Area

0.169 mils^2
109 µm^2

Power

0.24 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**
Delay A => Q	0.25	2.06	0.30	2.09	0.07	0.92	-0.05	1.00
Delay B => Q	0.25	2.06	0.22	2.03	0.08	0.93	0.01	1.01
Slew A => Q	0.21	4.71	0.23	4.72	0.09	2.07	0.43	2.15
Slew B => Q	0.21	4.72	0.23	4.70	0.12	2.10	0.54	2.19

XNR21 is a 2-input EXCLUSIVE-NOR (XNOR) gate with 1x drive strength.

Truth Table

A	B	Q
0	0	1
0	1	0
1	0	0
1	1	1

Capacitance

Pin	Cap [pF]
A	0.014
B	0.013

Area

0.169 mils^2
109 µm^2

Power

0.5 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay A => Q	0.18	1.82	0.12	1.77	0.07	0.90	0.00	0.99
Delay B => Q	0.18	1.82	0.19	1.83	0.06	0.88	-0.07	0.97
Slew A => Q	0.16	4.28	0.18	4.36	0.11	2.03	0.51	2.12
Slew B => Q	0.16	4.31	0.19	4.30	0.07	2.00	0.41	2.09

XNR22 is a 2-input EXCLUSIVE-NOR (XNOR) gate with 2x drive strength.

Truth Table

A	B	Q
0	0	1
0	1	0
1	0	0
1	1	1

Capacitance

Pin	Cap [pF]
A	0.027
B	0.025

Area

0.31 mils^2
200 µm^2

Power

1.03 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**	**0.002**	**0.64**
Delay A => Q	0.14	1.72	0.08	1.65	0.07	0.90	0.00	0.99
Delay B => Q	0.14	1.73	0.14	1.71	0.05	0.88	-0.08	0.97
Slew A => Q	0.13	4.16	0.16	4.16	0.12	2.05	0.52	2.12
Slew B => Q	0.13	4.17	0.16	4.14	0.06	2.01	0.40	2.07

XNR30 is a 3-input EXCLUSIVE-NOR (XNOR) gate with 0.5x drive strength.

Truth Table

A	B	C	Q
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Capacitance

Pin	Cap [pF]
A	0.007
B	0.009
C	0.007

Area

0.31 mils^2
200 µm^2

Power

0.58 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**
Delay A => Q	0.62	2.21	0.66	2.25	0.45	1.57	0.48	1.57
Delay B => Q	0.63	2.22	0.59	2.18	0.45	1.55	0.41	1.51
Delay C => Q	0.19	1.80	0.29	1.88	0.08	0.93	0.02	1.03
Slew A => Q	0.25	4.29	0.25	4.30	0.23	2.53	0.23	2.54
Slew B => Q	0.25	4.29	0.25	4.29	0.23	2.56	0.23	2.55
Slew C => Q	0.20	4.27	0.23	4.26	0.16	2.14	0.55	2.23

XNR31 is a 3-input EXCLUSIVE-NOR (XNOR) gate with 1x drive strength.

Truth Table

A	B	C	Q
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Capacitance

Pin	Cap [pF]
A	0.007
B	0.009
C	0.012

Area

0.31 mils^2
200 µm^2

Power

0.91 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay A => Q	0.69	2.22	0.73	2.26	0.51	1.46	0.55	1.48
Delay B => Q	0.70	2.23	0.66	2.19	0.52	1.44	0.47	1.43
Delay C => Q	0.16	1.71	0.28	1.80	0.07	0.91	0.01	1.00
Slew A => Q	0.22	4.12	0.24	4.13	0.26	2.41	0.25	2.41
Slew B => Q	0.22	4.12	0.24	4.11	0.25	2.40	0.25	2.41
Slew C => Q	0.17	4.09	0.20	4.10	0.14	2.08	0.54	2.16

XNR40 is a 4-input EXCLUSIVE-NOR (XNOR) gate with 0.5x drive strength.

Truth Table

A	B	C	D	Q
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
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1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
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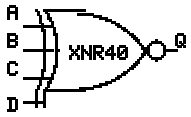

Capacitance

Pin	Cap [pF]
A	0.008
B	0.008
C	0.008
D	0.008

Area

0.423 mils^2
273 µm^2

Power

0.51 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**	**0.0005**	**0.16**
Delay A => Q	0.56	2.38	0.52	2.34	0.48	1.41	0.51	1.44
Delay B => Q	0.55	2.37	0.59	2.41	0.45	1.38	0.45	1.37
Delay C => Q	0.58	2.40	0.54	2.35	0.49	1.38	0.53	1.42
Delay D => Q	0.57	2.39	0.61	2.44	0.47	1.35	0.47	1.36
Slew A => Q	0.29	4.70	0.31	4.68	0.18	2.10	0.18	2.10
Slew B => Q	0.27	4.71	0.31	4.70	0.18	2.10	0.18	2.10
Slew C => Q	0.28	4.74	0.31	4.67	0.22	2.11	0.22	2.10
Slew D => Q	0.27	4.74	0.30	4.74	0.22	2.10	0.21	2.12

XNR41 is a 4-input EXCLUSIVE-NOR (XNOR) gate with 1x drive strength.

Truth Table

A	B	C	D	Q
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
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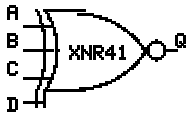
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1



Capacitance

Pin	Cap [pF]
A	0.008
B	0.008
C	0.008
D	0.008

Area

0.423 mils^2
273 µm^2

Power

0.81 µW/MHz

Delay [ns] = tpd.. = f(SL, L) with SL = Input Slope [ns] ; L = Output Load [pF]
Output Slope [ns] = op_sl.. = f(SL, L) with L = Output Load [pF]

AC Characteristics: Tj = 25°C VDD = 3.3V Typical Process

AC Characteristics

	Rise				Fall			
Slope [ns]	**0.05**		**2**		**0.05**		**2**	
Load [pF]	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**	**0.001**	**0.32**
Delay A => Q	0.56	2.21	0.52	2.17	0.45	1.30	0.47	1.33
Delay B => Q	0.55	2.20	0.58	2.23	0.45	1.29	0.48	1.33
Delay C => Q	0.55	2.19	0.52	2.15	0.44	1.29	0.47	1.31
Delay D => Q	0.55	2.19	0.58	2.22	0.43	1.29	0.46	1.32
Slew A => Q	0.26	4.32	0.30	4.31	0.20	2.04	0.20	2.03
Slew B => Q	0.25	4.34	0.29	4.28	0.20	2.04	0.20	2.03
Slew C => Q	0.25	4.29	0.28	4.32	0.16	2.03	0.16	2.03
Slew D => Q	0.25	4.34	0.27	4.28	0.16	2.03	0.16	2.03