Cell Library Databook

a single team databook with tightly controlled structure

Main Body

- Title Page
- Contents - including list of all cells with page numbers
- Introduction (max 3 sides)
- Datasheet (1 per cell - 1 side each)
- Summary of results (max 1 side)

Appendix A

- Team Management (max 1 side)
- Division of Labour Form (1 side)

Appendix B

- Design detail for major cells (max 2 sides per major cell)

- Title Page

  Cell Library Databook

  by Team C1

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- Introduction (max 3 sides)

  Introduces the library and the databook.

  Gives detail of features common to all cells in the library (e.g. cell height)

  Picture showing position of signals and other cell structures such as the N-well as they exist at the interface between cells

Cell Library Databook

- Datasheet (1 side per cell[1])

  Include datasheets for cells to be used by the ASIC designer (e.g. scanreg) rather than cells only used by library cell designers (e.g. rdtype, smux3).

  - cell name
  - cell description
  - cell designer(s)
  - symbol[2]
  - gate level circuit diagram[3]
  - abstract

    black box view showing dimensions
  - table of measured parameters
  - verilog simulation waveform

[1] trivial support cells may be combined on one page
[2] no symbol exists for leftbuf, rightend, tiehigh, tielow, rowcrosser
[3] no gate level circuit diagram required for nand, nor, inv, tiehigh, tielow, rowcrosser

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- Design detail for major cells (max 2 sides per major cell)

  `rdtype, smux2, smux3, fulladder, halfadder, xor2, leftbuf`

  A sub-section should exist for each designer, dealing with the major cells they have designed.

  For each cell the following information should be included in the design detail:[4]

  - transistor level circuit diagram
    with comments on derivation if appropriate
  - stick diagram
  - details of circuit for loaded simulation
  - results of loaded simulation
    numerical and graphical

[4] take care with diagrams, don't scan/capture my schematics, avoid screen capture of simulation and layout if possible, and avoid using inappropriate pre-defined circuit symbols (e.g. MOS transistors with visible substrate connection).

Cell Library Databook

- Presentation
  - Use full sentences and paragraphs
    note form is acceptable on the datasheets but not in design detail sections or elsewhere in the databook
  - Cover
    The handin system allows you to print a standard cover for this report
  - Binding
    This report must be bound. If printing double sided, then a neat line of staples down the long edge of the report will be sufficient.

Documentation for this exercise should be submitted to the school office.

Deadline for documentation is 16:00 on Tuesday 11th December.

Final note: extra credit may be given for advanced characterization e.g. Δt_p *,* t_{setup} *(for sequential gates), or clock skew simulations (for left end of row cell)*