Digital Simulation using NC-Verilog

Shengyu Duan and Terrence Mak

Digital Simulations Lab Instructions

For this lab you will need:

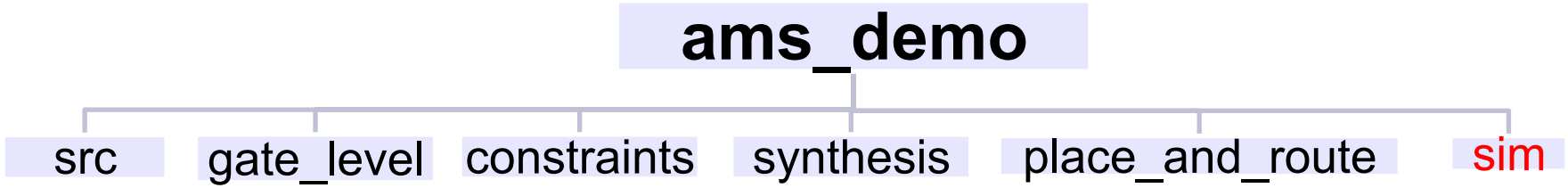
1. *A post-layout Verilog net list of the design* -
   obtained from place and route lab (wrap_qmults_final.v)

2. *A Standard Delay Format file of the design*
   - again, from place and route (wrap_qmults_func_max.sdf)

3. *A Verilog testbench*
   - the same as in synthesis lab (wrap_qmults_stim.sv)

Design Directory Management

1. Inside your design directory create a sub-directory called sim
2. Copy the design files into sim



Introduction

- The simulator we are going to use in this lab is Cadence NC-Verilog

- Before we run the simulation, there are some modifications you need to make …

Timescale

- **NC-Verilog requires pre-defined timescales. Thus, put it on all modules of your post-layout netlist (wrap_qmults_final.v),**

```
module qmults_N8_DW01_add_1 (
        A,
        B,
        CI,
        SUM,
        CO);

   // timescale definition
   timeunit 1ns;
   timeprecision 1ps;

   ...........
```

```
module wrap_qmults (
        nReset,
        multiplicand,
        Clock,
        overflow,
        start,
        complete,
        multiplier,
        result);

   // timescale definition
   timeunit 1ns;
   timeprecision 1ps;

   .........
```

SDF Annotation

- **In order to simulate your design with correct delays, you need to annotate the .sdf file, in the testbench:**

```
module wrap_qmults_stim;

  .......

  // Instantiate the Unit Under Test (UUT)
  wrap_qmults uut (
    .......
   );

  initial
    begin
      // sdf annotation
      $sdf_annotate ("wrap_qmults_func_max.sdf", uut);
      ......
    end

  .......
```

- **Make sure you annotate the .sdf for the right instance**

Run Simulation

- Now you can simulate your design by following command:

ncverilog -sv +naccess+r -f /opt/cad/designkits/ams/v410/verilog/c35b4/verilogin.inc wrap_qmults_stim.sv wrap_qmults_final.v

- The circuit under test is a multiplier. Thus the functionality can be easily verified by observing the waves.