Full chip constraints (1)

- Specify Clock Frequency

```
create_clock -period 20 -name master_clock [get_ports Clock]
```

- Model Clock Tree *uncertainty = skew + jitter*

```
set_clock_latency     2.5 [get_clocks master_clock]
set_clock_transition  0.5 [get_clocks master_clock]
set_clock_uncertainty 1.0 [get_clocks master_clock]
```

- Specify Input and Output Timing

```
set_output_delay 2.0 -max -network_latency_included -clock master_clock \
    [all_outputs]
set_output_delay 0.1 -min -network_latency_included -clock master_clock \
    [all_outputs]

set_input_delay  2.0 -max -network_latency_included -clock master_clock \
    [remove_from_collection [all_inputs] [get_ports Clock]]
set_input_delay  0.1 -min -network_latency_included -clock master_clock \
    [remove_from_collection [all_inputs] [get_ports Clock]]
```

Full chip constraints (2)

- Specify Input Drive and Output Load

```
set_load 1.0  -max [all_outputs]
set_load 0.01 -min [all_outputs]

set_driving_cell -max -library c35_IOLIB_WC -lib_cell BU24P -pin PAD [all_inputs]
set_driving_cell -min -library c35_IOLIB_WC -lib_cell BU1P  -pin PAD [all_inputs]
```

- Specify Timing Exclusions

```
set_ideal_network [get_ports nReset]
```

- Other constraints

```
set_max_area 0
```