C035U (0.35 Micron) Core CMOS Design Rules

DES-0005 Rev. 11.0

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C035U (0.35 Micron) Core CMOS Design Rules

Owner: Technology Research & Development

Location: Global

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C035U (0.35 Micron) Core CMOS Design Rules (DES-0005)
Revision History

Revision	Requestor	Release Date	Description
11.0	AL	05-Oct-2010	• removal of Schottky diode layout rules and reference to this device in electrical parameters section
10.0	BG	28-Jun-2010	• MIMC Layout Rule 78.17 update: rule description change and rule value changed from 2.00 to 2.20
9.0	HDV	26-Apr-2010	• lfndm14 table and graphs added – V_absmax of the device limited to 12V • ProbePad rule PAD.4 on metdis changed to 'not checked' • Lonely via note added • Matching info on poly and diffused resistors added • AMI Semiconductor references changed to ON Semiconductor
8.0	HD, HDV	01-Dec-2008	• Addition of optional power metal layers and related rules and exceptions. • Move WCAPA recommendations to suggested, not checked. • Allow MIMC shapes <2025 um2, not only squares • Addition LREC marker description
7.0	HDV	19-Sept-2008	• Model update after verification up till 200C on i3t50 added to manual for cmos and diodes. • Corners provided on temperature model of mimcs. • Electrical info on mmchb and mmchp
6.0	HDV	25-Mar-2008	• Change in bondpad style due to metal lift issue. • wtopmetal3, wtopmetal4 : exception for bondpads and probepads. • XN.1, XN.5, XP.2 descriptions changed, implementation stayed. • XP.6: not checked outside of y9, if present. • Matched mimcs - minimum size reduced from 20 to 10 • MMC.3, MMC.4 (Dummy caps) 'suggested not checked'. • 17.23 min. matched resistor length changed from 25 to 5 • MR.2 & SHIE.3 redundancy solved. • Mtl4/5a.min/max checks made consistent with use of top layer. • 18.21 implemented and value in manual changed from 0.4 to 0.3. • Wcapa rules : typo corrected, no change. • Pldd description : typo corrected (pldd implanted), no change.
5.0	HDV	10-Jul-2007	• MIMC rules updated and graphic drawings added • 13.2a1 rule description modified in High-Density Memories • PWIMP graphic drawing modified to clarify 50.4,50.7 • Remove electrical characterisation of not-released devices enmsib/epmsib
4.0	HDV	25-May-2007	The DES-0005 is updated starting from 1000042 Rev.A. Changes with respect to 1000042 Rev.A.: • textual changes on rules

			31.32,31.33,2.10,26.3,XN.5mem,XP.4mem, XN.5, XP.4,13.28,13.29,23.11,27.7,34.7,36.7,53.7,50.3 • add rule 61.1 (NOGEN) • removal of rule MR.1 • reorganisation ZZD rules/exceptions. (removal ZZD_EXC3,ZZD_EXC4,ZZD_EXC6,ZZD_EXC8) • removal enmio/epmio devices from this manual
The following reflect revisions to Document# 1000042			
A	MA	09-Aug-2006	Initial release of 1000042. Unreleased version corresponding to this initial release was referred to as DES-0005 version 3.7, DES-0005 version 3.0 is a released Document Control specification which moves to a status of obsolete with this release.
The following reflect revisions to Document# DES-0005			

Revision	Requestor	Release Date	Request Number Date	Request Number	Pages	Description
3.0	JDG, JR, HDV, DB		26-May-2005	31257	All	(Corresponds to draft revision no 3.2) Updated Section 8.2 to current device, model and P-Cell names Addition of lonely via rules Additional push rules for high density memories Correction electro migration lifetime from 25 to 10 years Introduce m4, m5 resistor devices in par. 8.2.3. Added topic on Layout and design rules for Polydiode and on metal metal capacitors (bar and plate) Modified rules on mshield for matched poly resistors and matched MIMC capacitors Added drawing on bondpad rules Replaced guidelines by rules Added Schottky diode Added: guidelines for MRES and MDIODE markers; basic rules for NOTPW and PWIMP; rules for PWARNW common resistor Added wide metal spacing rules for porting C035M blocks to C035U-based process technologies. Added metal 5 option for for bar and plate metal capacitors Aligning DRM to input deck. Adapting rule 18.3 Adapting rules for

						nndm15/lfnndm14 for unification Adaptation of the rule 13.5, removal of the exception Rule 18.37 added Rule 26.3 re-phrased Change ref document 13600 into global document 1000033
2.0	JDG		16-Jan-2004	029411	All 72,91-95 85	Complete revision for migration of C035U-based technologies from p-epi to n-epi Remove rule 13.27; update electromigration rules Rule 31.34a: - rename to 31.34 - Change from fixed via spacing to minimum via spacing on the bonding pads - Delete Rule 31.34b
1.0	JDG		19-Feb-2003	027755	All	New document

C035U (0.35 Micron) Core CMOS Design Rules

Introduction and Definitions

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Introduction and Definitions

PURPOSE

This Design Rule Manual provides the layout rules and electrical parameters for the core, Low Voltage, Mixed Signal CMOS in C035U based technologies built on N-type epitaxial silicon.

SCOPE

This document applies to Design Engineers, Technology Engineers, CAD Engineers, Process Engineers, Quality Assurance Engineers, Reliability Engineers and Product Engineers.

It is the prime reference to be applied for the design and layout of any Low Voltage, Mixed Signal CMOS component or block in C035U based technologies.

This document also applies to layout rules for Power metal option.

REFERENCE DOCUMENTS

GP 10800	General Description of the measurement methods of electrical parameters
DS 13330	C035M-D Design Rule Manual
DS 13337	C035M Design Rule Manual Supplement for Analogue Option (C035M-A)
1000115	I3T25 (0.35 Micron) Design Rules
DES-0034	I3T50U / I3T50E Layout Rules Manual
DES-0002	I3T80U Layout Rule Manual
08-0496	I3T80U Flash Analogue IP Design Rule Manual
1000033	Assembly/Probe Related Layout Rules

GLOSSARY

DRC	Design Rule Check
DTI	Deep Trench Isolation
GDS	Graphical Design System
IGS	Interactive Graphical System
LVS	Layout Versus Schematic
OTP	One Time Programmable
TD	Technology Development
TRD	Technology R&D Department
ARC	Anti Reflective Coating

GENERAL REQUIREMENTS

Responsibilities

It is the responsibility of the ON Semiconductor TRD department to maintain this document and ensure its content is correct and up to date.

It is the responsibility of the TD/CAD department to create and maintain technology files consistent with the information contained in this document; technology files include DRC, LVS and GDS layer stream tables.

Updates of this document are possible. It is the user's responsibility to consult the document control center on the availability of updated revisions of this specification.

Safety Requirements

NA.

Equipment and Material

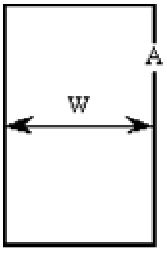
NA.

DEFINITIONS

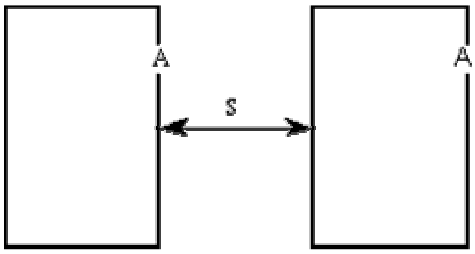
Convention for specifying layout rules

The following conventions are used to specify the layout rules in this specification:

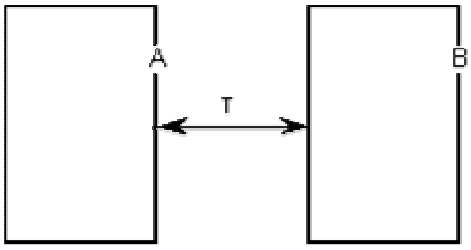
- Level A width "W" is defined as:



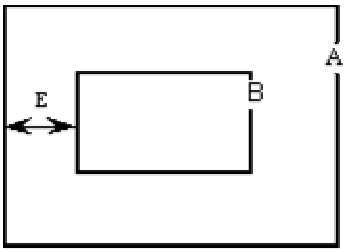
- Level A spacing "S" is defined as:



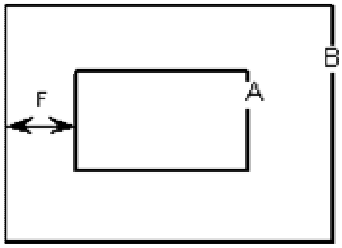
- Level A spacing "T" to level B is defined as:



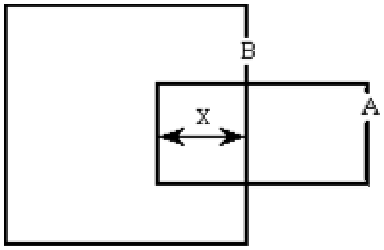
- Level A enclosure "E" of level B is defined as:



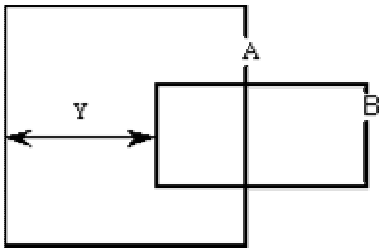
- Level A enclosure "F" by level B is defined as:



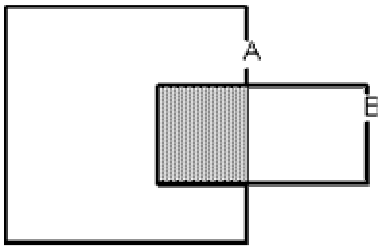
- Level A intersection "X" with level B is defined as:



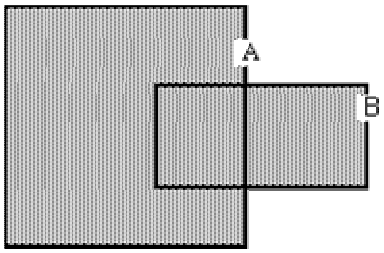
- Level A extension "Y" on level B geometry is defined as:



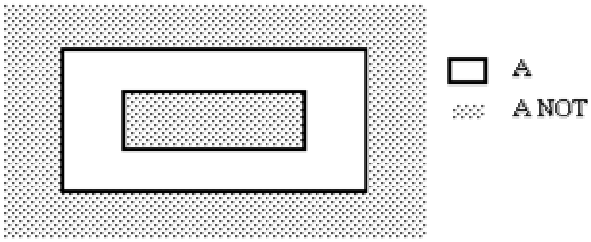
- Level A "AND" level B is defined as the area common to both:



- Level A "OR" level B is defined as the union of both geometries:



- Level "A NOT" is defined as the complement of level A:



C035U (0.35 Micron) Core CMOS Design Rules

Mask Identification

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MASK IDENTIFICATION

Introduction

The core Low Voltage, Mixed Signal CMOS in ON Semiconductor's C035U-based technologies is built on n-epitaxial silicon.

Isolation between N-EPI pockets is technology dependent. Refer to the process technology specific Layout Rule Manuals for isolation rules, and layout rules applicable to process technology specific components.

The 0.35 µm Low Voltage, Mixed Signal core CMOS is developed for the design of circuits operating at a power supply voltage of 3.3 volt (+0.3/-0.6 volt). It is based on the ON Semiconductor Belgium BVBA qualified C035M technology family (see specifications DS00013330 and DS00013337 for C035M Design Rule Manuals). The differences include:

- Enhanced analogue performance
  - Improved resistor and transistor matching
  - Higher unit area capacitance – 1.5 fF/ µm ^{2} versus 1.1 fF/ µm ^{2})
- Replacement of the poly/poly capacitor by a metal/metal capacitor
- Layout rule enhancements, resulting in a higher packing density

C035U-based technologies offer flexible metallization schemes. Minimum number of metal layers is 3, maximum number of metal layers is 5. The top layer metal can be either thin or thick. The table below gives an overview of the qualified metallization modules available for product design.

Level	Option 1	Option 2	Option 3	Option 4	Option 5	Option 6
Metal 1	72 mΩ/sq	72 mΩ/sq	72 mΩ/sq	72 mΩ/sq	72 mΩ/sq	72 mΩ/sq
Metal 2	55 mΩ/sq	55 mΩ/sq	55 mΩ/sq	55 mΩ/sq	55 mΩ/sq	55 mΩ/sq
Metal 3	55 mΩ/sq	55 mΩ/sq	55 mΩ/sq	34 mΩ/sq	55 mΩ/sq	55 mΩ/sq
Metal 4	-	55 mΩ/sq	55 mΩ/sq	-	34 mΩ/sq	55 mΩ/sq
Metal 5	-	-	55 mΩ/sq	-	-	34 mΩ/sq

The mixed-signal options include high-ohmic polysilicon resistors (HIPO - 1 kΩ/sq) and high precision metal/metal capacitors (MIM - 1.5 fF/ µm ^{2}). The MIM capacitor top plate is sandwiched between metal 2 and metal 3.

Characterized Devices for Circuit Design

Hereafter, the list of characterized devices available for circuit design is given. Only these devices are listed which are common to all C035U-based technologies.

Several classes of devices can be defined. Other devices than those specified are not allowed.

Fully Characterized Devices

For this first class of devices, room temperature characterization, temperature sensitivity, voltage sensitivity, matching, statistical behavior, description in terms of DRC, extraction of layout, symbol, SPICE modeling are available. These devices can be used for any kind of application.

Component	Device name	Model name	Pcell name	Application & notes
NMOS transistor	ENM	enm	enm	Standard low voltage NMOS
PMOS transistor	EPM	epm	epm	Standard Low voltage PMOS
Unsal. N+ poly resistor	NPOR	npor/nporxwnl/nporxwbb	npor	Medium resistivity poly resistor
Unsal. P+ poly resistor	PPOR	ppor/pporxwnl/pporxwbb	ppor	Medium resistivity poly resistor
Unsal. N+ active resistor (in Pwell/N-epi; Pwell is third terminal)	NPRPW	nprpw/nprpwnl/nprpwbb	nprpw	Medium resistivity diffusion resistor
Unsal. P+ active resistor (in Nwell/N-epi, Nwell is third terminal)	PPRNW	pprnw/pprnwnl/pprnwbb	pprpw	Medium resistivity diffusion resistor
Silicided P+ poly resistor	LOPOR	lopor/ loporxwnl/ loporxwbb	lopor	Poly interconnect parasitic modeling
Silicided N+/Pw junction diode	NPPWD	nppwd	nppwd	LV I/O diode
Silicided P+/Nw junction diode	PPNWD	ppnwd	ppnwd	LV I/O diode
Floating, 14V natural NDMOS	LFNDM14	lfndm14	lfndm14	General purpose
Metal/Metal Capacitor – BAR	MMCHB	mmchb / mmchbxw	mmchb	
Metal/Metal Capacitor – PLATE	MMCHP	mmchp / mmchpxw	mmchp	

Devices available for specific applications

This second class of devices is available only for a restricted kind of applications. The characterization of these devices is limited to the strict minimum for use in the targeted application.

Component	Device name	Model name	Pcell name	Application & notes
NMOS I/O transistor (with non-silicided source, drain, gate)	ENMIO	enmio	enmio	Nmos connected to I/O pin
PMOS I/O transistor (with non-silicided source, drain,gate)	EPMIO	epmio	epmio	Pmos connected to I/O pin
Poly Diode	POLYD	polyd	polyd	
Poly Diode over N-Well	POLYDNW	polydnw	polydnw	
P^+/NLDD diode	CLIOD7	cliod7	cliod7	ESD protection, gate voltage clamping diode
Non-floating, 15V natural NDMOS	LNNDM15	lnndm15	lnndm15	OTP
Zapping N+/P+ Zener Diode	UZZD/ZZD	uzzd / zzd	uzzd / zzd	OTP

PNP bipolar transistors are used in circuit for band-gap voltage reference. Due to the peculiarity of the process of each C035U-based process technology, see the related DRM for the specific structure and performance.

Natural Digital Devices

This third class includes "naturally built-in devices". Any characterization performed on these devices is for process control purposes only. The support of these devices is not guaranteed.

Component	Device name	Model name	Pcell name	Application & notes
Metal 1 Resistor	m1r	m1r	m1r	refer to Introduction section above for values
Metal 2 Resistor	m2r	m2r	m2r	refer to Introduction section above for values
Metal 3 Resistor	m3r	m3r	m3r	refer to Introduction section above for values
Metal 4 Resistor	m4r	m4r	m4r	refer to Introduction section above for values
Metal 5 Resistor	m5r	m5r	m5r	refer to Introduction section above for values

Fully Characterized Analogue Devices

Component	Device name	Model name	Pcell name	Application & notes
Highly linear M2/M2.5 floating capacitor	MIMC	mimc / mimcxw	mimc	Typical 1.5fF/μm^2
High ohmic p-doped poly resistor (HIPO)	HIPOR	hipor / hiporxwnl / hiporxwbb	hipor	Typical 1 kΩ/sq; 2 terminals, floating

It is strongly advised that analogue designs should be made using only the fully characterized devices.

Process Flow

Key features of the core C035U-based CMOS process flow are:

SUBSTRATE : the CMOS devices are integrated into the n-type epitaxial layer grown on top of the p-type doped substrate; resistivity of the p-type substrate is 10-20 Ωcm. The resistivity of the n-type epitaxial layer is process-technology dependent.

LOCOS : conventional LOCOS is used for active device isolation.

RETROGRADE WELLS have lower lateral well diffusion, which allows smaller N^+/P^+ spacing across the well border with enhanced latch-up behaviour as compared to conventionally diffused wells. Lower well sheet resistances can be achieved and an additional advantage is the good control of parasitic field transistors.

N^+/P^+ POLY GATE: N^+ poly gate is used for NMOS transistors, P^+ poly gate is used for PMOS transistors. This allows symmetrical design of the active devices. For PMOS transistors, compared to N^+ poly gate, P^+ poly gate improves short channel behaviour and sensitivity to hot carrier degradation.

HIPO RESISTOR: High ohmic poly-silicon resistor formed in the gate poly layer but using an additional masking step and separate implant to achieve the appropriate sheet resistance.

SILICIDE: the silicide technology provides low gate and source/drain series resistance. The silicide is needed to short N^+ poly and P^+ poly. Circuit packing density can be increased because the silicide allows abutting straps with only one contact.

SILICIDE PROTECTION: this feature allows preventing silicide formation over I/O transistors for improved ESD performance. It is also used to obtain non-silicided resistors in active area and/or polysilicon.

PLANARIZED DIELECTRICS: for enhanced step coverage of metal lines and lithography performance (depth-of-focus). CHEMICAL MECHANICAL POLISHING (CMP) is used to achieve the required level of planarisation.

TUNGSTEN PLUGS: contacts and vias are filled with tungsten; this results in enhanced step coverage of the metal lines in the contacts and vias. This technology feature allows random placement of contacts and vias, without proximity rules. Full stacking of contacts and vias is allowed.

METAL/METAL CAPACITOR: Formed using the metal2 layer as bottom plate, a deposited dielectric and an additional metal2.5 layer as top plate of the capacitor.

General Requirements for GDS numbering

The preparation of the final data based on which the masks will be fabricated is performed on the GDS data. GDS data are generated by streaming out (exporting) the layout data from the IGS system using a technology specific stream out layers table.

Data on a GDS layer can either be directly used to generate a mask, or several GDS layers may have to be combined to generate a mask.

In order to distinguish between data on a GDS layer and data on a mask, in this specification the name of an GDS layer will be in lower case (e.g. "active"), while the name of the corresponding mask (if any) will be in upper case (e.g. "ACTIVE").

Only layout databases meeting the requirements listed hereafter will be accepted for mask making.

- Layout data and special purpose data (e.g. LVS markers, dummy metal exclusion marker, …) must be present on the correct GDS layers and the correct data types as specified in the technology-specific layer stream tables.
- Layout data present on other GDS layers than those indicated in this specification are ignored during mask preparation.
- Generally, a number of GDS layers are not "drawn" (i.e. during layout), but automatically "generated" from one or more other layers. No layout data must be present on GDS layers that are generated automatically, unless covered by GDS layer 61 (nogen). GDS layer 61 (nogen) disables ALL automatic data generations, meaning that all data on the area covered by layer 61 is used as drawn. All data, present on automatically generated GDS layers and which are not covered by GDS layer 61 will be ignored during mask preparation. The use of GDS layer nogen is not permitted except in consultation with the mask making and Technology R&D departments at ON Semiconductor.

  Refer to technology-specific mask generation specifications for the details on how drawn layers are combined to result in the final data, which will be used for mask preparation.
- Non-layout data such as CD structures, layer identifications and/or revision numbers, logo's, ETEST structures etc., must not introduce any layout rule violations. When layout rule violations cannot be avoided, the customer shall always notify ON Semiconductor prior to tape delivery, giving details of the cell names of the structures not complying with this layout rule specification.
- Layout data which translate into patterns on the physical masks, must be on the correct data types:

  All other data types are for CAD purposes only and will be ignored during mask generation and preparation.

Layout data GDS numbering

The table hereafter gives the list of GDS layers that will contain data to be translated into processing masks (marker layers, special layers for e.g. LVS checking, etc. are excluded from this table).

Only the common layers for all C035U-based technologies and required for the core low voltage mixed-signal CMOS are listed in the table.

For the GDS numbers in the table below, data type 0 (normal layout – dg) and data type 30 (high density – hd) are assumed; in case other data types are involved, this is indicated by xx_yy, where xx refers to the GDS number and yy refers to the data type.

MASK NAME	DIGITIZED AREA	GDS NUMBER	GDS LAYER NAME	DRAWN/ GENERATED	LAYOUT GRID
ACTIVE	DARK	2	active	D	0.05 µm
NWELL	CLEAR	1	nwell	D	0.05 µm
PWELL	DARK	8	not_pwell	G	0.05 µm
-	-	50	pwimp	D	0.05 µm
POLY	DARK	13	poly	D	0.025 µm(*)
HIPO	CLEAR	26	hipo	D	0.05 µm
NLDD	DARK	14	nldd	G	0.05 µm
-	-	38	nlddprotect	D	0.05 µm
PLDD	CLEAR	90	plddonly	G	0.05 µm
-	-	47	plddprotect	D	0.05 µm
N+IMPLANT	DARK	16	nplus	G	0.05 µm
-	-	66	nplusprotect	D	0.05 µm
P+IMPLANT	CLEAR	17	pplus	D	0.05 µm
SALPROTECT	DARK	18	siprot	D	0.05 µm
CONTACT	CLEAR	19	contact	D	0.025 µm(*)
METAL1	DARK	23 23_1 23_2	metal1 metal1_pS metal1_nS	D	0.05 µm
VIA1	CLEAR	25	v1	D	0.05 µm
METAL2	DARK	27 27_1 27_2	metal2 metal2_pS metal2_nS	D	0.05 µm
MIMC	DARK	78	mimc	D	0.05 µm
VIA2	CLEAR	32	v2	D	0.05 µm
METAL3	DARK	34 34_1 34_2	metal3 metal3_pS metal3_nS	D	0.05 µm
VIA3	CLEAR	35	v3	D	0.05 µm
METAL4	DARK	36 36_1 36_2	metal4 metal4_pS metal4_nS	D	0.05 µm
VIA4	CLEAR	52	v4	D	0.05 µm
METAL5	DARK	53 53_1 53_2	metal5 metal5_pS metal5_nS	D	0.05 µm
PASSIVATION	CLEAR	31(**)	nitride	D/G	0.05 µm
-		105	ViaEP	D	0.05 µm
POWERMETAL	CLEAR	85	MetalEP	D	0.05 µm

(*) The 0.025 µm layout grid is a legacy from the C035M process technology.
(**) For power metal option, GDS layer #105 is merged into GDS layer #31 to generate data for 'Passivation' mask.

Marking Layers GDS numbering

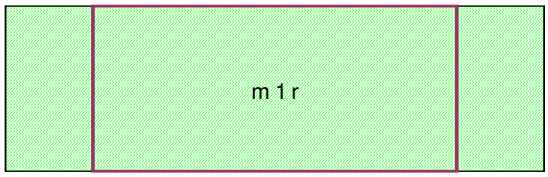
Drawing layers for CAD (DRC/LVS) and/or mask making purposes.

GDS NAME	GDS NR.	Data Type	Purpose	Description
nogen	61	0	Drawing [dg]	Blocks automatic generation of data during mask preparation
mexclude	62	4	?	Blocks automatic generation of dummy metal during mask making; is also used in DRC for metal density checks
metdis	63	0	D	Blocks automatic generation of dummy metal during mask making; is also used in DRC for metal density checks
dractxt	15	0	[dg]	To allow use of ON Semiconductor bonding diagram editor, all bonding pads must be labelled using IGS layer 15, "dractxt". Labels must have a unique name per pad (e.g. all VDD pads must have a different name, i.e. VDD1, VDD2, ...). Bonding labels must have their origin within the layer passivation.
noring	51	0	[dg]	Used in mask making to disable generation of ring bond pads (5-layer metal process only)
mcapa	3	0	[dg]	Identifies bottom plate of metal or poly capacitors
mres	7	0	[dg]	Marks all kind of resistors, but often has no impact on LVS
mdiode	4	0	[dg]	Layer to identify all diodes
lowacc	108	0	[dg]	Identifies polysilicon resistors for which matching/linearity is not important; used during DRC to disable checks on matching rules
i3tpoly	109	0	[dg]	Layer to identify non-silicided N+ and P+ polysilicon resistors in C035U-based technologies (see section on “porting C035M layout”)
excmem	97	0	[dg]	Layer to identify C035U high-density memories; used in DRC and mask making
c035mrec	111	0	[dg]	Layer to identify C035M layouts; used in DRC and mask making (see section on “porting C035M layout”)
mrpo	13	17	MarkerR [mR]	Salicided polysilicon resistor
mrm1	23	17	[mR]	Metal 1 resistor
mrm2	27	17	[mR]	Metal 2 resistor
mrm3	34	17	[mR]	Metal 3 resistor
mrm4	36	17	[mR]	Metal 4 resistor
mrm5	53	17	[mR]	Metal 5 resistor
mpnp	6	0	[dg]	Marker for PNP transistor
mnpn	5	0	[dg]	Marker for NPN transistor
msub	9	0	[dg]	Marker to define substrate regions when they form a multiple ground net
mshield	62	49	[dg]	Used to mark shielding implants under floating passive elements (capacitors and resistors)
DREC	113	0	[dg]	device recognition
LREC	114	0	[dg]	high voltage pocket recognition
NREC	118	0	[dg]	

In general, a device is recognised by means of (1) an original combination of layers, (2) a marking layer and (3) a piece of text (on the marking layer) denoting the type of device. This combination will be referred to as the device marker.

Rules for MRES layer (resistor marking)

A resistor device marker must outline the body of each resistor (well, active, poly, and metal resistors). Without this device marker the resistors will not be recognized. This device marker is created with MRES and placed coincident with the body of the resistor. The size of the resistor is defined according to the combination of the characteristic layers and the described marker (see the metal1 resistor below). The metal1 resistor below is a metal1 polygon with an MRES rectangle coincident with the body of the resistor and MRES text (over the body of the resistor) telling which resistor it is.



The LOWACC ("low accuracy") marking layer is introduced to avoid the application of specific layout rules intended for optimised matching and/or linearity performance when the device does not require those constraints in that specific application. Several layout rules will be disabled when this layer is placed over that device, for example, over a bank of HIPO resistors.

Rules for MDIODE layer (diode marking)

A diode is made by the juxtaposition (or inclusion) of a region implanted with one kind of dopant to another region having opposite doping. The diode device markers outline most diodes. This device marker is created with MDIODE and encloses the extents of the diode. The size of the diodes is generally defined according to the combination of the characteristic layers interacting with the described marker.

Rules for the extent of a capacitor (capacitor marking)

Note 1: A capacitor device must have its exterior defined. The exterior corresponds physically to the bottom plate of the mimc capacitor and to the extent of the mmchb and mmchp capacitors and can include the real capacity contributing area as well as a well-defined part of the connectors or surrounding material. The size of the capacitor is defined according to the combination of the characteristic layers.
These rules are to be flagged as warnings for mmchb and mmchp and low-accuracy mim capacitors. They are to be flagged as errors for matched mimc capacitors.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
WCAPA.1	WARNING : Minimum spacing of the exterior of the capacitor to unrelated METAL1.	3.00	µm	***	Warnings for mmchb/mmchp and low-accuracy mim capacitors
WCAPA.2	WARNING : Minimum spacing of the exterior of the capacitor to unrelated METAL2	3.00	µm	***	Warnings for mmchb/mmchp and low-accuracy mim capacitors
WCAPA.3	WARNING : Minimum spacing of the exterior of the capacitor to unrelated METAL3	3.00	µm	***	Warnings for mmchb/mmchp and low-accuracy mim capacitors
WCAPA.4	WARNING : Minimum spacing of the exterior of the capacitor to unrelated METAL4	3.00	µm	***	Warnings for mmchb/mmchp and low-accuracy mim capacitors
WCAPA.5	WARNING : Minimum spacing of the exterior of the capacitor to unrelated METAL5	3.00	µm	***	Warnings for mmchb/mmchp and low-accuracy mim capacitors
WCAPA.6	WARNING : Minimum spacing of the exterior of the capacitor to unrelated ACTIVE	3.00	µm	***	Warnings for mmchb/mmchp and low-accuracy mim capacitors
WCAPA.7	WARNING : Minimum spacing of the exterior of the capacitor to unrelated POLY	3.00	µm	***	Warnings for mmchb/mmchp and low-accuracy mim capacitors
CAPA.1	Minimum spacing of the exterior of the capacitor to unrelated METAL1	3.00	µm	*	Rules for matched MIMC capacitors related to MCAPA
CAPA.2	Minimum spacing of the exterior of the capacitor to unrelated METAL2	3.00	µm	*	Rules for matched MIMC capacitors related to MCAPA
CAPA.3	Minimum spacing of the exterior of the capacitor to unrelated METAL3	3.00	µm	*	Rules for matched MIMC capacitors related to MCAPA
CAPA.4	Minimum spacing of the exterior of the capacitor to unrelated METAL4	3.00	µm	*	Rules for matched MIMC capacitors related to MCAPA
CAPA.5	Minimum spacing of the exterior of the capacitor to unrelated METAL5	3.00	µm	*	Rules for matched MIMC capacitors related to MCAPA
CAPA.6	Minimum spacing of the exterior of the capacitor to unrelated ACTIVE	3.00	µm	*	Rules for matched MIMC capacitors related to MCAPA
CAPA.7	Minimum spacing of the exterior of the capacitor to unrelated POLY layer	3.00	µm	*	Rules for matched MIMC capacitors related to MCAPA

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

Rules for the MPNP layer (pnp device marking)

The pnp device marker must outline each pnp device. Without this device marker the pnp devices will not be recognized. This device marker is created with MPNP and encloses the extents of the pnp device. The size of the PNP device is defined according to the combination of the characteristic layers interacting with the described marker.

Rules for the MNPN layer (npn device marking)

The npn device marker must outline each npn device. Without this device marker the npn devices will not be recognized. This device marker is created with MNPN and encloses the extents of the npn device. The size of the NPN device is defined according to the combination of the characteristic layers interacting with the described marker.

Rules for the DREC layer (mos device marking)

The mos device marker outlines most devices. The only mos devices not needing a device marker are the standard enm and epm devices. The second two are the enmio and epmio devices, which have some special conditions that are checked using the marking layer (See Device Specific section on ENMIO/EPMIO). All other mos devices must have this device marker. This device marker is created with DREC and encloses the extents of the mos device. The size of the device is generally defined according to the combination of the characteristic layers interacting with the described marker.

Rules for the LREC marker:

The LREC marker layer can be used for identifying isolated high voltage n-epi pockets and high voltage devices within this pocket. The use is technology specific.

Rules for the shielding devices

Shielded devices are recognised by means of the device marking layers (mcapa,mres) and the device label. They require an implant enclosing the shape of floating passive elements in order to have a controlled impact on its linearity, noise coupling, matching, resistance depletion…

The implant must enclose the body of the passive element which is mostly NWELL in Nepi, but in some special cases it could be a Ptype implant (made with PWIMP and eventually a PFIELD) or with a generated pwell (without PFIELD)..

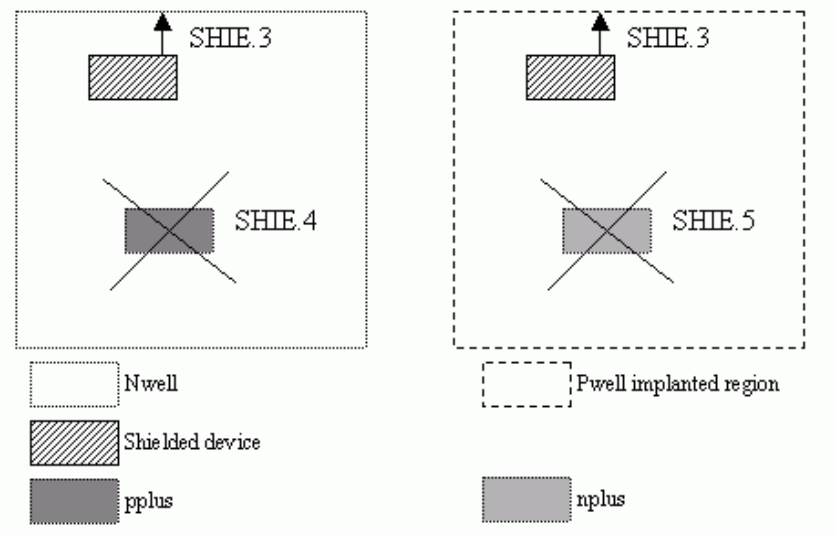
If a layer which can be recognised as shield does not enclose the whole body of the device, an error is signalled. It is not advised to merge a shield implant with the bulk of an active device, at least to allow a resistive decoupling when they are at the same potential: see also rules SHIE3/4.

The use of LOWACC has no direct relationship with the shielding of devices, hence it will not affect its handling by DRC and/or LVS.

In other words, shielding devices specifies the properties of the diffusion underlying the device, while LOWACC removes constraints on the metal routing to and across them.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
SHIE.3	Minimum shield implant enclosure of the body of the floating element (e.g. poly diode, poly resistor, capacitor), an enclosure must be present	1.50	µm	*	The body is: • the poly shape of the poly diode, the hipo resistor or the unsalicided N+/P+ poly resistors; • the area of the bottom plate of a capacitor enclosed by MCAPA
SHIE.4	P+ active area inside nwell shield diffusion is not allowed (to avoid parasitic field transistor)			*	
SHIE.5	N+ active area inside pwell shield diffusion is not allowed (to avoid parasitic field transistor)			*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)



Placement of metal capacitors, use of the mshield layer and recognition by LVS

This section applies to all metal capacitors: MIMC, bar metal capacitor and plate metal capacitor.

Only when metal capacitors are placed on top of a shield implant (nwell or pwell) AND surrounded by the mshield marker layer, they will be recognized by LVS as 3-terminal devices.

In all other cases, they will be treated as 2-terminal devices.

Ring Bond Pads

- Modification of bonding pads to ring bond pads is done for 5-layer metal products only.
- In order to comply with assembly requirements, it is necessary to generate ring bond pads by cutting away a section of metal from the central region of the bonding pad. This operation is automatically carried out during mask making, on all metal layers, except metal 5.
- The generation of ring bond pads can be blocked by the use of the layer **noring** (GDS layer 51); this is e.g. done for 5-layer metal engineering projects where it is anticipated that wafers will be processed with fewer layers of me tal.
- Rules for the use of the **noring** layer:

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
51.1	Minimum noring enclosure of pad opening	1.0	µm	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

Via generation on MIMC top plate metal

The MIMC layer represents the top plate of the metal capacitor: it is an intermediate metal layer deposited over the MTL2 and covered by MTL3. A matrix of VIA2 will automatically be generated on top of this intermediate metal plate to connect it to the MTL3 plate above.

The generation of VIA2 on the MIMC top plate can be suppressed by the use of layer **noviagen** (GDS 106). In this case, the vias have to be drawn. Specific layout rules apply (see the section on MIMC layout rules in this document).

Details of the generation procedure can be found in the Mask Generation Specifications.

C035U (0.35 Micron) Core CMOS Design Rules

Layout Rules and Device Specific Rules

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LAYOUT RULES: Introduction and General Requirements

Introduction

In this section, the process layout rules are presented.

- All dimensions given below are dimensions as drawn on the Interactive Graphical System (IGS).
- All dimensions are given in microns (µm), unless specified otherwise.
- Each layout rule is identified by a code in the following format: "GDS layer.x" where GDS layer refers to the GDS layer and x is a number, e.g. 13.1 refers to the first layout rule applicable for GDS layer 13 which corresponds to the polysilicon mask.
- For rules that are not mandatory, it is recommended that greater than minimum dimensions be used whenever possible.
- Each layout will be subject to a DRC (Design Rule Check) prior to final tape preparation.
- All drawings are for illustrative purposes only. They are not drawn to scale.
- All dimensions given in the layout rules are FINAL-ON-WAFER dimensions. During reticle fabrication proper sizing is applied in order to ensure that final dimensions are the same as drawn.
- This document is used in conjunction with 1000033 "Assembly Layout Rules". In the event of a disagreement between the two documents, please contact ON Semiconductor TRD.

General Layout Requirements

- The standard layout grid size is 0.05 µm, and the spot size is 0.25 µm @ 5X. For the layers poly (layer 13) and contact (layer 19) a 0.025 µm grid is to be used. These 2 layers are always fractured and ordered to reticle vendors with 0.125 µm spot size. The use of 0.025 µm layout design grid is restricted to those 2 layers. All edges of polygons must be on the grid.
- For all mask layers, rules are present to check that the drawing is on grid. Vertex points for a specific layer that are not on grid, are flagged.
- The chip dimensions in X- and Y- directions, defined as the distance from the centre of the scribe lane to the centre of the adjacent scribe lane, must be a multiple of 10 µm to allow compatibility with test- and assembly requirements.
- Apart from 0° and 90° layouts, only 45° layouts are allowed. Edges for a specific layer that are under different angles, are flagged.
- Transistor length is measured from drain to source as defined by the polysilicon mask. Transistor width is equal to the width centre line of the gate with one half the device channel length subtracted for each 90° bend.

- Silicided resistor length is measured by counting the numbers of squares from contact edge to contact edge. Non-silicided resistor length is measured by counting the number of squares under SIPROT (GDS Layer 18). A 90° bend is counted as one half square.

Product Identification

Circuit Identification

A circuit identification number/name must be assigned by ON Semiconductor for every device. It must always be present in the circuit and appear only once. It may appear in any metal level provided it is present in the top metal level. It must be DRC clean. A region no smaller than 150µm x 25µm must be reserved for placement of identification. Additional identifications of any sort are allowed provided these are DRC clean and present in METAL1 only.

ON SEMICONDUCTOR Logo

ON SEMICONDUCTOR logo must always be present in the circuit unless otherwise forbidden. It is preferably placed near the circuit identification and must not appear more than once. It is placed in METAL1 only. A region no smaller than 100µm x 50µm must be reserved for placement of logo. Additional logo of any sort are allowed provided these are DRC clean and present in METAL1 only.

Mask and Iteration Numbering

- Every circuit must contain the correct mask numbering on each layer, including the automatically generated layers (e.g. pwell, nplus) but with the exception of the passivation layer (layer 31). The mask number is wafer fab dependent.
- On every layer, including the non-drawn layers (e.g. pwell, nplus) but with the exception of the passivation layer (layer 31), the iteration number must be present. All layer iterations for a completely new design will be "A".
- Mask numbers and iteration numbers must not be superimposed. They will be covered by the nogen layer (layer 61). They can be combined with the CD structures (see section on CD structures).
- To ensure process compatibility the following rules apply for the letters:
  - poly pad must be drawn under contact letters
  - contact letters to be covered by metal 1
  - METAL(i) to be drawn under VIA(i) for i = 1 → 4
  - VIA(i) to be covered by METAL(i+1) for i = 1 → 4
  - All related enclosures to be 1.0 µm minimum.
- Layer- and iteration numberings shall not introduce any layout rule violations; only 45° angles are allowed.

CD structures

- Every circuit must contain the CD structures on each layer, including the automatically generated layers (e.g. pwell, nplus) but with the exception of the passivation layer (layer 31).
- The CD structures must not be superimposed. They will be covered by the nogen layer (layer 61).
- To ensure process compatibility the following rules apply for the CD structures:
  - active pad must be drawn under contact CD bar
  - contact CD bar to be covered by metal 1
  - METAL(i) to be drawn under VIA(i) for i = 1 → 4
  - VIA(i) to be covered by METAL(i+1) for i = 1 → 4
  - All related enclosures to be 1.0 µm minimum.
- CD structures shall not introduce any layout rule violations; only 45° angles are allowed.

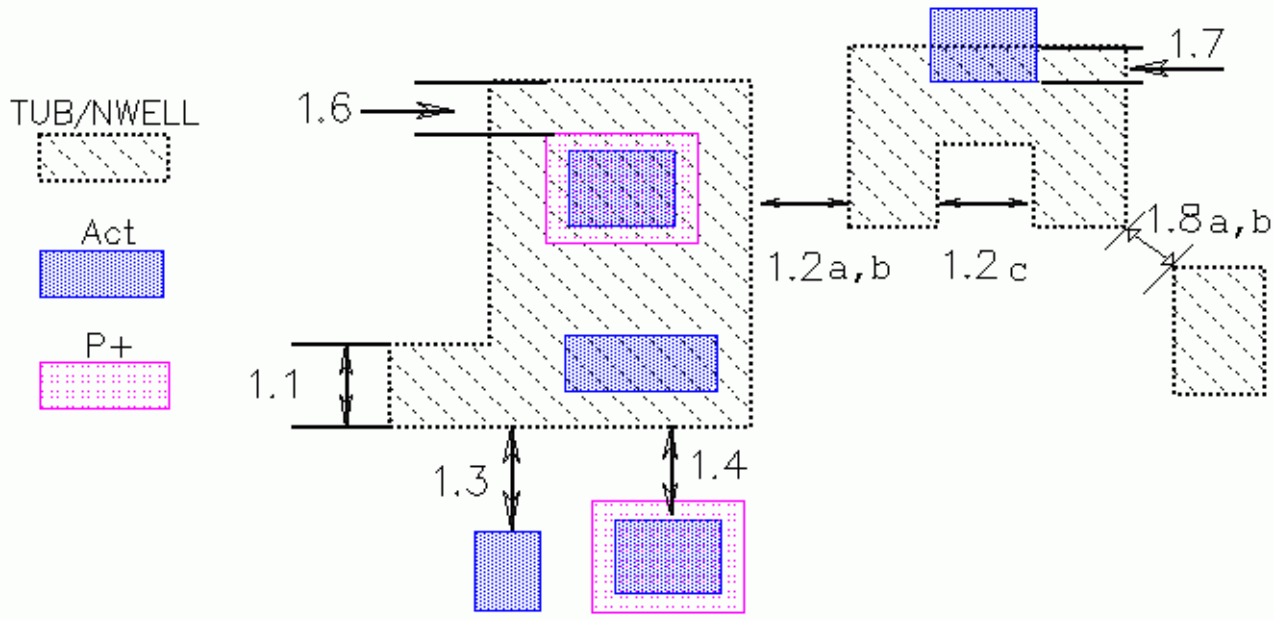
Diagonal Layout Rules

The layout rules in this chapter are valid for layout of lines in X and Y directions, and 45 degree lines.

For layers with positive sizing such as e.g. active area, the way the sizing is done during final tape preparation may lead to a spacing on the mask smaller at 45 degrees than in X or Y direction. Specific layout rules apply for active area and n-well to prevent these small spacings at 45 degrees.

C035U (0.35 Micron) N-WELL Layout Rules

Layer/level #1



Note 1: N-WELL (GDS layer 1) is used to define regions that will be implanted with n-well implant. The presence of N-WELL layer also implies the absence of p-well implant.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
1.1	Minimum n-well width	1.70	µm	*	
1.2a	Minimum n-well spacing - at different potential	2.10	µm	*	
1.2b	Minimum n-well spacing - at same potential (merge if less)	1.40	µm	*	
1.2c	Minimum n-well spacing - on same geometry	1.40	µm	*	
1.3	Minimum n-well spacing to n+ active area	1.00	µm	*	
1.4	Minimum n-well spacing to p-well strap	0.50	µm	*	
1.6	Minimum n-well enclosure of p+ active area	1.00	µm	*	
1.7	A n-well strap is allowed to cross the n-well boundary; minimum n-well intersection with n-well strap if n-well strap crosses the n-well boundary	0.70	µm	*	
1.8a	Minimum n-well spacing after 0.20 µm sizing (diagonal rule) - at different potential	1.70	µm	*	

1.8b	Minimum n-well spacing after 0.20 µm sizing (diagonal rule) - at same potential (merge if less)	1.00	µm	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

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C035U (0.35 Micron) RNWELL Layout Rules

Layer/level #112

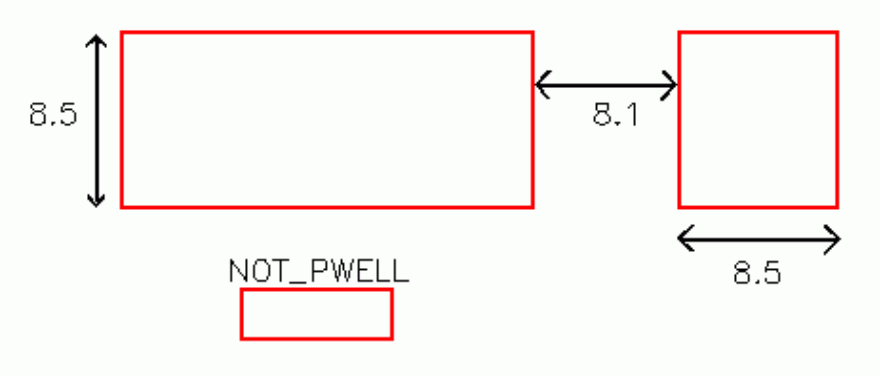
Note 1: All GDS data on layer RNWELL (GDS 112) suffers from being at the same potential unless properly isolated in C035U family. RNWELL is kept as a legacy layer to allow porting of C035M layout into C035U. A warning is issued to alert the user of a possible short if the n-well resistor in C035M is not converted to an appropriate resistor in C035U with proper isolation.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
112.0	WARNING: DATA ARE PRESENT ON GDS LAYER 112 – RNWELL; CHECK TECHNOLOGY SPECIFIC LRM FOR PORTING OF N-WELL RESISTORS AND PROCESS TECHNOLOGY SPECIFIC SHEET RESISTANCE			*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

C035U (0.35 Micron) NOT_PWELL Layout Rules

Layer/level #8



Note 1: NOT_PWELL (GDS layer 8) allows the creation of regions in a layout that are not implanted by p-well implant. Typically p-well implanted region is an inverse of n-well implanted region, and hence only n-well drawing is required in C035U family. Only a few devices in C035U family require use of NOT_PWELL for proper device operation.

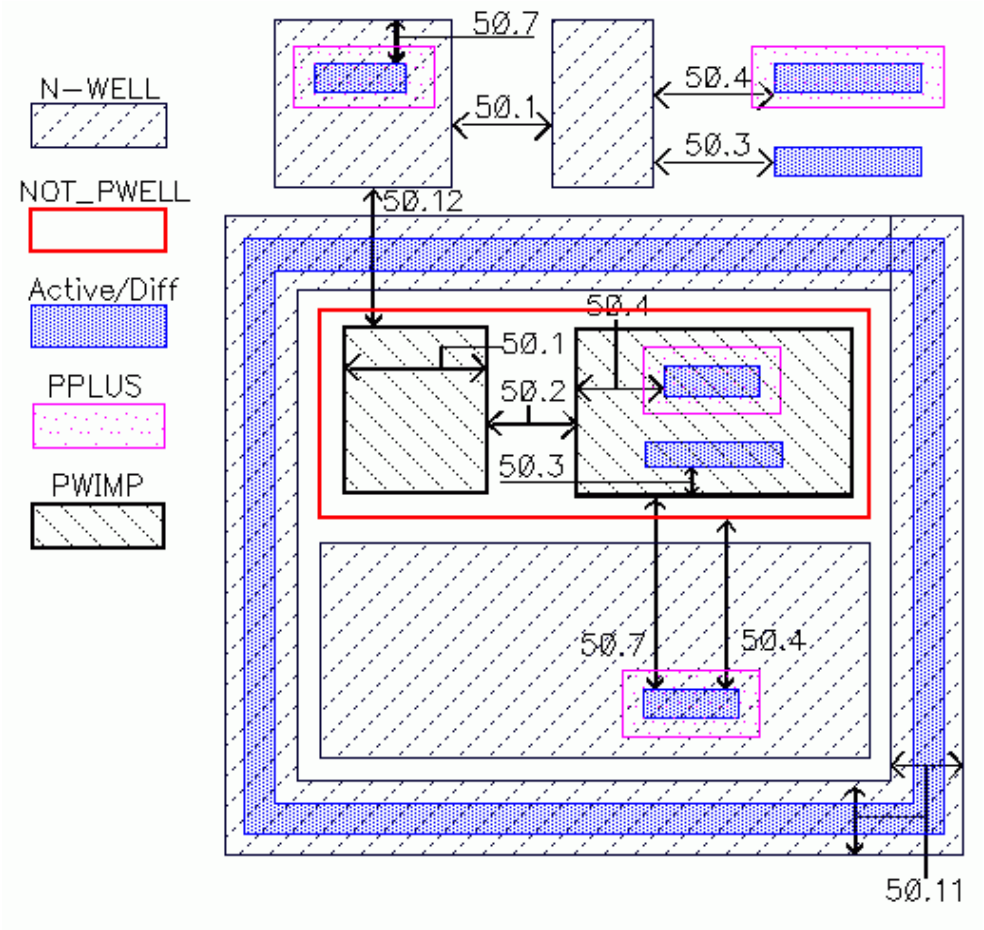
In the event that a floating p-well region is used to build a specific device, PWIMP (GDS layer 50) is used in conjunction with NOT_PWELL. A minimal set of technology independent rules for NOT_PWELL are given in the table below, with a reference to corresponding rules in other parts of this manual. Please refer to technology specific rules for proper device construction.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
8.1	Minimum NOT_PWELL spacing	1.40	µm	*	1.2, 50.1
8.5	Minimum NOT_PWELL width	1.70	µm	*	1.1, 50.2

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

C035U (0.35 Micron) PWIMP Layout Rules

Layer/level #50



Note 1: Used in conjunction with NOT_PWELL, PWIMP (GDS layer 50) may be used to construct a floating P-WELL. A floating P-WELL is defined as a region that is implanted with P-WELL species and is electronically isolated from other regions with P-WELL implant.

A floating P-WELL may be used to construct certain specific devices. In the following set of rules, P-WELL implanted region is defined as one of the following:

- Regions where N-WELL is not drawn and NOT_PWELL is not drawn.
- Regions where NOT_PWELL and PWIMP is drawn. The implanted region is the area where PWIMP is enclosed inside of NOT_PWELL.

In a logical construction, P-WELL implanted regions are given by: NOT(N-WELL OR NOT_PWELL) OR (NOT_PWELL AND PWIMP)

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
50.1	Minimum Pwell implanted region width	1.40	µm	*	1.2
50.2	Minimum Pwell implanted region spacing (merge if less)	1.70	µm	*	1.1
50.3	Minimum Pwell implanted region enclosure of N+ ACTIVE	1.00		*	Except DMOS channel area and NWELL straps that cross NWELL/Pwell implanted region boundary.
50.4	Minimum Pwell implanted region enclosure of P+ ACTIVE	0.50	µm	*	1.4
50.7	Minimum Pwell implanted region spacing to P+ ACTIVE	1.00	µm	*	1.6
50.11	Each isolated Pwell implanted region should be surrounded by a N+ or N+/NWELL guard ring			*	
50.12	Minimum Pwell implanted region spacing to NWELL or RNWELL. NWELL or RNWELL must not enclose PWIMP	0.00		*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

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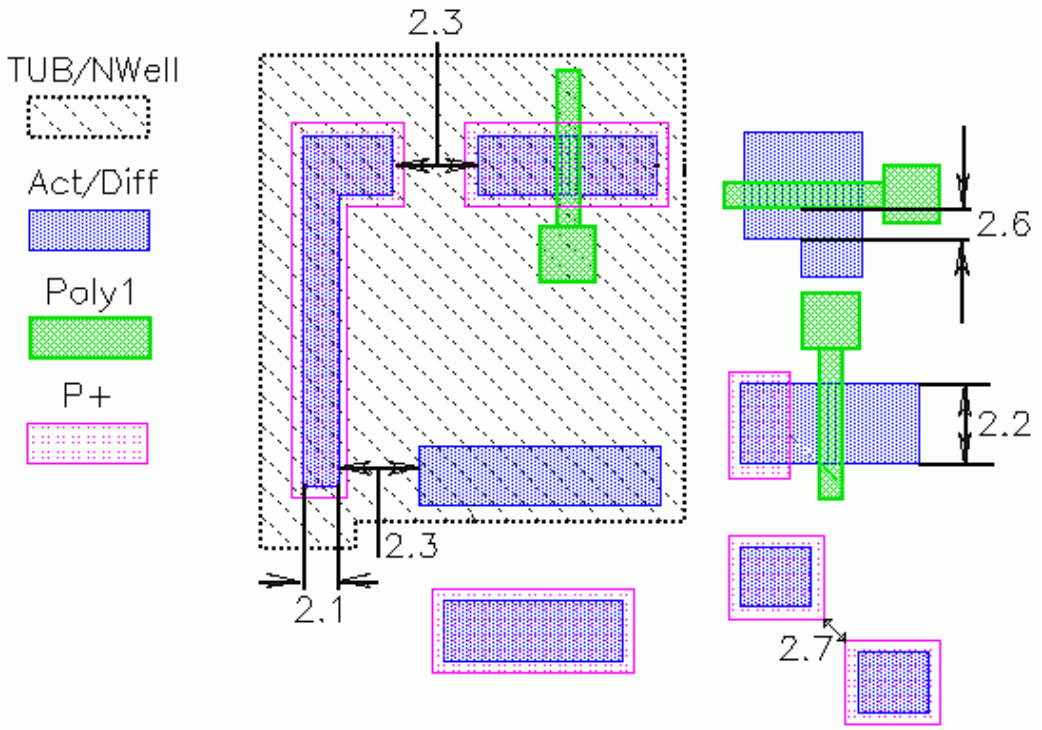
C035U (0.35 Micron) ACTIVE Layout Rules

Layer/level #2



Note 1: ACTIVE (GDS layer 2) is used to define regions that form MOS devices, diffused resistors, diffused interconnect and well straps, etc. The use of ACTIVE layer is not limited to this list.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
2.1	Minimum active area width for interconnect, resistors and straps	0.40	µm	*	
2.2	Minimum active area width for transistors	0.50	µm	*	
2.3	Minimum active area spacing	0.60	µm	*	Abutting (touching) allowed if at same potential (see also 18.8)
2.6	Minimum active area enclosure of polysilicon	0.65	µm	*	Only applies to source drain of MOS devices
2.7	Minimum active area spacing after sizing by 0.1 um (to cover diagonal active area spacing)	0.40	µm	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

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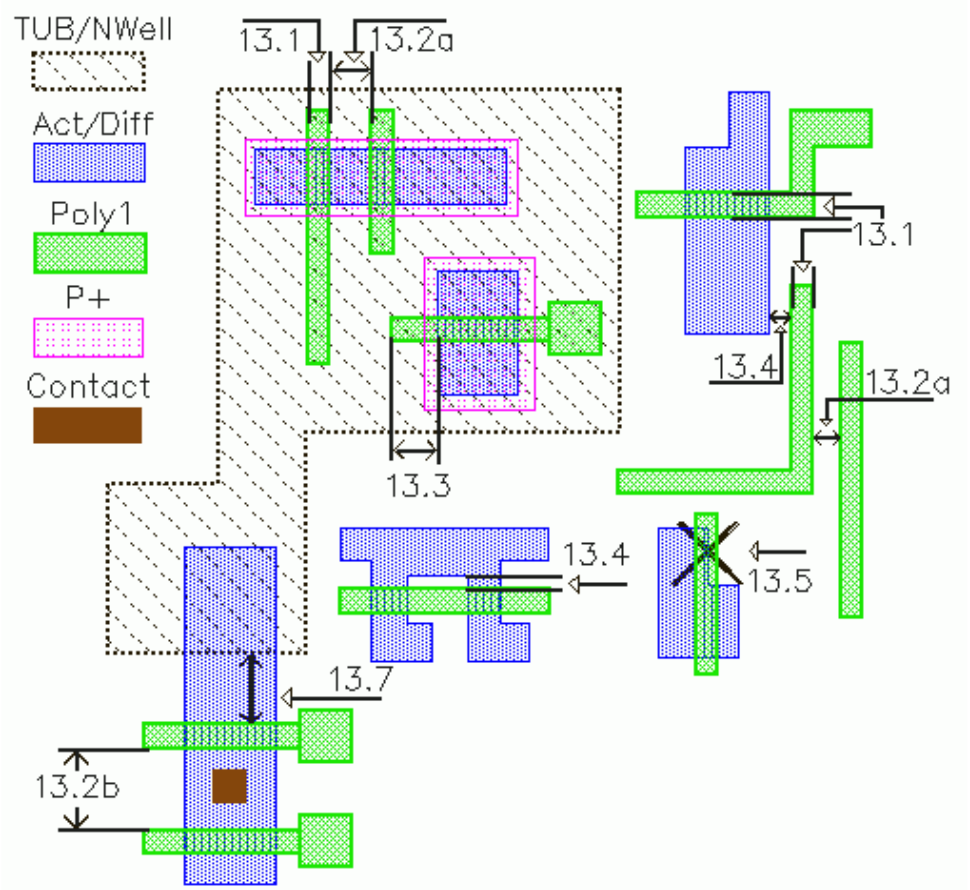
C035U (0.35 Micron) POLYSILICON Layout Rules

Layer/level #13



Note 1: POLYSILICON (GDS layer 13) is used to define MOS gates, resistors and interconnect, etc. The use of POLYSILICON is not limited to this list.

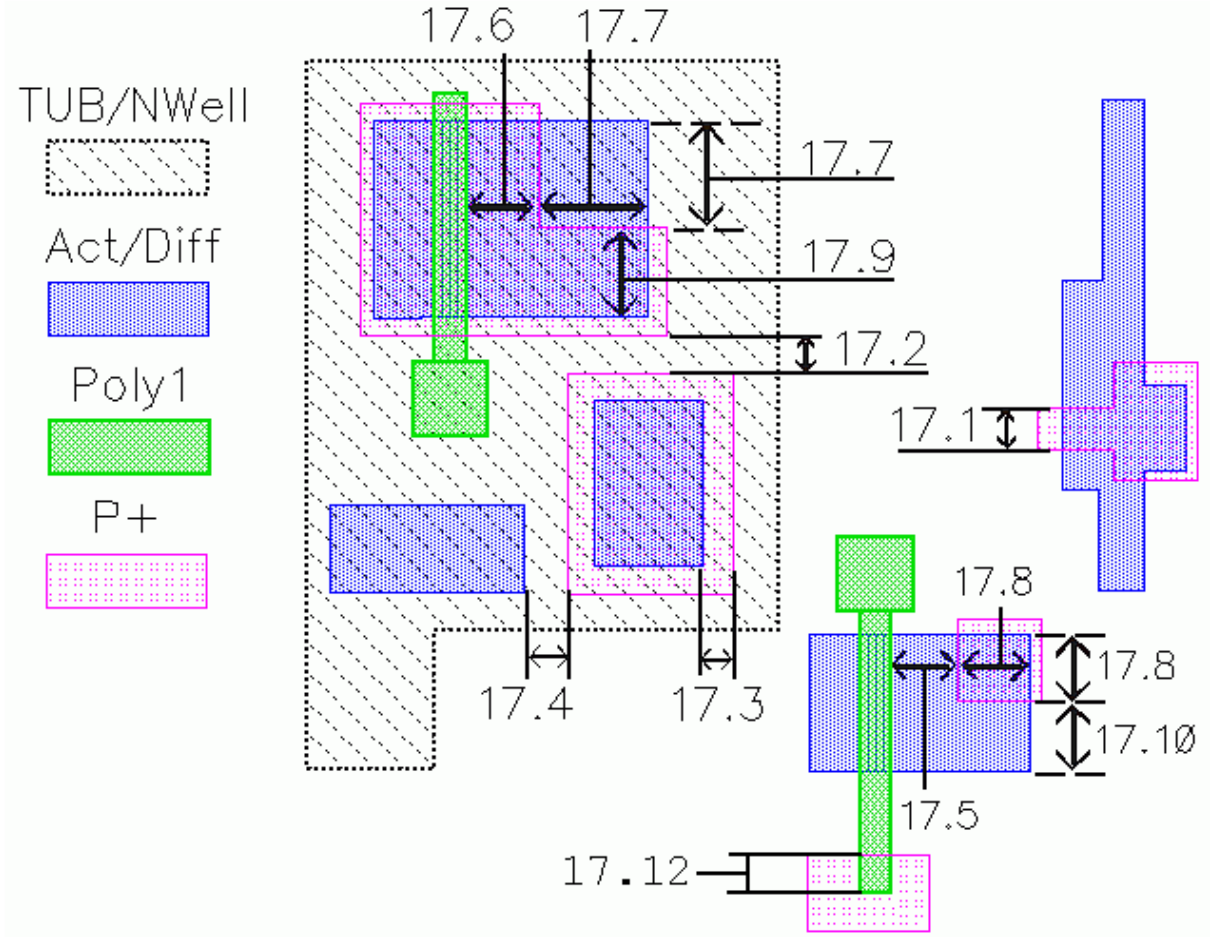
Rule Name	Rule Description	Rule	Units	Rule Type	Notes
13.1	Minimum polysilicon width (-interconnect, -transistors)	0.35	µm	*	
13.2a	Minimum polysilicon spacing (-on field oxide, -on active area)	0.50	µm	*	
13.2b	Minimum polysilicon spacing on active area when the active area between the polysilicon lines is contacted	0.65	µm	*	
13.3	Minimum polysilicon extension beyond gate, on field oxide (= endcap)	0.40	µm	*	
13.4	Minimum polysilicon spacing to active area	0.25	µm	*	

13.5	Polysilicon gate running over active area corner is not allowed			*	Exception for LNNDM15 and LFNDM14
13.7	Minimum polysilicon spacing to n-well, on active, in case this active crosses the n-well boundary	1.00	µm	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

C035U (0.35 Micron) PPLUS Layout Rules

Layer/level #17



Note 1: PPLUS (GDS layer 17) is used to define areas implanted by PPLUS implant. PPLUS implant is used to form PMOS source/drain, PPLUS ACTIVE and POLYSILICON resistors, and p-well straps. PPLUS implant uses are not limited to this list. The presence of PPLUS layer also implies absence of NPLUS implant.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
17.1	Minimum pplus width	0.50	µm	*	Exception for ZZD tip area (see ZENER ZAP DIODE section for description of tip area)
17.2	Minimum pplus spacing	0.50	µm	*	
17.3	Minimum pplus enclosure of p+ active area	0.30	µm	*	Exception for CLD and ZZD tip area (see ZENER ZAP DIODE section for description of tip area)
17.4	Minimum pplus spacing to n+ active area	0.30	µm	*	Exception for ZZD tip area (see ZENER ZAP DIODE section for description of tip area)

17.5	Minimum NMOS polysilicon gate spacing to p+ active area of abutting p-well strap	0.80	µm	*	
17.6	Minimum PMOS polysilicon gate spacing to n+ active area of abutting n-well strap	0.80	µm	*	
17.7	Minimum n+ active area width of abutting n-well strap	0.50	µm	*	
17.8	Minimum p+ active area width of abutting p-well strap	0.50	µm	*	
17.9	Minimum p+ active area width	0.40	µm	*	
17.10	Minimum n+ active area width	0.40	µm	*	Exception for ZZD tip area (see ZENER ZAP DIODE section for description of tip area)
17.11	WARNING: each p+ active area covered by layer nogen must be covered either by nldd (GDS layer 14) or nplus (GDS layer 16)			*	Exception for ZZD tip area (see ZENER ZAP DIODE section for description of tip area)
17.12	Minimum PPLUS intersection with a POLY gate, if any is present	0.30	µm	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

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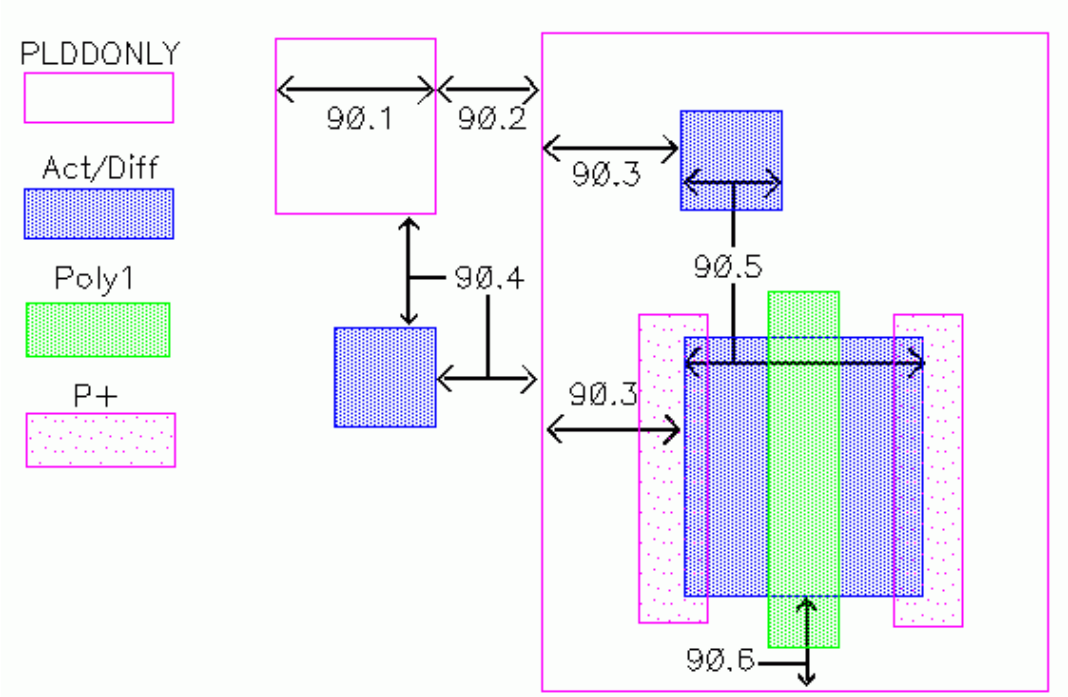
C035U (0.35 Micron) PLDDONLY Layout Rules

Layer/level #90



Note 1: PLDDONLY (GDS layer 90) if drawn results in at least PLDD implant in that region. Presence of PLDDONLY implies blocking of NPLUS and NLDD implants. In certain C035U technologies PLDDONLY must be drawn in a region covered with NOGEN (GDS layer 61) to implant the area with PLDD.

Currently ZZD and UZZD in C035U family use this layer. The results of drawing this layer are technology dependent. User must gather more information before using the layer outside of ZZD and UZZD devices. There is currently no need to draw this layer outside of this limited scope.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
90.1	Minimum PLDDONLY width	0.50	µm	*	
90.2	Minimum PLDDONLY spacing	0.50	µm	*	
90.3	Minimum PLDDONLY enclosure of ACTIVE	0.30	µm	*	Exception for ZZD tip area (see ZENER ZAP DIODE section for description of tip area)
90.4	Minimum PLDDONLY spacing to N+ ACTIVE	0.30	µm	*	Exception for ZZD tip area (see ZENER ZAP DIODE section for description of tip area)
90.5	Minimum width of active area enclosed in PLDDONLY	0.40	µm	*	
90.6	Minimum PLDDONLY overlap on POLY gate	0.30	µm	*	

90.7	WARNING: each PLDDONLY inside NOGEN must be covered by NLDD (#14) and NPLUS (#16) to stop respectively Nldd and Nplus implant			*	Exception for ZZD tip area (see ZENER ZAP DIODE section for description of tip area)

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

(Confidential)
DES-0005 Rev: 11.0, 05-Oct-2010

C035U (0.35 Micron) PLDDPROT Layout Rules

Layer/level #47

Note 1: In C035U, PLDD implant is a copy of PPLUS implant. PLDDPROT (GDS layer 47) is used to define regions that will not be implanted by PLDD implant. Certain technologies require such a flexibility and hence it is retained in the manual.

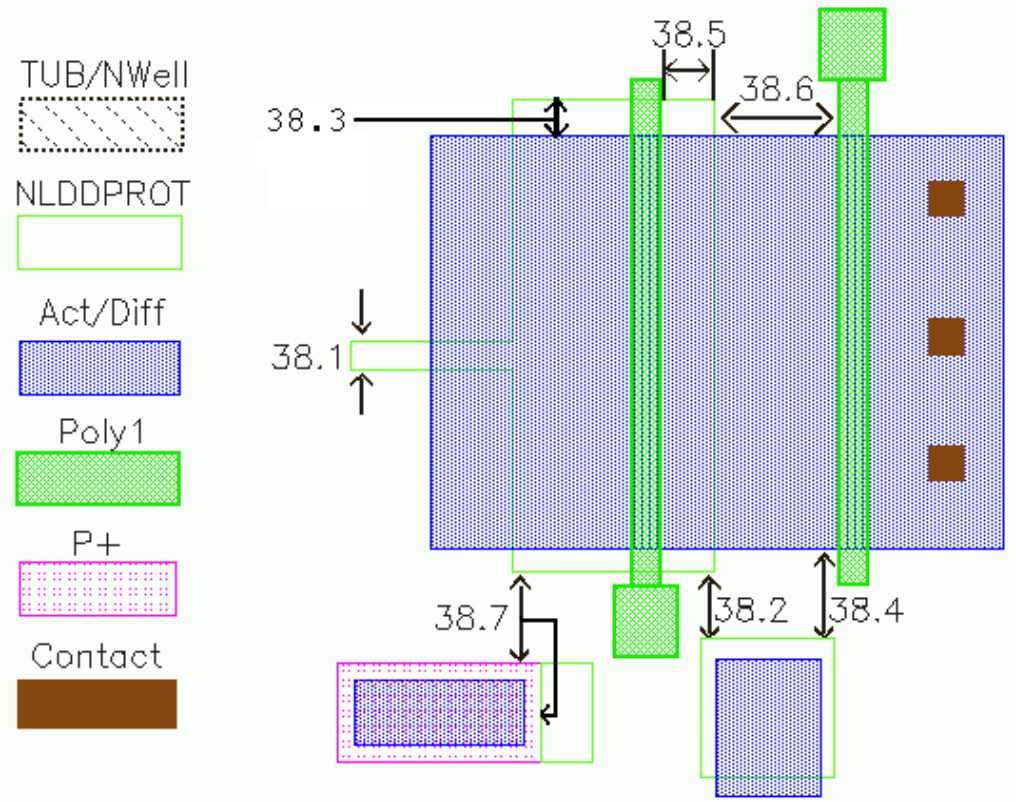
PLDDPROT has no effect if drawn outside of PPLUS region. PLDDPROT supersedes PLDDONLY if drawn in the same region.

PLDDPROT is not required by any devices in C035U base at this time.

(Confidential)
DES-0005 Rev: 11.0, 05-Oct-2010

C035U (0.35 Micron) NLDDPROT Layout Rules

Layer/level #38



Note 1: Typically all areas not defined as PPLUS are implanted with NLDD and NPLUS implants. NLDDPROT (GDS layer 38) is used to block NLDD implant from such a region. Typical application is an NMOS clamping device for ESD protection in the I/O cells. NPLUS implant is not blocked in such a region.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
w38	WARNING : NLDDPROT cannot be used inside NOGEN, where only NLDD(#14) can be used for the same purpose			*	
38.1	Minimum nlddprotect width	0.50	µm	*	
38.2	Minimum nlddprotect spacing	0.50	µm	*	
38.3	Minimum nlddprotect extension on n+ active area	0.30	µm	*	
38.4	Minimum nlddprotect spacing to n+ active area	0.30	µm	*	
38.5	Minimum nlddprotect extension on polysilicon on active area (gate area) if any extension is present	0.70	µm	*	

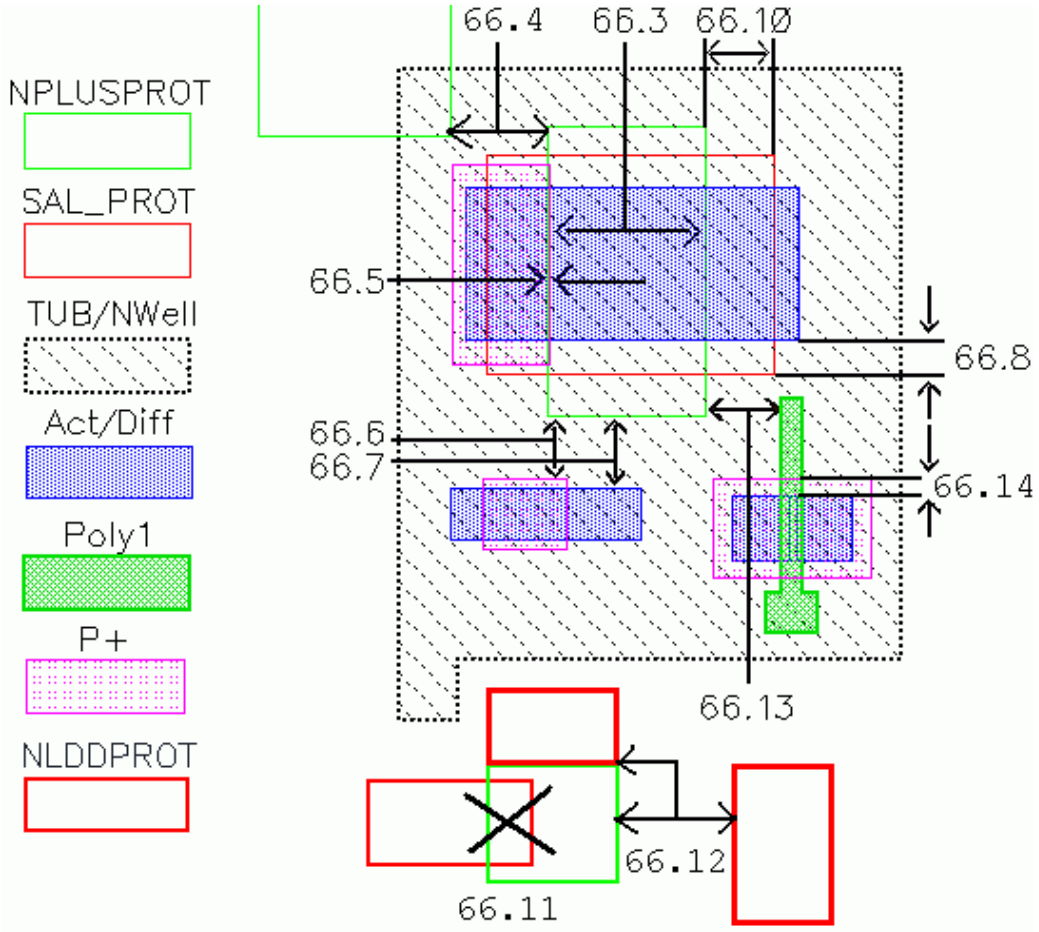
38.6	Minimum nlddprotect spacing to polysilicon gate on active area (distance between nlddprotect on active to transistor gate with LDD)	0.70	µm	*	Only in the event of an NMOS cascoded with an NLDD protected NMOS with no contacts in the shared active area.
38.7	Minimum nlddprotect spacing to pplus, if spacing is present. Touching is allowed	0.50	µm	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

(Confidential)
DES-0005 Rev: 11.0, 05-Oct-2010

C035U (0.35 Micron) NPLUSPROT Layout Rules

Layer/level #66



Note 1: Typically NPLUS and NLDD implanted regions are a copy of each other. In the event that a device construction requires an area to be implanted with NLDD without NPLUS implant, the layer NPLUSPROT (GDS layer 66) is used. Typical application is PPLUS/NLDD junction diodes for ESD protection.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
w66	WARNING : NPLUSPROT cannot be used inside NOGEN, where only NPLUS(#16) can be used for the same purpose			*	
66.3	Minimum nplusprotect width	1.20	µm	*	
66.4	Minimum nplusprotect spacing	0.80	µm	*	
66.5	Fixed nplusprotect spacing to pplus of related P+/NLDD diode	0.00	µm	*	Exception for ZZD

66.6	Minimum nplusprotect spacing to pplus of unrelated device, if any is present. Touching is allowed.	0.55	µm	*	
66.7	Minimum nplusprotect spacing to active	0.40	µm	*	
66.8	Minimum nplusprotect extension on active	0.50	µm	*	
66.9	nplusprotect on active must be covered by sal_prot			*	
66.10	Minimum sal_prot extension on nplusprotect (on active)	0.40	µm	*	
66.11	nplusprotect must not intersect nlddprot			*	All edges coincident is allowed
66.12	Minimum nplusprotect spacing to nlddprot, on active, if any is present. Touching is allowed	0.40	µm	*	Exception for PWARNW
66.13	Minimum nplusprotect spacing to polysilicon; overlap is forbidden except for cases covered by rule 66.14	0.40	µm	*	Exception for POLYD
66.14	Minimum nplusprot overlap on the edge of polysilicon gate, like for drain/source of extended MOS	0.30	µm	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

(Confidential)
DES-0005 Rev: 11.0, 05-Oct-2010

C035U (0.35 Micron) NPLUS Layout Rules

Layer/level #16

Note 1: As a general rule NPLUS (GDS layer 16) must never be drawn. It defines areas where NPLUS implant does not occur. Typically it is generated from PPLUS and NPLUSPROT layers. Certain specific devices require drawing of NPLUS, in which case it is completely enclosed by NOGEN (GDS layer 61).

If N+ implant needs to be blocked, use NPLUSPROT layer.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
w16	WARNING : NPLUS is drawn only inside NOGEN where it defines the N+ should be stopped			*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

(Confidential)
DES-0005 Rev: 11.0, 05-Oct-2010

C035U (0.35 Micron) NLDD Layout Rules

Layer/level #14

Note 1: As a general rule NLDD (GDS layer 14) must never be drawn. It defines areas where NLDD implant does not occur. Typically it is generated from PPLUS and NLDDPROT layers. Certain specific devices require drawing of NLDD, in which case it is completely enclosed by NOGEN (GDS layer 61).

If NLDD implant needs to be blocked, use NLDDPROT layer.

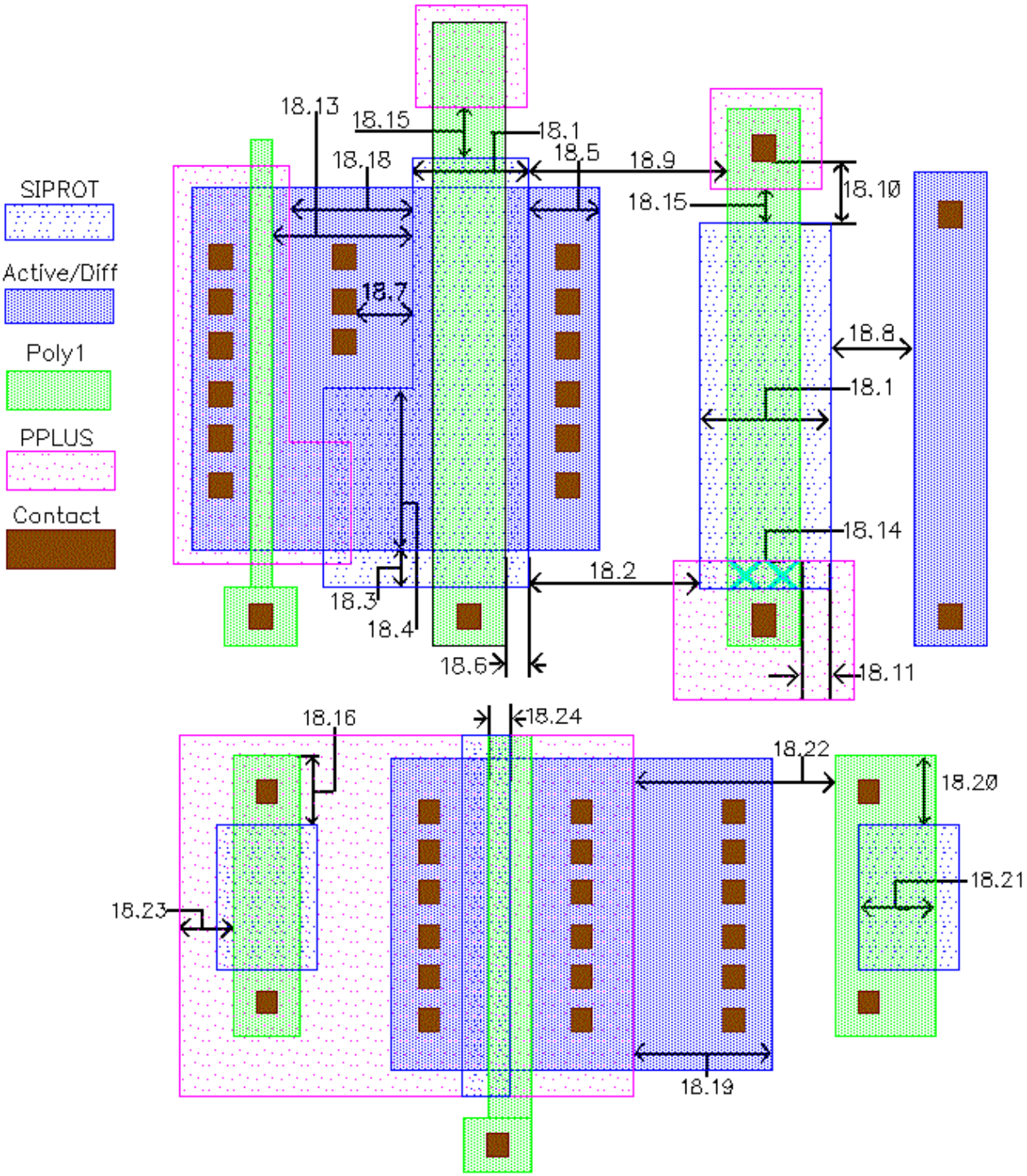
Rule Name	Rule Description	Rule	Units	Rule Type	Notes
w14	WARNING : NLDD is drawn only inside NOGEN it defines the NLDD regions should be stopped			*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

(Confidential)
DES-0005 Rev: 11.0, 05-Oct-2010

C035U (0.35 Micron) SIPROT Layout Rules

Layer/level #18



Note 1: To reduce resistance of polysilicon and/or diffusion active areas or to bridge both terminals of a diode the process of silicidation is used. In C035U family, all areas of the chip are silicided unless covered

by SIPROT (GDS layer 18). Typical applications include non-silicided I/O transistors, non-silicided diffusion or poly resistors and Zener diodes.

For a non-silicided resistor, the dimensions of SIPROT perpendicular to the current flow determines the length of the resistor. Ends of the resistor used to electrically contact are always silicided. All NPLUS/PPLUS diodes must always be silicided with the exception of Zener Zap Diode (ZZD) for OTP applications.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
18.1	Minimum siprot width	0.90	µm	*	
18.2	Minimum siprot spacing	0.70	µm	*	
18.3	Minimum siprot extension on active area for non-salicided source/drain	0.30	µm	*	
18.4	Minimum siprot intersection with active area for non-salicided source/drain	0.40	µm	*	
18.5	Minimum active area extension on siprot	0.55	µm	*	
18.6	Minimum siprot extension on polysilicon on active area	1.20	µm	*	
18.7	Minimum siprot spacing to contact on active area	0.35	µm	*	
18.8	Minimum siprot spacing to active area	0.40	µm	*	Exception for ZZD
18.9	Minimum siprot spacing to polysilicon on field oxide	0.40	µm	*	
18.10	Minimum siprot spacing to contact on polysilicon for resistors	0.35	µm	*	
18.11	Minimum siprot extension on polysilicon on field	0.30	µm	*	
18.13	Minimum siprot spacing to polysilicon gate, on active area (= non-salicided active area spacing to salicided active gate)	0.65	µm	*	
18.14	Non-salicided polysilicon must not be crossed by pplus boundary			*	Exception for HIPOR and POLYD
18.15	Minimum siprot spacing to p+ edge created by p+ and polysilicon crossing	0.80	µm	*	
18.16	Minimum p+ polysilicon extension on siprot	0.80	µm	*	
18.18	Minimum siprot spacing to p+ active area, on active (abutting n+/p+) – Abutting (touching) active areas are allowed if they are at the same potential	0.80	µm	*	
18.19	Minimum p+ active area extension on siprot (abutting n+/p+)	0.80	µm	*	
18.20	Minimum polysilicon extension on siprot	0.55	µm	*	

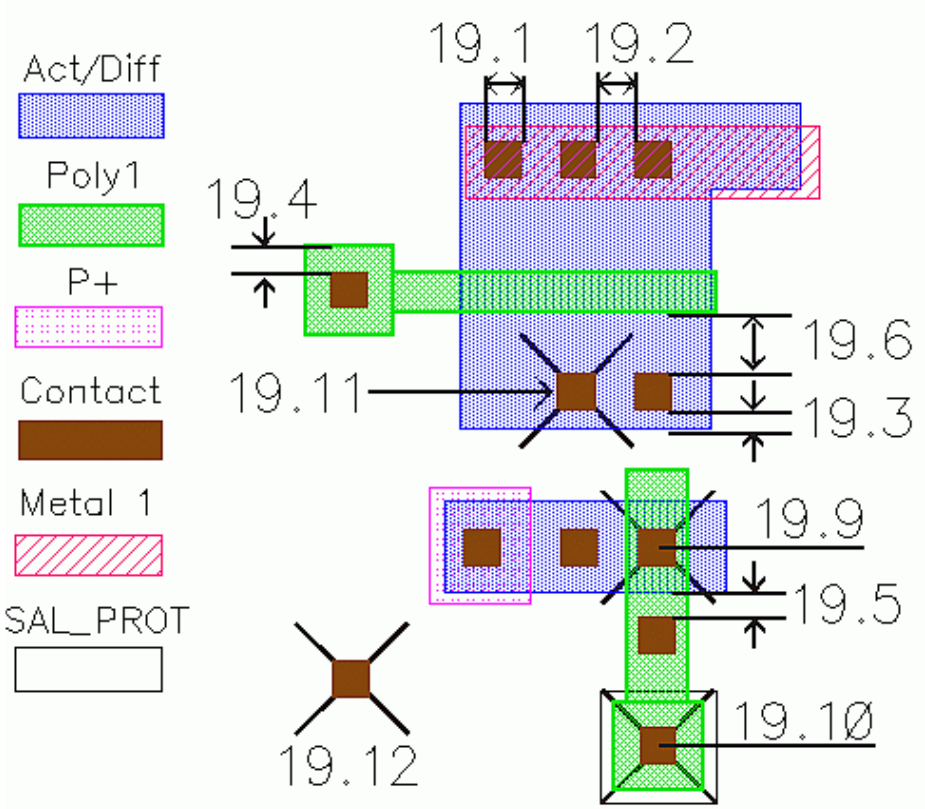
18.21	Minimum siprot intersection of polysilicon for non-salicided polisilicon on field oxide	0.30	µm	*	
18.22	Minimum pplus spacing to non-salicided polysilicon	0.35	µm	*	
18.23	Minimum pplus enclosure of non-salicided polysilicon	0.35	µm	*	
18.24	When present and intersecting (not enclosing), fixed SIPROT intersection with POLY gate	0.30	µm	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

(Confidential)
DES-0005 Rev: 11.0, 05-Oct-2010

C035U (0.35 Micron) CONTACT Layout Rules

Layer/level #19



Note 1: CONTACT (GDS layer 19) is used to establish an electrical connection from METAL1 to POLYSILICON or ACTIVE. A CONTACT can be placed at a PPLUS/NPLUS junction if the junction is not covered by SIPROT.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
19.1	Fixed contact dimensions (width = length)	0.40	µm	*	
19.2	Minimum contact spacing	0.40	µm	*	
19.3	Minimum active area enclosure of contact	0.20	µm	*	
19.4	Minimum polysilicon enclosure of contact	0.20	µm	*	
19.5	Minimum polysilicon contact spacing to active area	0.35	µm	*	
19.6	Minimum active area contact spacing to polysilicon gate	0.30	µm	*	
19.9	Contacts on polysilicon over active area are not allowed			*	
19.10	Contacts inside siprot are not allowed			*	

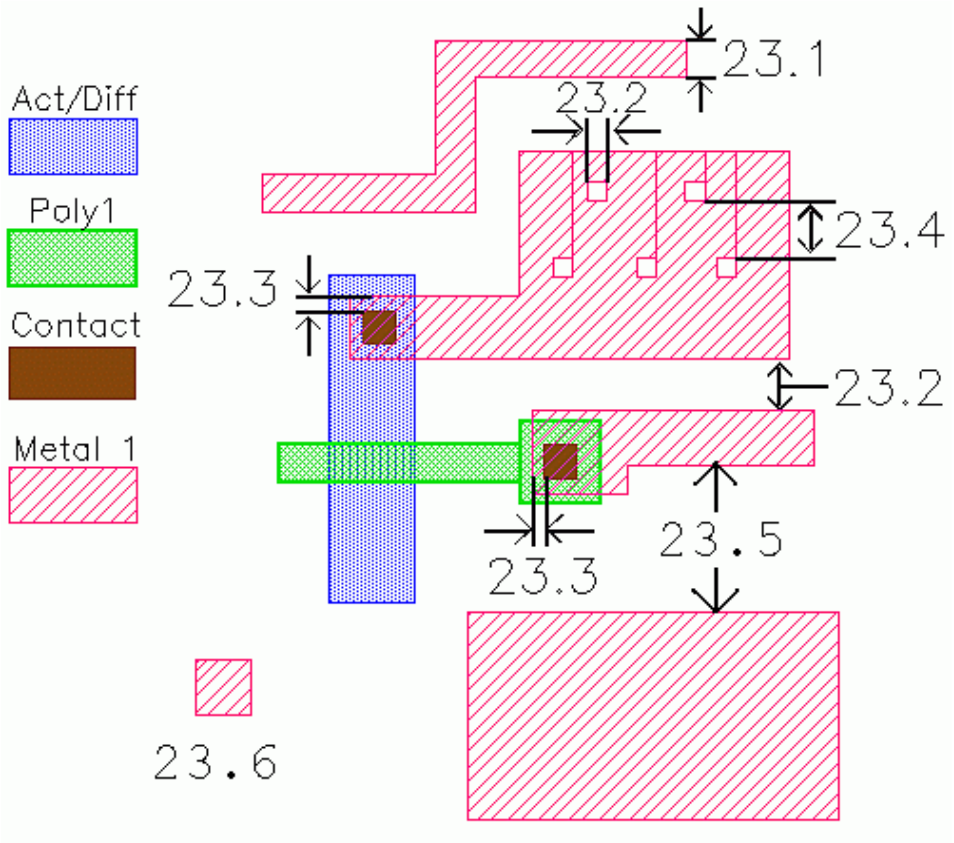
19.11	All contacts must be covered by metal1			*	
19.12	All contacts must be on active area or on poly			*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

(Confidential)
DES-0005 Rev: 11.0, 05-Oct-2010

C035U (0.35 Micron) METAL 1 Layout Rules

Layer/level #23



Note 1: METAL1 (GDS layer 23) provides electrical connectivity to and from CONTACT and VIA1 layers.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
23.1	Minimum metal 1 width	0.50	µm	*	
23.2	Minimum metal 1 spacing	0.50	µm	*	
23.3	Minimum metal 1 enclosure of contact	0.10	µm	*	
23.4	Maximum metal 1 width simultaneously in both directions	30.00	µm	*	If any dimension of METAL1 exceeds 30µm, sections of METAL1 can be cut to introduce holes such that 23.4 holds. The holes must obey all METAL1 design rules and should be staggered. The only exception to 23.4 is MMCHB and MMCHP capacitors.

23.5	Minimum wide metal 1 spacing (metal 1 width > 10 um) to any metal 1	1.00	µm	*	
23.6	Minimum metal 1 area	0.36	µm²	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

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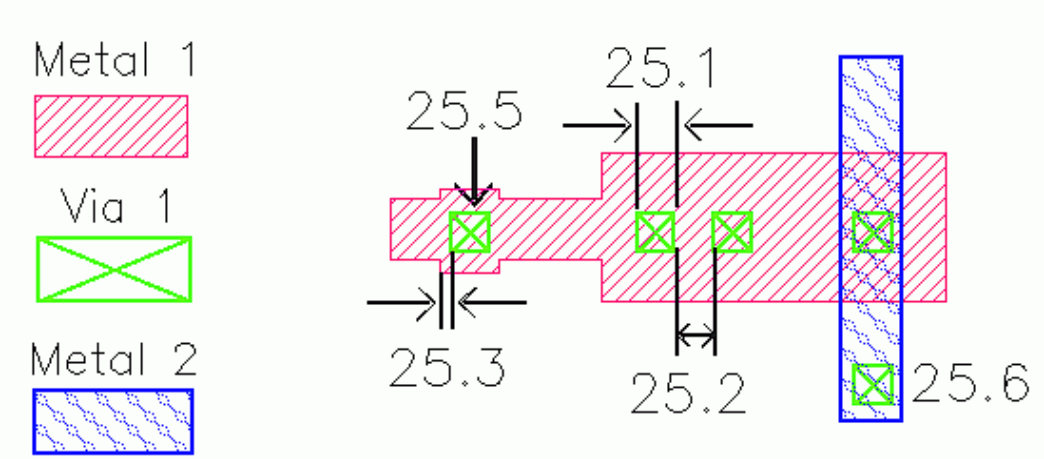
C035U (0.35 Micron) VIA 1 Layout Rules

Layer/level #25



Note 1: VIA1 (GDS layer 25) provides electrical connectivity to and from METAL1 and METAL2 layers. VIA1 may be stacked over CONTACT.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
25.1	Fixed via 1 dimensions (width = length)	0.40	µm	*	
25.2	Minimum via 1 spacing	0.50	µm	*	
25.3	Minimum metal 1 enclosure of via 1	0.15	µm	*	
25.5	All via 1 must have underlying metal 1			*	
25.6	All via 1 must be covered by metal 2			*	
25.7	Lonely via 1 needs redundancy, extra metal or addition of dummy metal on lonely vias			*	For lonely vias, please refer to LONELY VIA RULES section of this document

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

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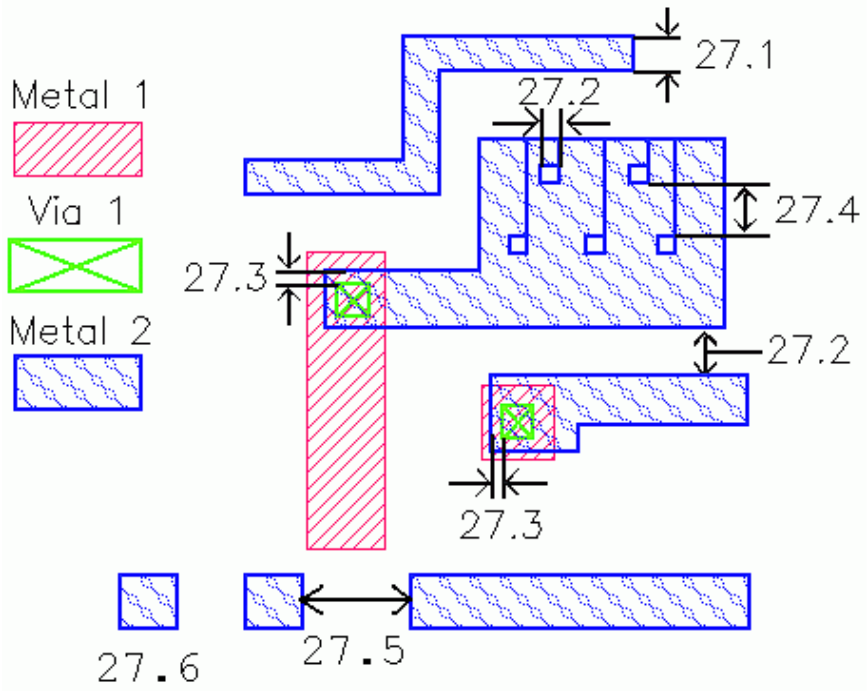
C035U (0.35 Micron) METAL 2 Layout Rules

Layer/level #27



Note 1: METAL2 (GDS layer 27) provides electrical connectivity to and from VIA1 and VIA2 layers.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
27.1	Minimum metal 2 width	0.60	µm	*	
27.2	Minimum metal 2 spacing	0.50	µm	*	
27.3	Minimum metal 2 enclosure of via 1	0.15	µm	*	
27.4	Maximum metal 2 width simultaneously in both directions	30.00	µm	*	If any dimension of METAL2 exceeds 30µm, sections of METAL2 can be cut to introduce holes such that 27.4 holds. The holes must obey all METAL2 design rules and should be staggered. The only exception to 27.4 is MIMC, MMCHB and MMCHP capacitors.
27.5	Minimum wide metal 2 spacing (metal 2 width > 10 um) to any metal 2	1.00	µm	*	
27.6	Minimum metal 2 area	0.49	µm²	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

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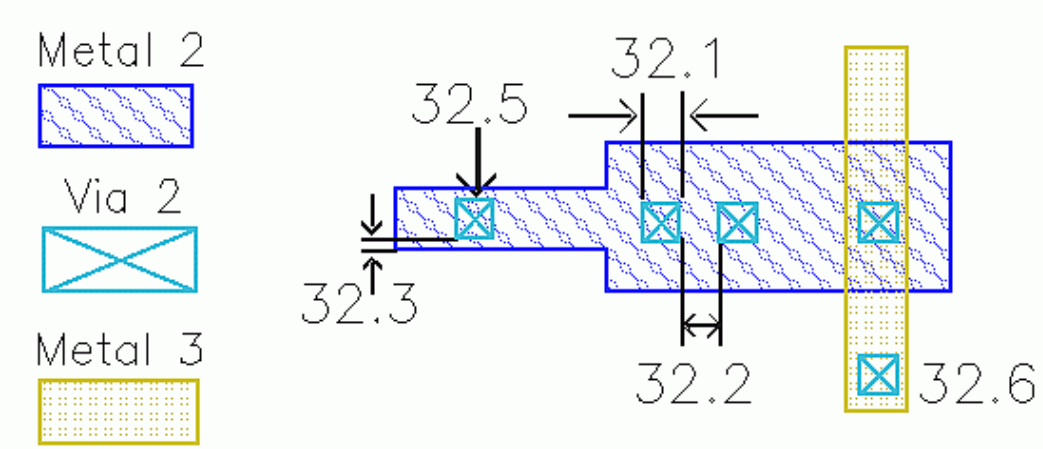
DES-0005 Rev: 11.0, 05-Oct-2010

C035U (0.35 Micron) VIA 2 Layout Rules

Layer/level #32



Note 1: VIA2 (GDS layer 32) provides electrical connectivity to and from METAL2, METAL3 and MIMC layers. VIA2 may be stacked over VIA1.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
32.1	Fixed via 2 dimensions (width = length)	0.40	µm	*	
32.2	Minimum via 2 spacing	0.50	µm	*	
32.3	Minimum metal 2 enclosure of via 2	0.15	µm	*	
32.5	All via 2 must have underlying metal 2			*	
32.6	All via 2 must be covered by metal 3			*	
32.7	Lonely via 2 needs redundancy, extra metal, or addition of dummy metal patterns			*	For lonely vias, please refer to LONELY VIA RULES section of this document

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

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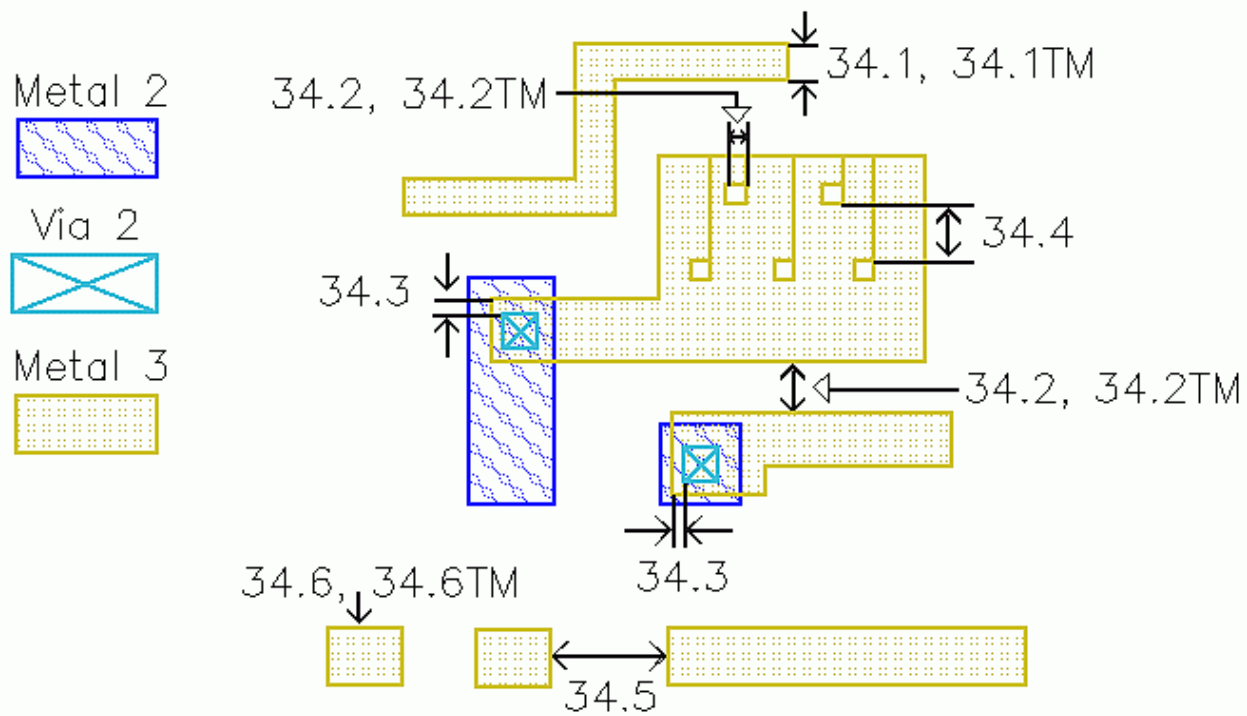
C035U (0.35 Micron) METAL 3 Layout Rules

Layer/level #34



Note 1: METAL3 (GDS layer 34) provides electrical connectivity to and from VIA2 and VIA3 layers. For a process with only three layers of metal, METAL3 acts as a termination of metal levels. There are two options for METAL3 layer in C035U family (please refer to manuals for individual technologies to determine if a particular option is offered):

TLM: Triple Layer Metal (TLM) process with thin top metal layer.
TLM-TM: Triple Layer Metal (TLM) process with Thick top Metal layer (TM).

Rules appended with TM after rule name are checked only if TM process option is selected in the design kit for a given metal level.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
34.1	Minimum metal 3 width	0.60	µm	*	
34.1TM	Minimum metal 3 width for TLM-TM process	0.70	µm	*	
34.2	Minimum metal 3 spacing	0.50	µm	*	
34.2TM	Minimum metal 3 spacing for TLM-TM process	0.70	µm	*	
34.3	Minimum metal 3 enclosure of via 2	0.15	µm	*	

34.4	Maximum metal 3 width simultaneously in both directions	30.00	µm	*	If any dimension of METAL3 exceeds 30µm, sections of METAL3 can be cut to introduce holes such that 34.4 holds. The holes must obey all METAL3 design rules and should be staggered. The only exception to 34.4 is MIMC, MMCHB and MMCHP capacitors.
34.5	Minimum wide metal 3 spacing (metal width > 10 um) to any metal 3	1.00	µm	*	
34.6	Minimum metal 3 area	0.49	µm²	*	
34.6TM	Minimum metal 3 area for TLM-TM process	0.64	µm²	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

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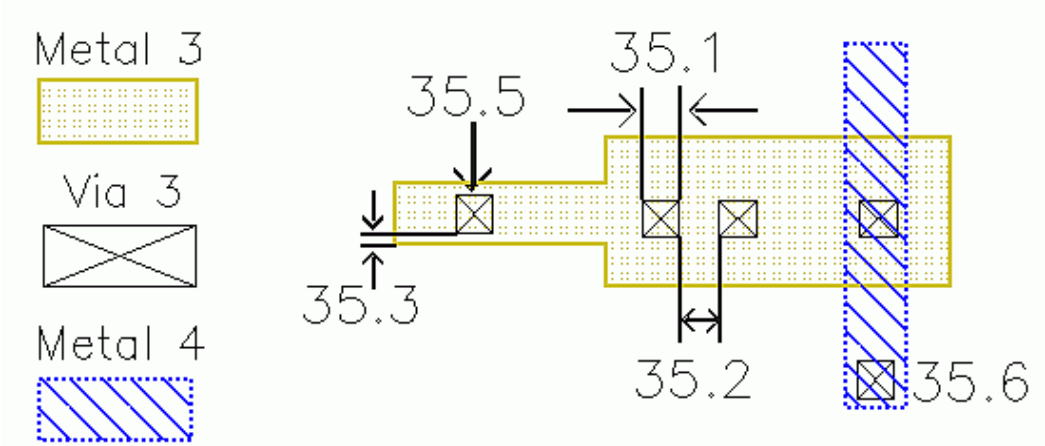
C035U (0.35 Micron) VIA 3 Layout Rules

Layer/level #35



Note 1: VIA3 (GDS layer 35) provides electrical connectivity to and from METAL3 and METAL4 layers. VIA3 may be stacked over VIA2.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
35.1	Fixed via 3 dimensions (width = length)	0.40	µm	*	
35.2	Minimum via 3 spacing	0.50	µm	*	
35.3	Minimum metal 3 enclosure of via 3	0.15	µm	*	
35.5	All via 3 must have underlying metal 3			*	
35.6	All via 3 must be covered by metal 4			*	
35.7	Lonely via 3 needs redundancy, extra metal, or addition of dummy metal patterns			*	For lonely vias, please refer to LONELY VIA RULES section of this document

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

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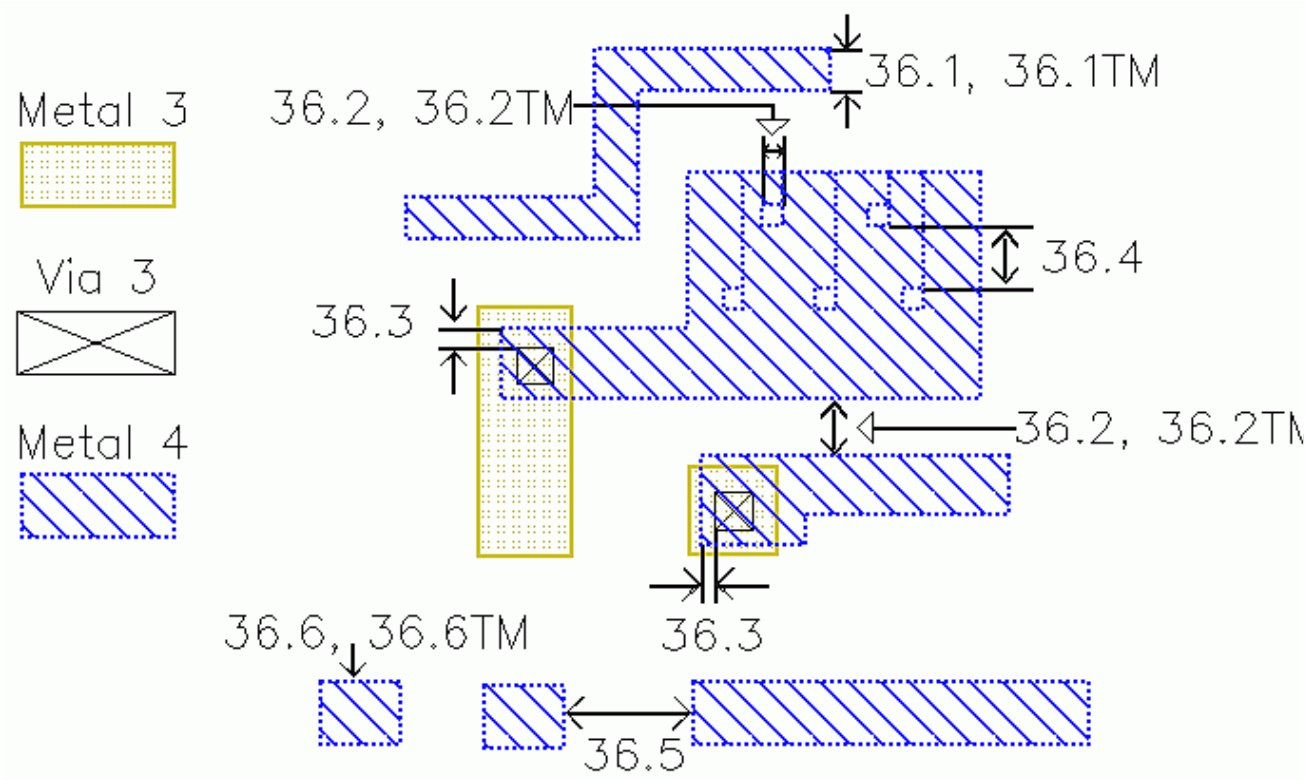
C035U (0.35 Micron) METAL 4 Layout Rules

Layer/level #36



Note 1: METAL4 (GDS layer 36) provides electrical connectivity to and from VIA3 and VIA4 layers. For a process with only four layers of metal, METAL4 acts as a termination of metal levels. There are two options for METAL4 layer in C035U family (please refer to manuals for individual technologies to determine if a particular option is offered):

QLM: Quadruple Layer Metal (QLM) process with thin top metal layer
QLM-TM: Quadruple Layer Metal (QLM) process with Thick top Metal layer (TM).

Rules appended with TM after rule name are checked only if TM process option is selected in the design kit for a given metal level.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
36.1	Minimum metal 4 width	0.60	µm	*	
36.1TM	Minimum metal 4 width for QLM-TM process	0.70	µm	*	
36.2	Minimum metal 4 spacing	0.50	µm	*	
36.2TM	Minimum metal 4 spacing for QLM-TM process	0.70	µm	*	

36.3	Minimum metal 4 enclosure of via 3	0.15	µm	*	
36.4	Maximum metal 4 width simultaneously in both directions	30.00	µm	*	If any dimension of METAL4 exceeds 30µm, sections of METAL4 can be cut to introduce holes such that 36.4 holds. The holes must obey all METAL4 design rules and should be staggered. The only exception to 36.4 is MMCHB and MMCHP capacitors.
36.5	Minimum wide metal 4 spacing (metal width > 10 um) to any metal 4	1.00	µm	*	
36.6	Minimum metal 4 area	0.49	µm²	*	
36.6TM	Minimum metal 4 area for QLM-TM process	0.64	µm²	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

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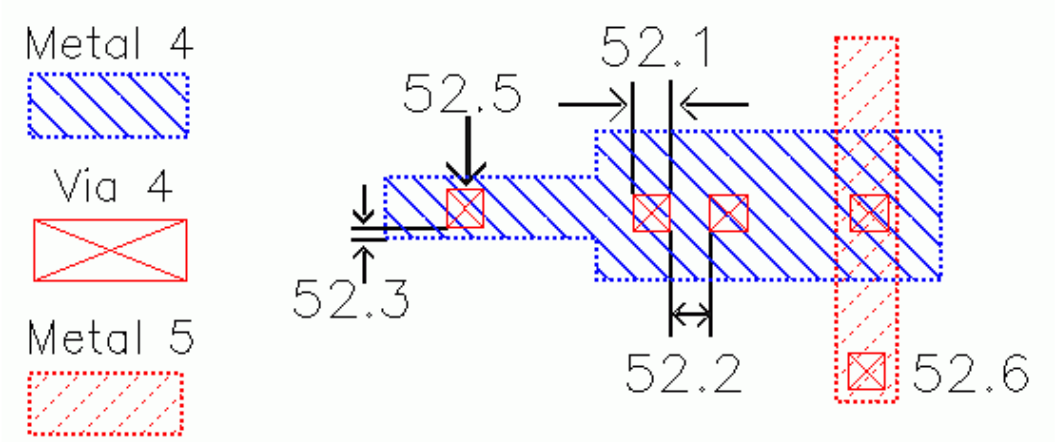
C035U (0.35 Micron) VIA 4 Layout Rules

Layer/level #52



Note 1: VIA4 (GDS layer 52) provides electrical connectivity to and from METAL4 and METAL5 layers. VIA4 may be stacked over VIA3.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
52.1	Fixed via 4 dimensions (width= length)	0.40	µm	*	
52.2	Minimum via 4 spacing	0.50	µm	*	
52.3	Minimum metal 4 enclosure of via 4	0.15	µm	*	
52.5	All via 4 must have underlying metal 4			*	
52.6	All via 4 must be covered by metal 5			*	
52.7	Lonely via 4 needs redundancy, extra metal, or addition of dummy metal patterns			*	For lonely vias, please refer to LONELY VIA RULES section of this document

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

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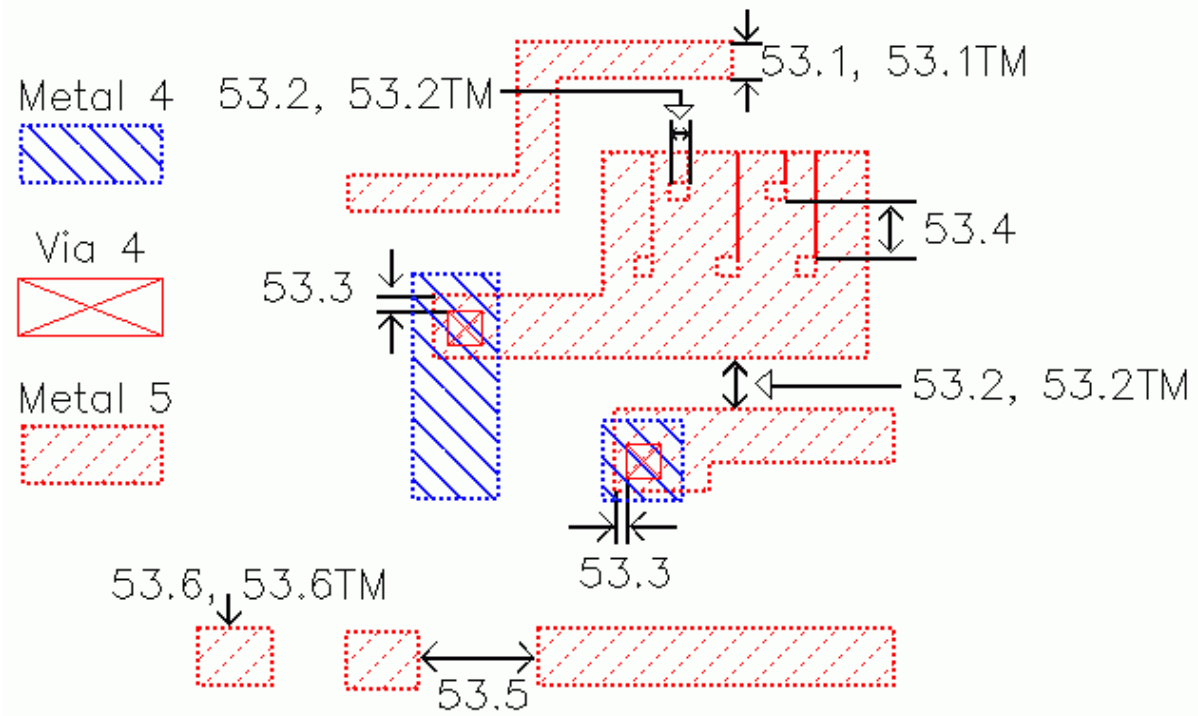
C035U (0.35 Micron) METAL 5 Layout Rules

Layer/level #53



Note 1: METAL5 (GDS layer 53) provides electrical connectivity to and from VIA4 layer. In C035U family, at the most 5 levels of metal are allowed. There are two options for METAL5 layer in C035U family (please refer to manuals for individual technologies to determine if a particular option is offered):

PLM: Pentuple Layer Metal (PLM) process with thin top metal layer.
PLM-TM: Pentuple Layer Metal (PLM) process with Thick top Metal layer (TM).

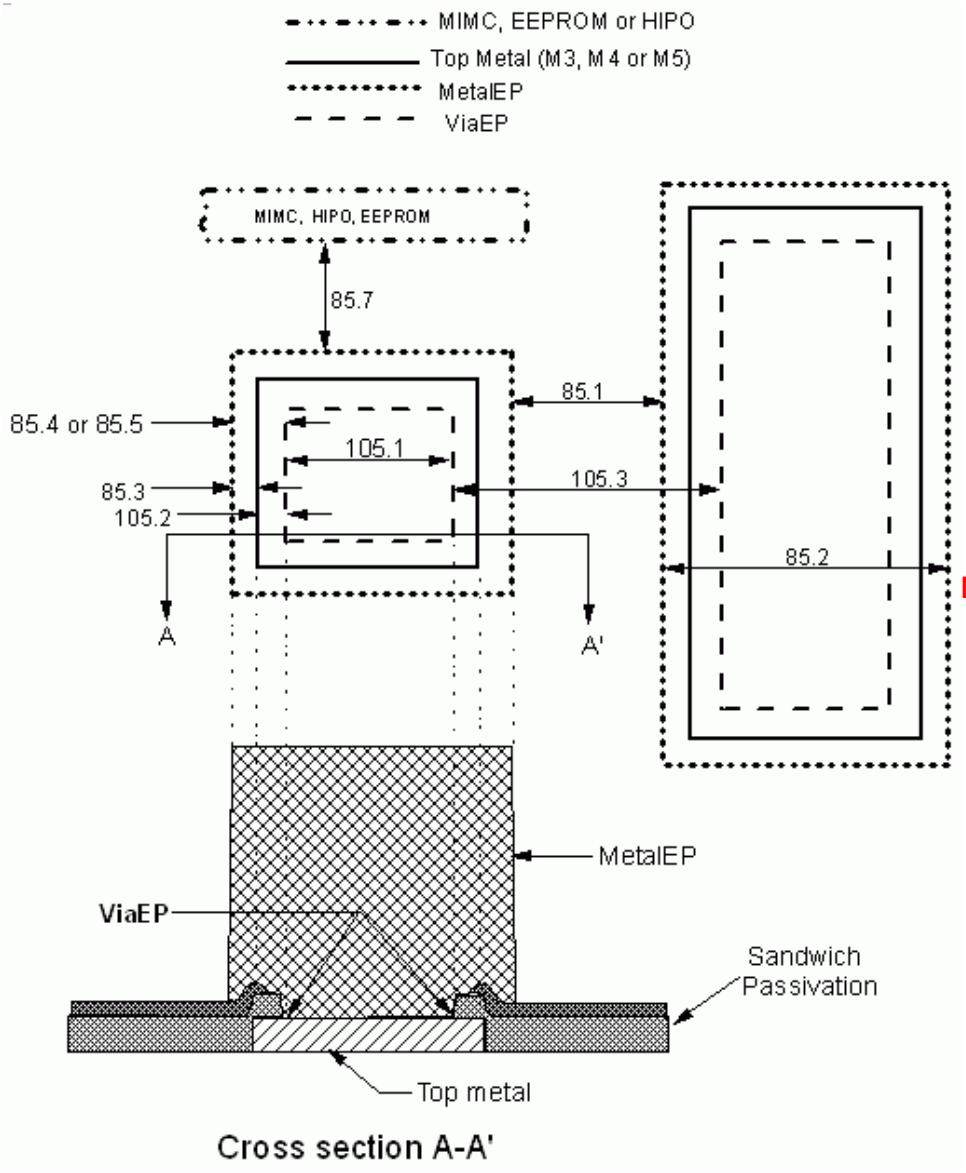
Rules appended with TM after rule name are checked only if TM process option is selected in the design kit for a given metal level.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
53.1	Minimum metal 5 width	0.60	µm	*	
53.1TM	Minimum metal 5 width for PLM-TM process	0.70	µm	*	
53.2	Minimum metal 5 spacing	0.50	µm	*	
53.2TM	Minimum metal 5 spacing for PLM-TM process	0.70	µm	*	
53.3	Minimum metal 5 enclosure of via 4	0.15	µm	*	

53.4	Maximum metal 5 width simultaneously in both directions	30.00	µm	*	If any dimension of METAL5 exceeds 30µm, sections of METAL5 can be cut to introduce holes such that 53.4 holds. The holes must obey all METAL5 design rules and should be staggered. The only exception to 53.4 is MMCHB and MMCHP capacitors.
53.5	Minimum wide metal 5 spacing (metal width > 10 um) to any metal 5	1.00	µm	*	
53.6	Minimum metal5 area	0.49	µm²	*	
53.6TM	Minimum metal5 area for PLM-TM process	0.64	µm²	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

C035U (0.35 Micron) POWER METAL Layout Rules



**NOTE --->
More graphics to view!
See following page
for graphic # 2**

Note 1: (Layers #105 and #85)

Power Metal is offered as an optional process where required for its associated advantages in Smart Power products. These rules are used only if power metal option is used.

Note 2: Power Metal Layers:

- ViaEP layer (GDS#105)
  - To open passivation over bond pads (GDS layer#31) and, over final metal traces (GDS layer #105) where required.
    At mask prep, the ViaEP layer (GDS layer #105) is merged into pad level Nitride layer (GDS layer#31); the resulting dataset is used to make PASSIVATION mask (Nitride), which is used for passivation etch.

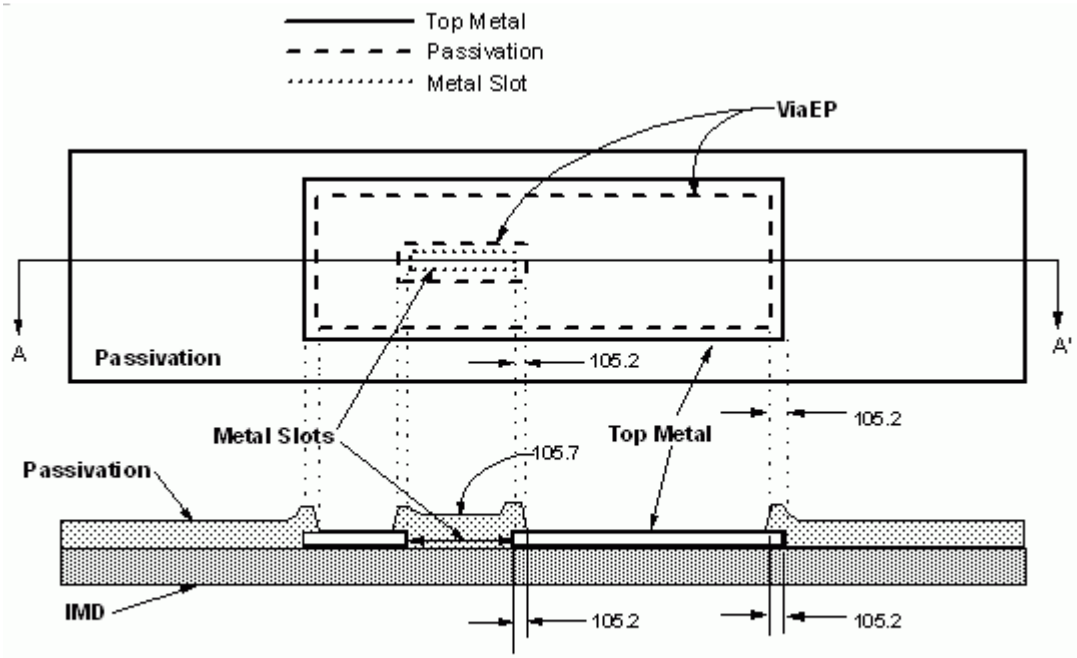
- MetalEP layer (GDS#85)
  - Designed by us (GDS Layer# 85) as a guideline for Subcon
  - Final mask design and mask build by Subcon
  - Defines Power Metal over bond pads and over final (top) metal traces where required.

Note 3: Power Metal Rules:

Rules 105.x and 85.x are only to be applied if MetalEP and ViaEP are present on the chip. No extra rule is to be applied if these layers are not present.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
105.1	Minimum ViaEP opening	5.00	µm	*	ViaEP rules
105.2	Minimum top metal enclosure of ViaEP	3.00	µm	*	ViaEP rules
105.3	Minimum ViaEP spacing	9.00	µm	*	ViaEP rules Top metal can be metal 3, 4, or 5
105.4	ViaEP without underlying top metal is not allowed			*	ViaEP rules No MetalEP in direct contact to IMD oxide.
105.5	ViaEP not covered by MetalEP is not allowed			*	ViaEP rules No Aluminum without SiN passivation
85.1	Minimum MetalEP spacing.	20.00	µm	*	MetalEP rules
85.2	Minimum MetalEP width	20.00	µm	*	MetalEP rules
85.3	Minimum MetalEP enclosure of top metal.	3.00	µm	*	MetalEP rules Top metal can be metal 3, 4, or 5
85.4	Minimum MetalEP enclosure of ViaEP	6.00	µm	*	MetalEP rules
85.5	Minimum MetalEP enclosure of nitride.	6.00	µm	*	MetalEP rules
85.6	Nitride not covered by MetalEP is not allowed			*	MetalEP rules
85.7a	Minimum spacing between MetalEP and matched unsalicided hipo and poly resistors.	50.00	µm	*	MetalEP rules
85.7b	Minimum spacing between MetalEP and MIMC	50.00	µm	*	MetalEP rules
85.7c	Minimum spacing between MetalEP and FREEPROM	50.00	µm	***	MetalEP rules
85.7d	Minimum spacing between MetalEP and matched transistors	50.00	µm	***	MetalEP rules
85.8	Maximum enclosure of MetalEP on ViaEP	50.00	µm	*	MetalEP rules
85.9	Any gate or poly plate connected to a net that is also connected to power metal should have a connection to active.			*	MetalEP rules Resistors and polydiodes are seen as shorts for this rule.

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)



Cross section A-A'

C035U (0.35 Micron) CORRECT USE OF TOP METAL Layout Rules

Note 1: C035U based technologies allows use of either a thick or thin top metal. This leads to different layout rules (for instance compare rule 34.2 with 34.2TM). To warn a user that metal routing exists above top metal for design, warnings are issued.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
wtopmetal3	WARNING: metal layers above top level metal detected. (flags when metal4 or metal5 are present when metal3 is the top metal layer)			*	exception for bondpads and probepads (including minimal enclosure of nitride by metal4 or metal5 as defined by bondpad & probepad rules)
wtopmetal4	WARNING: metal layers above top level metal detected. (flags metal5 is present when metal4 is top metal)			*	exception for bondpads and probepads (including minimal enclosure of nitride by metal5 as defined by bondpad & probepad rules)

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

C035U (0.35 Micron) NOGEN Layout Rules

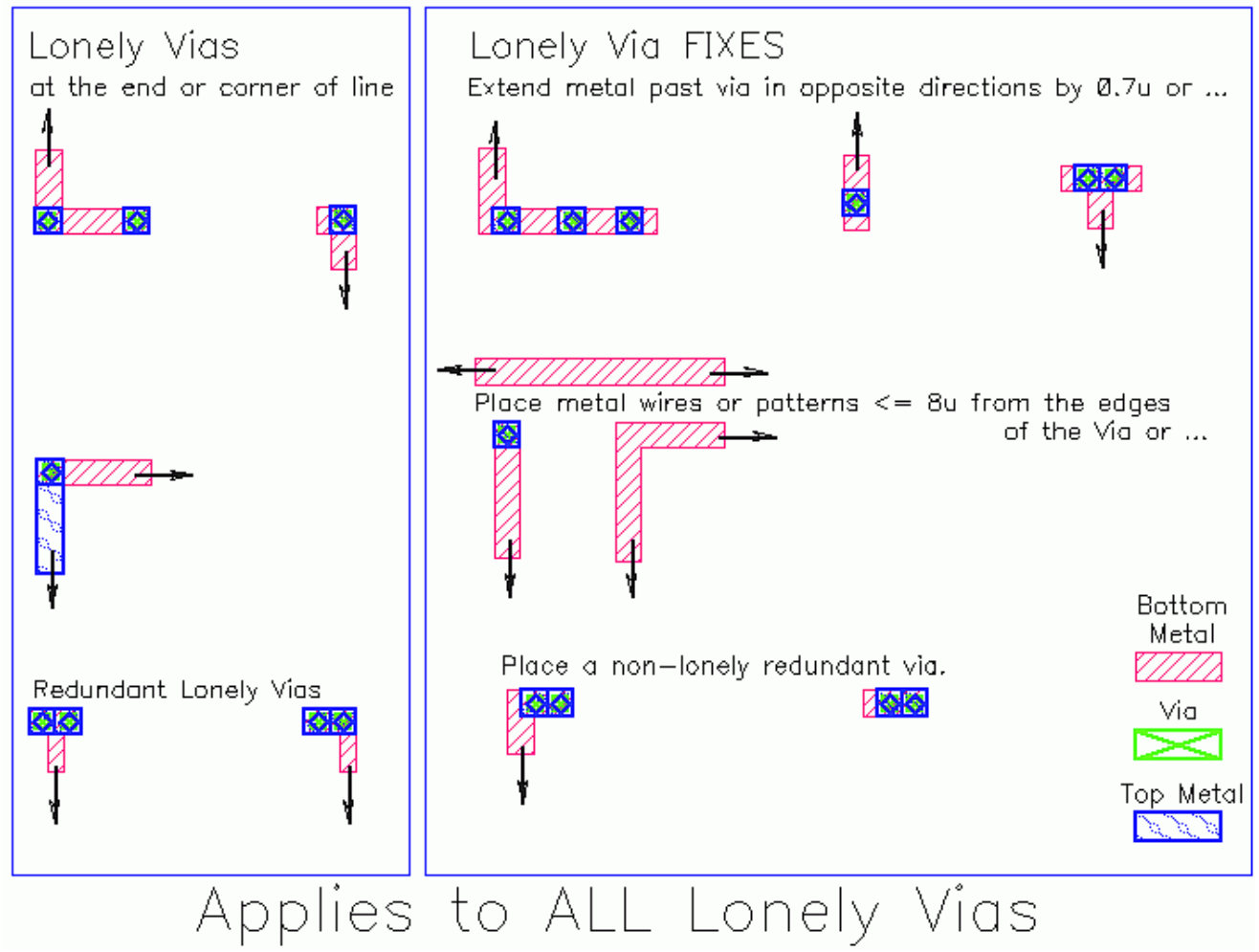
Layer/level #61

Note 1: NOGEN (GDS layer 61) is a technology debug layer. It prevents automatic generation at mask preparation and hence all automatically generated layers must be explicitly drawn if NOGEN is present. Use of this layer outside of its scope can have dire consequences.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
61.1	NOGEN may not be drawn			*	Exception for zener zap diode (ZZD)

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

C035U (0.35 Micron) LONELY VIAS Layout Rules



Note 1: The rules given in this section apply to all via levels and the underlying metal connect layer.

Note 2: Definition

A lonely via is defined as a via
- in a corner or at the end of a metal wire ,
- with minimum underlying metal enclosure,
- without redundancy,
- and without surrounding metal patterns within a distance of 8 um.

Note 3: Lonely via fixes

The following techniques can be used to fix lonely via cases

- Extend the underlying metal connect layer past the via by 0.7 um
- Add dummy metal wires or patterns within a distance of 8 um from the edges of the via
- Add non-lonely redundant vias

Note 4: The examples given in this section have been copied from AMIS doc. 4500104 Rev. P, ami350, 0.35 micron Design Rules.

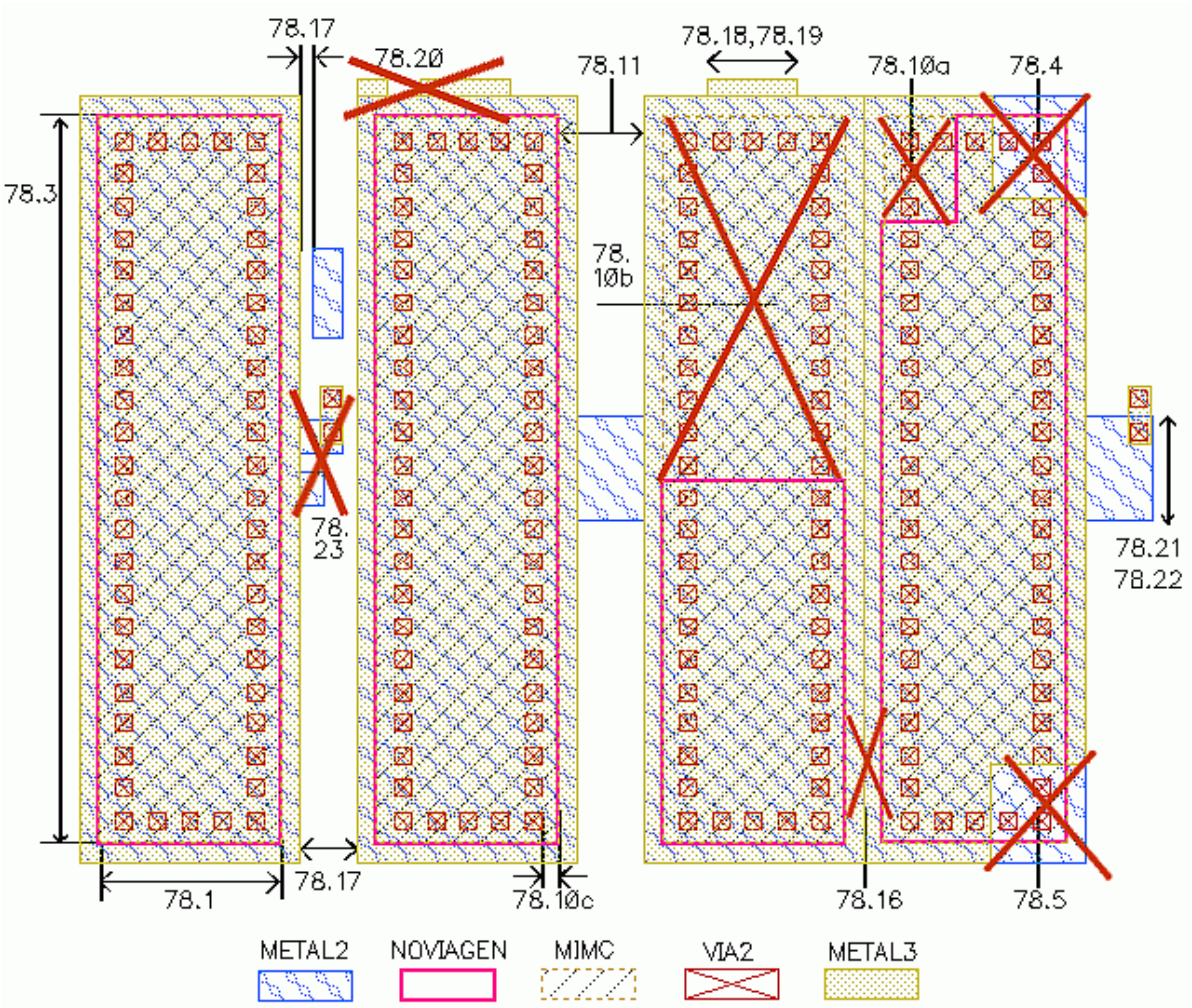
Note 5: Metal patterning is applied where there is none of the following layers:

- Metdis
- Mexclude
- Nitride
- Hipo
- Nogen
- Poly2

If the layers Metdis and Mexclude are absent from a layout the lonely via rules are applied to the whole layout.

C035U (0.35 Micron) MIMC Layout Rules

Layer/level #78



Note 1: MIMC (GDS layer 78) defines the top plate of Metal Insulator Metal (MIM) Capacitors. MIMC is also referred to as METAL2.5 because it is sandwiched between METAL2 and METAL3. Bottom plate of MIM Capacitors is defined by METAL2, and capacitor area is defined by the logical (MIMC AND METAL2). VIA2 is used to contact both top and bottom plates of the MIM Capacitor. METAL3 is needed to contact top plate of a MIM Capacitor. VIA2 on the top plate is generated during mask making unless either NOVIAGEN (GDS layer 106) or NOGEN (GDS layer 61) is used, in which case VIA2 must be explicitly drawn.

To achieve higher density a MIM Capacitor may be placed over active and/or passive circuit elements. For precision analog and RF applications, it is highly recommended not to place any active and/or passive circuit elements underneath the MIM Capacitor. For these applications, it is also highly recommended to block automatic metal fill generation by placing METDIS (GDS layer 63) over the MIM Capacitor and by not routing any metal over the MIM Capacitor.

Note 2: The rules that reference this note are located in the antenna rule checks and are not checked by the general DRC checks. These rules use connections via interconnect (POLY, CONTACT, VIAs, and all METAL levels)

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
78.1	Minimum MIMC width	2.00	µm	*	
78.3	Maximum MIMC area	2025.00	µm²	*	
78.4	Minimum MIMC enclosure by METAL2	1.50	µm	*	MIMC must be enclosed by METAL2.
78.5	Minimum MIMC enclosure by METAL3	1.50	µm	*	MIMC must be enclosed by METAL3.
78.7	For both plates, connection to ACTIVE must be made at the same metal level for metal 2 and higher			*	To avoid plasma charging damage. See Note 2.
78.8a	For a MIM Capacitor not connected to ACTIVE, the area of each metal level (METAL3 and above) connected to one plate must not differ from the area connected to the other plate by more than this ratio	0.10		*	To avoid plasma charging damage. See Note 2. For example, the ratio of METAL3 area between the top and bottom plate, and similar for higher metal layers.
78.8b	78.8a will not apply to the given metal layer if the area of a metal layer connected to a MIM Capacitor plate is less than this value.	2.00	µm²	*	Example: Area of METALx connected to top plate = 200µm², area of METALx connected to bottom plate = 2µm² (for all x>2). See Note 2.
78.9	For a MIM Capacitor not connected to ACTIVE, the number of VIAx (x>1) connected to each plate must either be identical or not greater than this value	2		*	To avoid plasma charging damage. See Note 2. This rule has been verified for up to 300 VIAx (x>1) in silicon processing. The maximum case tested had 2 VIAx on one plate and 300 VIAx on the other plate. The “identical number” method is preferred.
78.10a	If NOVIAGEN is not drawn on MIMC, VIA2 must not be drawn			*	In the absence of NOVIAGEN, VIA2 will be generated at mask preparation. Drawn VIA2 is the preferred method of MIM Capacitor layout.
78.10c	If either NOVIAGEN or NOGEN is drawn on MIMC, VIA2 must be drawn with minimum MIMC enclosure no less than this value	0.75	µm	*	Automatic VIA2 generation at mask preparation is suspended if NOVIAGEN or NOGEN is drawn. Drawn VIA2 is the preferred method of MIM Capacitor layout.

78.11	Minimum MIMC spacing to METAL3	2.50	µm	*	
78.16	Neighboring MIM Capacitors that are connected with METAL2 must use METAL2 leadaways			*	
78.17	All metal or poly connected to each floating MIM Capacitor requires this spacing to other common layer metal or poly that is connected to ACTIVE or gate at the same processing step as the MIM Capacitor plates	2.20	µm	*	
78.18	Maximum width of a METAL3 leadaway from a MIM Capacitor	5.00	µm	*	This width is checked perpendicular to the leading away METAL3.
78.19	Minimum width of a METAL3 leadaway from a MIM Capacitor	2.00	µm	*	This width is checked perpendicular to the leading away METAL3.
78.20	Only one METAL3 leadaway is allowed on each side of a MIM Capacitor			*	
78.21	Maximum width of a METAL2 leadaway from a MIM Capacitor	5.00	µm	*	This width is checked perpendicular to the leading away METAL2.
78.22	Minimum width of a METAL2 leadaway from a MIM Capacitor	2.00	µm	*	This width is checked perpendicular to the leading away METAL2.
78.23	Only one METAL2 leadaway is allowed on each side of a MIM Capacitor			*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

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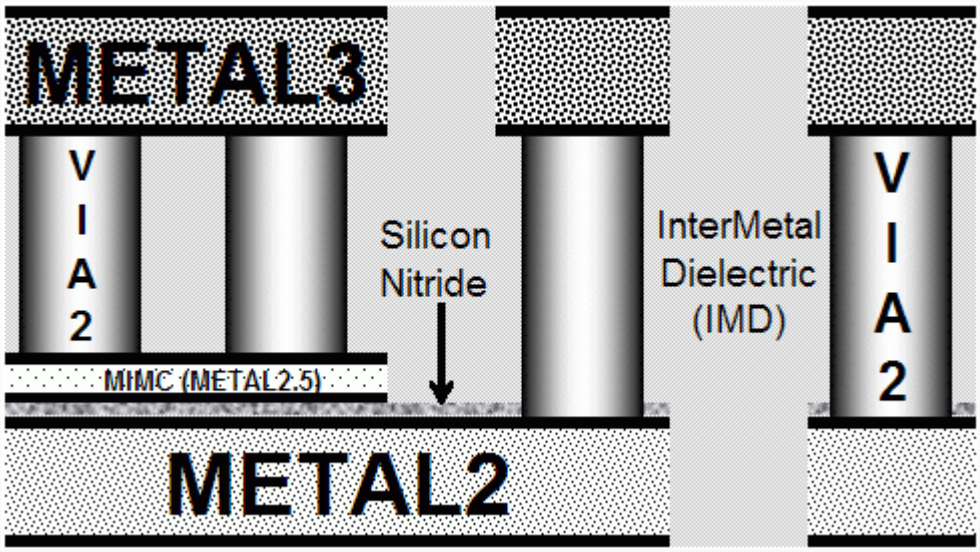
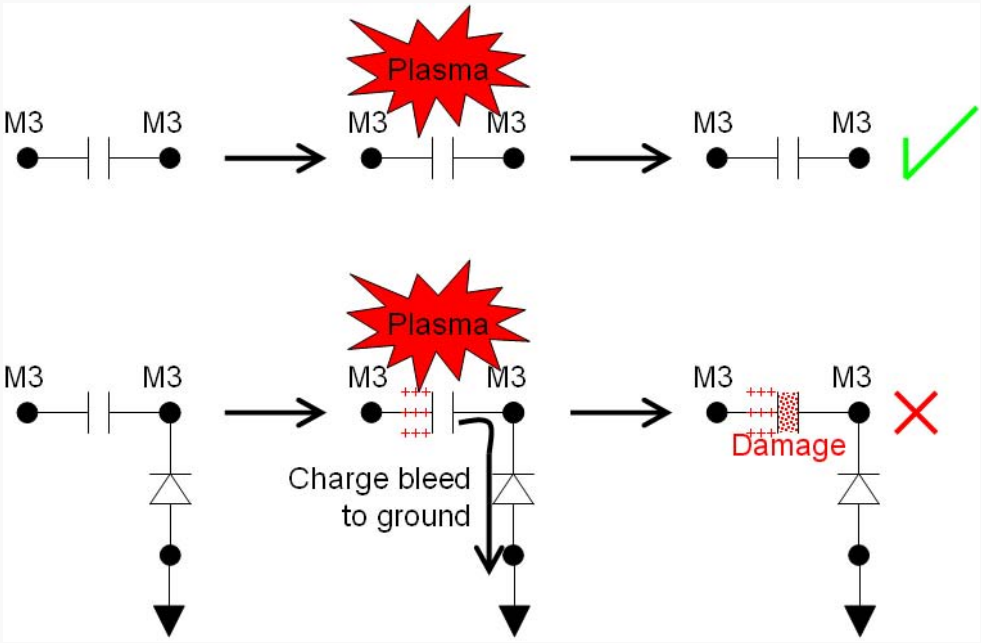
- **See below for information on cross sections of a MIM Capacitor and information regarding rules 78.7, 78.8a, 78.8b, 78.9, and 78.16 (or select here to view):**

C035U, 0.35 Micron MIMC Layout Rules *continued*

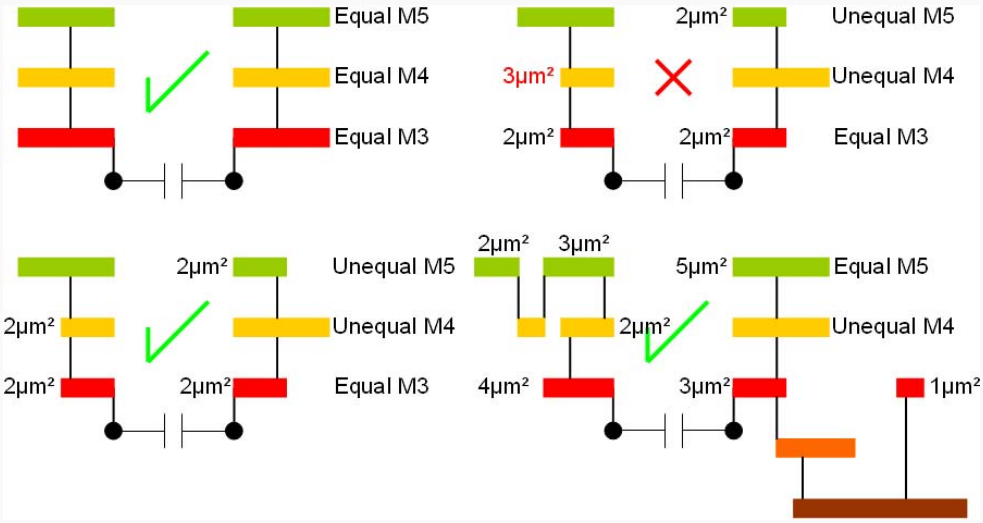
Cross Section of a MIM Capacitor:



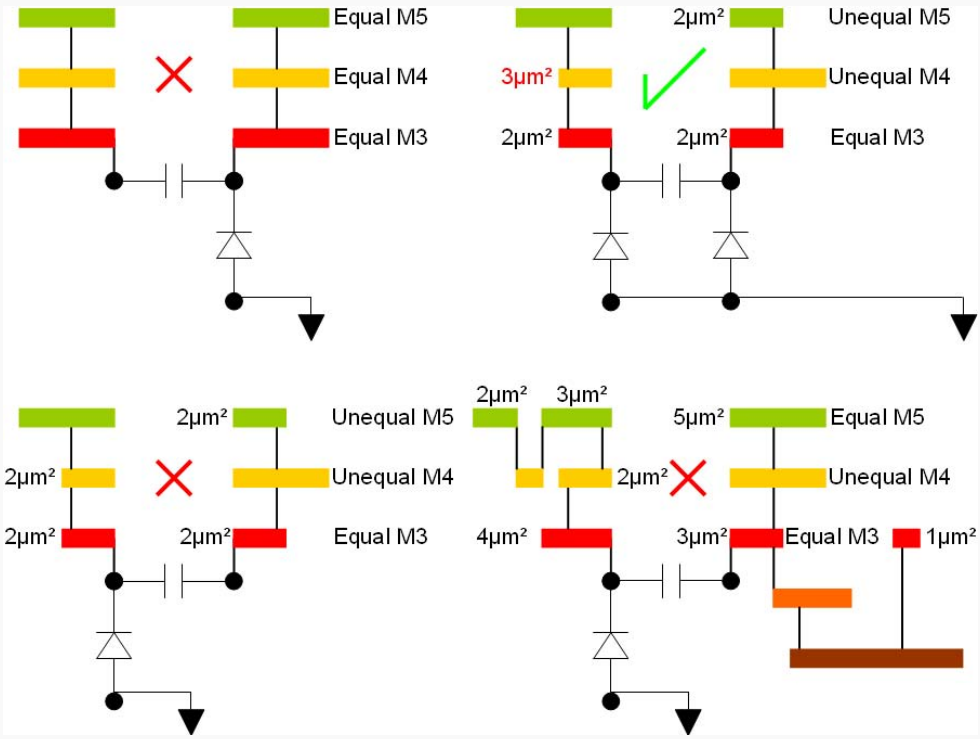
Schematic representations of 78.7 to avoid plasma charging damage:



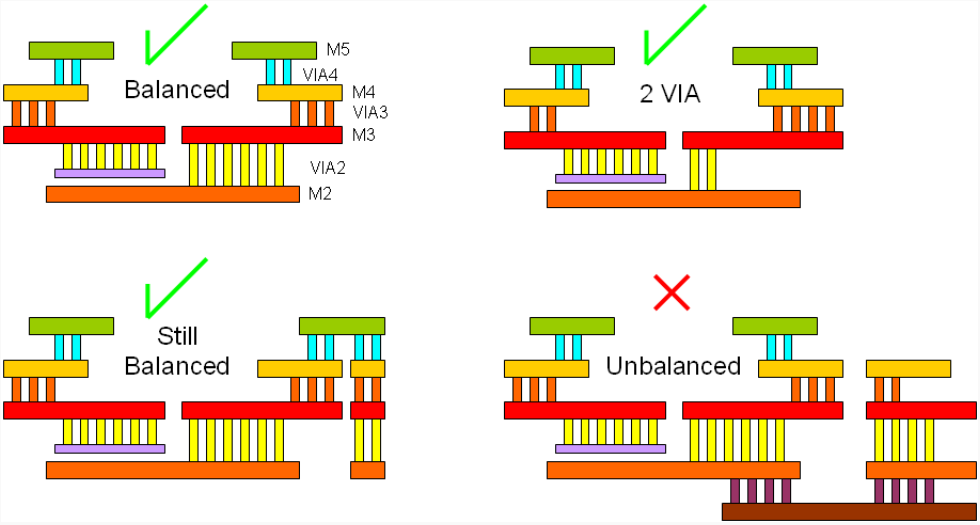
Schematic representation of 78.8a/78.8b to avoid plasma charging damage:



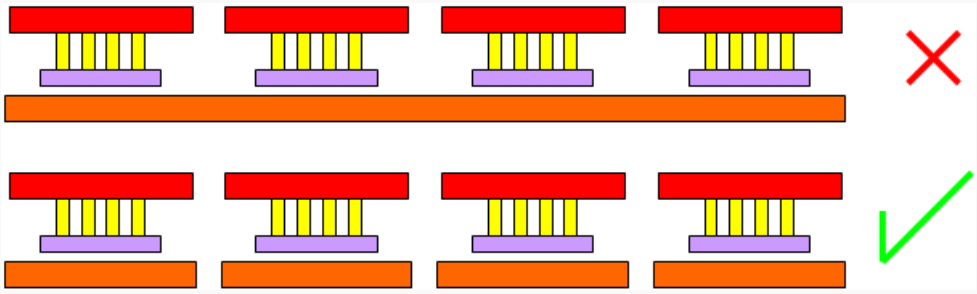
Schematic representation of 78.8a/78.8b to avoid plasma damage:



Cross section representation of 78.9 to avoid plasma damage:



Cross section representation of 78.16:



C035U (0.35 Micron) PATTERN DENSITY/ DUMMY METAL Layout Rules

Note 1: At mask preparation for C035U based technologies; dummy metal is generated on all metal levels to ensure manufacturability.

In areas of a layout where components sensitive to stress and capacitive coupling (through unrelated metal) exist, it may be desirable to block the generation of dummy metal. The presence of METDIS (GDS layer 63) blocks generation of dummy metal. METDIS must be drawn at layout stage and hence it is a responsibility of the design team.

Use of METDIS should be limited. It is possible to generate reticles without any dummy metal for design prototypes. In such a case a request must be made to mask preparation group prior to reticle generation.

DRC for this check is performed on 1mm by 1mm areas, overlapping 0.5mm.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
POLYA.min	Minimum polysilicon density, dummy poly to be added if density lower than specified	.05		*	
POLYA.max	Maximum polysilicon density	.40		*	
MTL1A.min	Minimum metal 1 density after dummy metal generation	.20		*	
MTL1A.max	Maximum metal 1 density after dummy metal generation	.60		*	
MTL2A.min	Minimum metal 2 density after dummy metal generation	.20		*	
MTL2A.max	Maximum metal 2 density after dummy metal generation	.60		*	
MTL3A.min	Minimum metal 3 density after dummy metal generation	.20		*	
MTL3A.max	Maximum metal 3 density after dummy metal generation	.60		*	
MTL4A.min	Minimum metal 4 density after dummy metal generation	.20		*	rule should not be checked if top metal is metal3
MTL4A.max	Maximum metal 4 density after dummy metal generation	.60		*	rule should not be checked if top metal is metal3
MTL5A.min	Minimum metal 5 density after dummy metal generation	.20		*	rule should not be checked if top metal is metal3 or metal4
MTL5A.max	Maximum metal 5 density after dummy metal generation	.60		*	rule should not be checked if top metal is metal3 or metal4

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

(Confidential)
DES-0005 Rev: 11.0, 05-Oct-2010

C035U (0.35 Micron) METDIS Layout Rules

Note 1: METDIS (GDS layer 63) is used to block generation of dummy metal at mask preparation. The primary use of this layer is to block generation of dummy metal on matched or sensitive components. The components may be sensitive to (including but not limited to) metal stress, capacitive coupling etc.

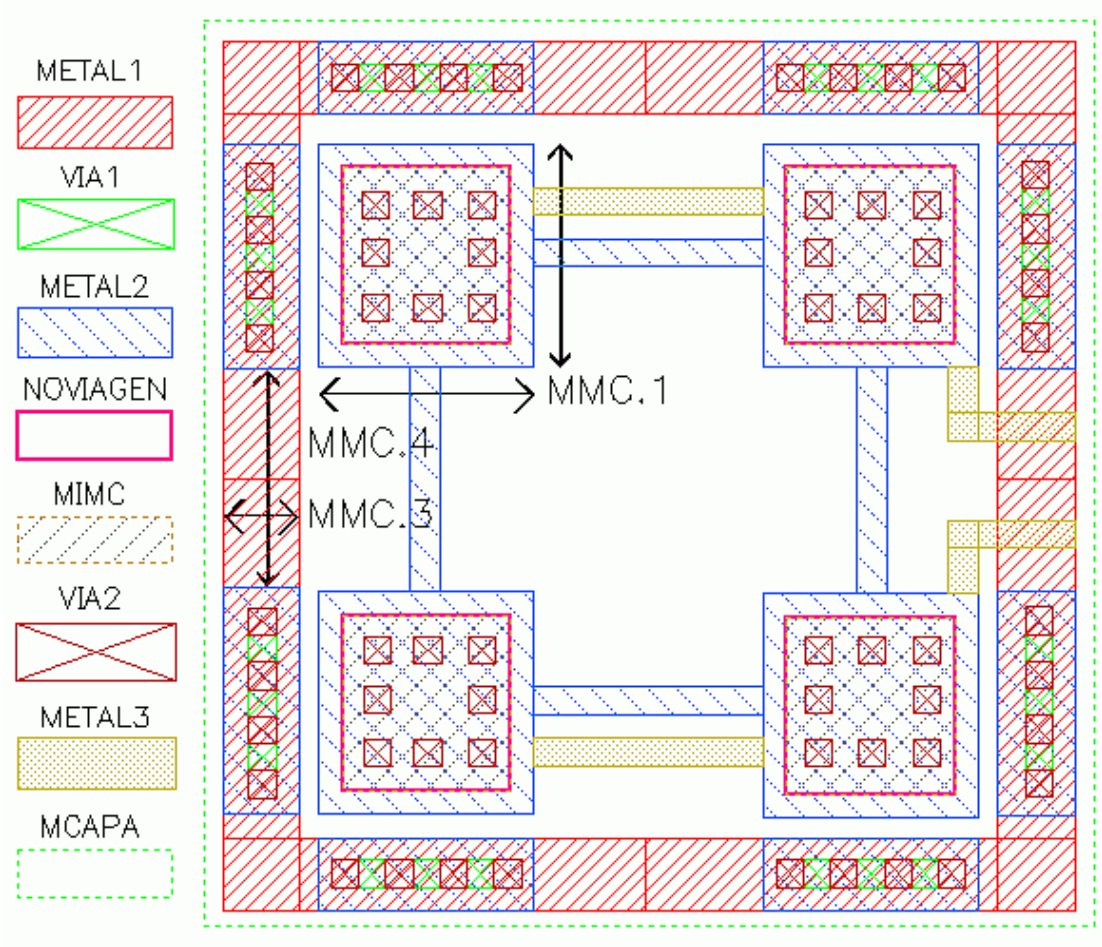
For resistors and capacitors, LOWACC (GDS layer 108) is used to determine if the component is considered a LOW ACCuracy (LOWACC) device. The absence of LOWACC is used to determine if a warning should be issued. Transistors include both CMOS and BIPolar devices.

Matched components are expected to have at least one terminal in common.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
63.1	WARNING: minimum metdis (or mexclude) enclosure of matched resistor pair	5.0	µm	*	
63.2	WARNING: minimum metdis (or mexclude) enclosure of matched capacitors	5.0	µm	*	
63.3	WARNING: minimum metdis (or mexclude) enclosure of matched transistors	5.0	µm	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

C035U (0.35 Micron) MATCHED MIM CAPACITORS Layout Rules



Note 1: Following is a list of good practices for pair of matched MIM Capacitors. Below the list is a set of rules that must be followed.

- Both capacitors in a matched pair should have identical properties and environment. Properties include width, length, number and spacing of elements in the bank. Environment includes (but is not limited to) proximity to unrelated metal, metal fill blocking using METDIS (GDS layer 63), etc.
- Dummy metal capacitors should be placed around the periphery of the banks to provide identical environment. Whenever possible, use identical layout. At the very least METAL2 and METAL3 strips shorted through VIA2 should be used to build dummy metal capacitors.
- A shield diffusion may be used to shield a bank of capacitors. Whenever possible, the shield should be connected to one terminal of each capacitor in the bank. The device is then modeled as a 3 terminal element.
- MCAPA (GDS layer 3) should enclose dummy capacitor elements. Similarly if shielded with a shield diffusion, MSHIELD (GDS layer 62 data type 49) should also enclose dummy capacitor elements.

To disable checking for linearity and/or matching enclose the bank by LOWACC (GDS layer 108).

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
MMC.1	Minimum width of MIMC in matched capacitors, in both directions	10.00	µm	*	78.1
MMC.3	Minimum width of dummy metal capacitor (for any used metals)	3.00	µm	***	
MMC.4	Maximum width of interruption in the dummy metal ring capacitor	3.00	µm	***	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

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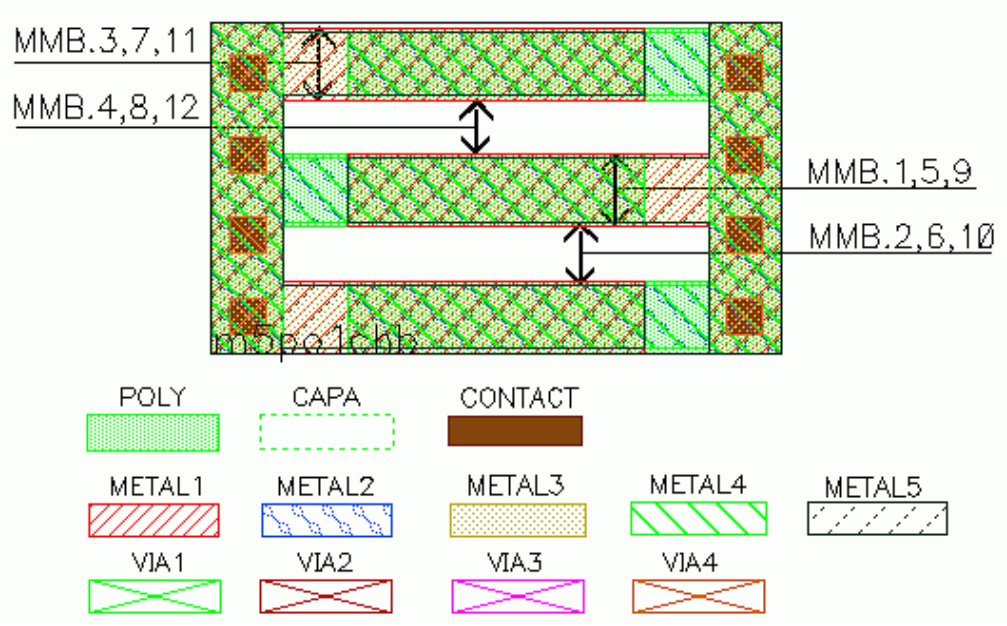
DES-0005 Rev: 11.0, 05-Oct-2010

C035U (0.35 Micron) INTERDIGITATED METAL CAPACITORS Layout Rules



Note 1: Interdigitated Metal Capacitors use standard metallization to form two flavors of capacitors; MMCHB and MMCHBNW, which differ in the presence of an N-WELL shield. Area of the capacitor is defined by the overlap of fingers. The capacitor must be marked by enclosure by MCAPA layer with model name. For example, a capacitor with POLY, METAL1, METAL2, METAL3 is marked with model name: m3po1chb.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
MMB.1	Fixed Poly width perpendicular to fingers in capacitor area (when poly)	0.80	µm	*	
MMB.2	Fixed Poly spacing perpendicular to fingers in capacitor area. (when poly)	0.60	µm	*	
MMB.3	Fixed Metal1 width perpendicular to fingers in capacitor area.	0.80	µm	*	
MMB.4	Fixed Metal1 spacing perpendicular to fingers in capacitor area.	0.60	µm	*	
MMB.5	Fixed Metal2 width perpendicular to fingers in capacitor area.	0.70	µm	*	
MMB.6	Fixed Metal2 spacing perpendicular to fingers in capacitor area.	0.70	µm	*	
MMB.7	Fixed Metal3 width perpendicular to fingers in capacitor area.	0.70	µm	*	
MMB.8	Fixed Metal3 spacing perpendicular to fingers in capacitor area.	0.70	µm	*	

MMB.9	Fixed Metal4 width perpendicular to fingers in capacitor area. (when metal 4)	0.70	µm	*	
MMB.10	Fixed Metal4 spacing perpendicular to fingers in capacitor area when metal 4)	0.70	µm	*	
MMB.11	Fixed metal 5 width perpendicular to fingers in capacitor area (when metal 5)	0.70	µm	*	
MMB.12	Fixed metal 5 spacing perpendicular to fingers in capacitor area (when metal 5)	0.70	µm	*	
MMB.13	A capacitor that goes up to metal 3 should not be routed with metal 4 or 5 on top			*	
MMB.14	A capacitor that goes up to metal 4 should not be routed with metal 5 on top			*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

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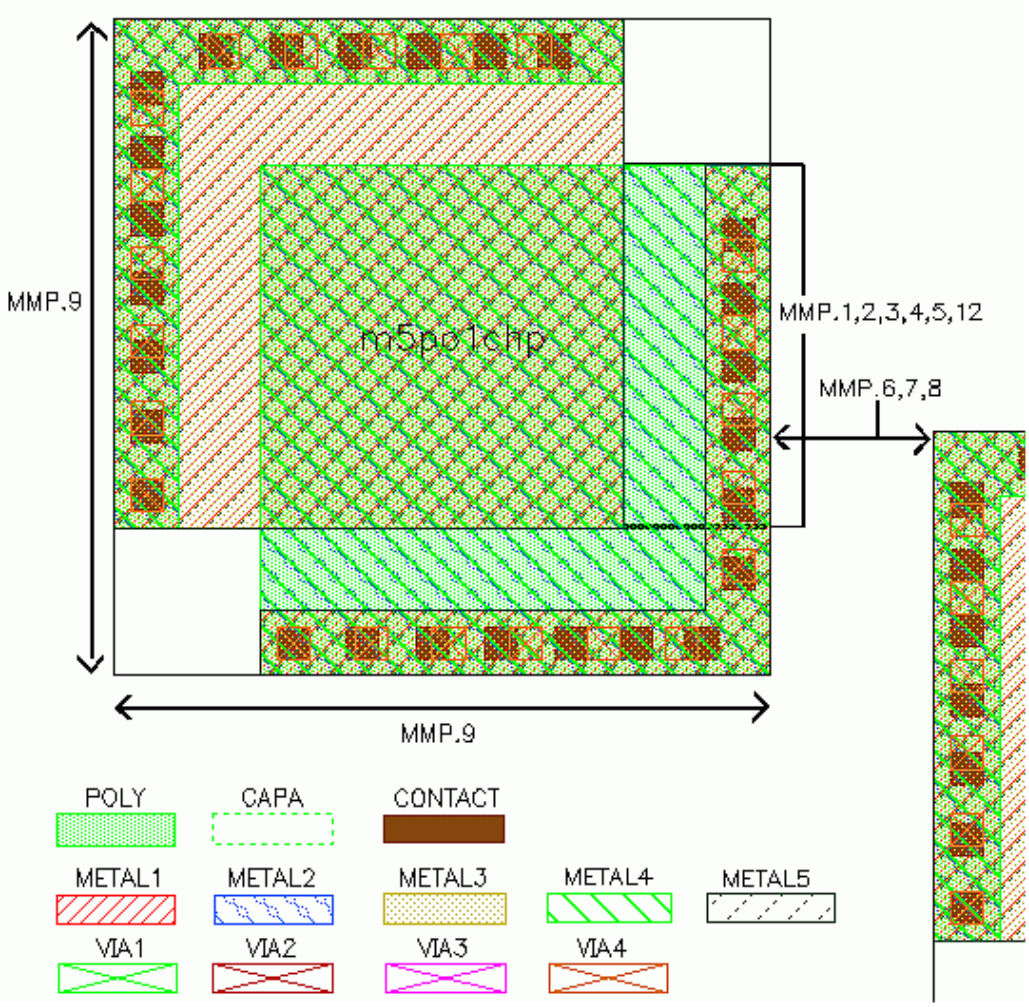
DES-0005 Rev: 11.0, 05-Oct-2010

C035U (0.35 Micron) METAL PLATE CAPACITORS Layout Rules



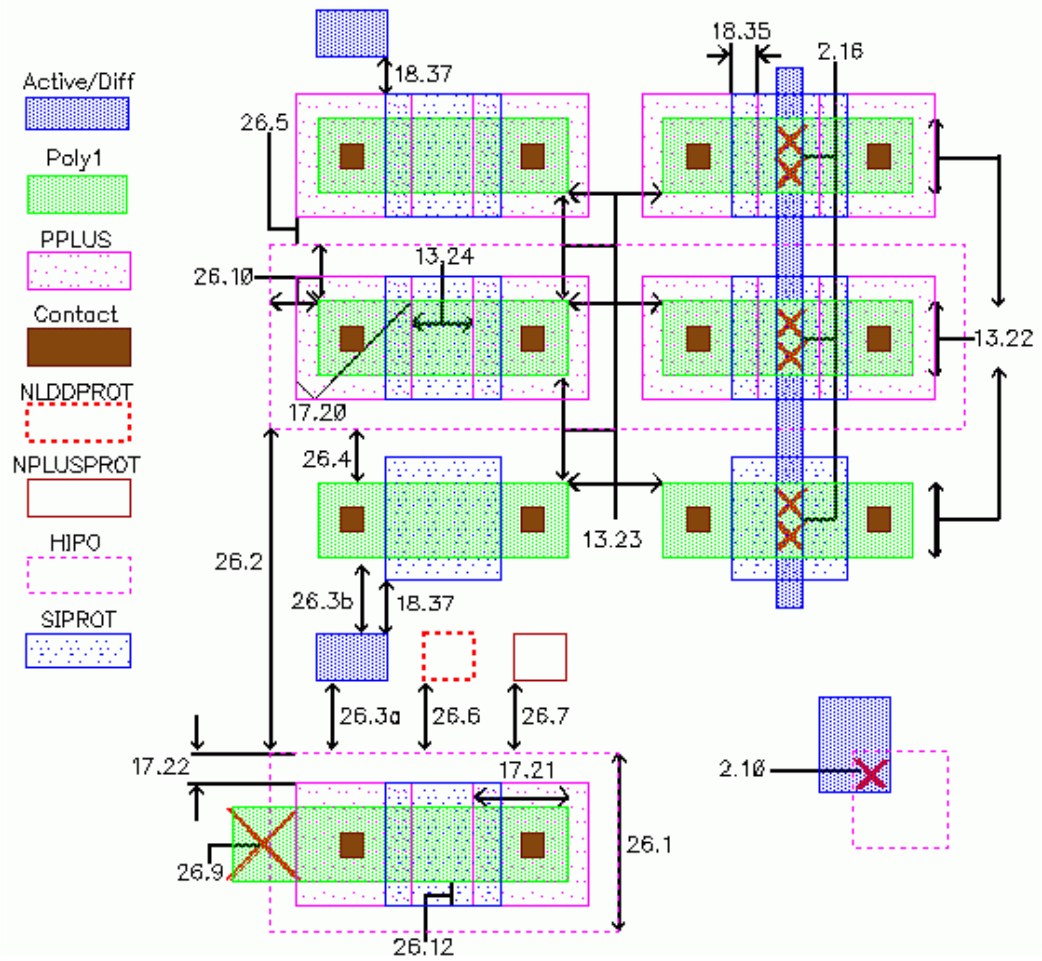
Note 1: Metal Plate Capacitors use standard metallization to form two flavors of capacitors; MMCHP and MMCHPNW, which differ in the presence of an N-WELL shield. Area of the capacitor is defined by the overlap of metal plates. The capacitor must be marked by enclosure by MCAPA layer with model name. For example, a capacitor with POLY, METAL1, METAL2, METAL3 is marked with model name: m3po1chp.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
MMP.1	Poly should cover the capacitor area fully (when poly)			*	
MMP.2	Metal1 should cover the capacitor area fully			*	
MMP.3	Metal2 should cover the capacitor area fully			*	

MMP.4	Metal3 should cover the capacitor area fully			*	
MMP.5	Metal4 should cover the capacitor area fully (when Metal 4)			*	
MMP.6	Minimum MMP spacing to other MMP if width or length > 100	25.00	µm	*	
MMP.7	Minimum MMP spacing to other MMP if width or length > 200	50.00	µm	*	
MMP.8	Minimum MMP spacing to other MMP if width or length > 450	100.00	µm	*	
MMP.9	Maximum size of width if the length of the MMP is above 200 (and maximum size of length if the width is above 200)	500.00	µm	*	
MMP.10	A capacitor that goes up to metal 3 should not be routed with metal 4 or 5 on top			*	
MMP.11	A capacitor that goes up to metal 4 should not be routed with metal 5 on top			*	
MMP.12	Metal5 should cover the capacitor area fully (when Metal 5)			*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

C035U (0.35 Micron) HIPO RESISTOR Layout Rules



Note 1: HIPO (GDS layer 26) is used to define a p-type non-silicided polysilicon resistor. The resistor has a typical Rsh of 1K Ohms/Sq. The ends of the resistor are highly doped to provided ohmic electrical contact to the body of the resistor.
Drawn width of the HIPO resistor is defined by the width of polysilicon line. Drawn length of the resistor is defined by the spacing between the drawn PPLUS regions that form the highly doped ends.
When drawing a HIPO resistor, there is no need to explicitly draw NPLUSPROT and/or NLDDPROT. These are generated during mask fabrication process. A HIPO resistor drawn underneath a MIM Capacitor or without a shield is considered as low accuracy and hence should be marked with LOWACC layer.
HIPO enclosed in LOWACC is not checked for matching and/or linearity performance.

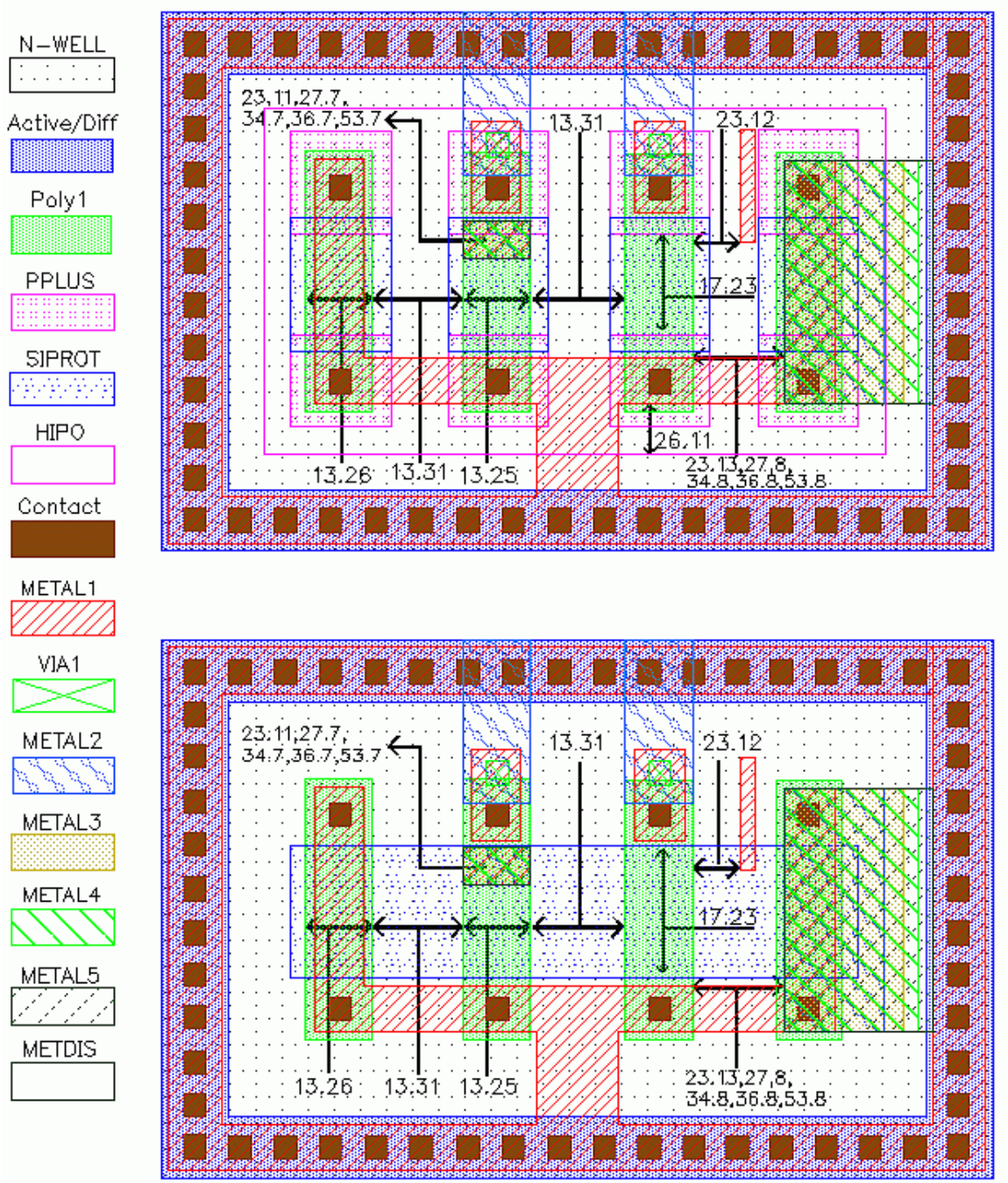
Additional rules apply for a bank of matched resistors. The user is referred to the section on Matched Resistors for additional information.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
2.10	The protection layer hipo of a HIPO resistor is not allowed on ACTIVE			*	ACTIVE AREA (GDS layer 2)
2.16	The body in POLY of hipo or unsalicided N+/P+ poly resistors is not allowed on ACTIVE.			*	ACTIVE AREA (GDS layer 2)

13.20	Hipo resistor, non-salicided n+ and p+ poly resistors must be shielded devices if used for matching/linearity applications: this rule is compulsory when the lowacc layer does not mark the resistor.			*	POLYSILICON (GDS layer 13)
13.22	Minimum width of POLY of hipo or unsalicided N+/P+ poly resistors	1.20	µm	*	POLYSILICON (GDS layer 13)
13.23	Minimum spacing between POLY of adjacent hipo or unsalicided N+/P+ poly resistors	0.80	µm	*	POLYSILICON (GDS layer 13)
13.24	Minimum length of HIPO resistor (i.e. separation of pplus regions)	3.60	µm	*	POLYSILICON (GDS layer 13)
17.20	pplus must be placed on the heads of the HIPO resistor			*	P+ IMPLANT (GDS layer 17)
17.21	Minimum pplus intersection with polysilicon of HIPO resistor	1.45	µm	*	P+ IMPLANT (GDS layer 17)
17.22	Minimum pplus extension on polysilicon of HIPO resistor or unsalicided P+ poly resistor	0.50	µm	*	P+ IMPLANT (GDS layer 17)
18.35	Minimum siprot intersection with pplus on heads of HIPO resistors	0.50	µm	*	SILICIDE PROTECT (GDS layer 18)
18.37	Minimum distance of siprot layer of non-salicided N+/P+ poly resistors to active area	0.80	µm	*	SILICIDE PROTECT (GDS layer 18)
26.1	Minimum hipo width	0.80	µm	*	HIPO (GDS layer 26)
26.2	Minimum hipo spacing	0.80	µm	*	HIPO (GDS layer 26)
26.3a	Minimum distance of HIPO to ACTIVE	0.80	µm	*	HIPO (GDS layer 26)
26.3b	Minimum distance POLY of non-silicided N+/P+ poly resistors to ACTIVE	0.80	µm	*	HIPO(GDS layer 26)
26.4	Minimum hipo distance to unrelated poly	1.00	µm	*	HIPO (GDS layer 26)
26.5	Minimum hipo distance to pplus	0.50	µm	*	HIPO (GDS layer 26)
26.6	Minimum hipo distance to nlddprotect if any is present.. Touching is allowed.	0.50	µm	*	HIPO (GDS layer 26)
26.7	Minimum hipo distance to nplusprotect if any is present. Touching is allowed.	0.50	µm	*	HIPO (GDS layer 26)
26.9	Polysilicon of HIPO resistor crossing hipo boundary is not allowed			*	HIPO (GDS layer 26)
26.10	Minimum hipo enclosure of polysilicon of HIPO resistor	1.60	µm	*	HIPO (GDS layer 26)
26.12	Minimum siprot extension on poly of HIPO resistor	0.40	µm	*	HIPO (GDS layer 26)

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

C035U (0.35 Micron) MATCHED RESISTORS Layout Rules



Note 1: Following is a list of good practices for pair of matched non-silicided polysilicon resistors in C035U. Below the list is a set of rules that must be followed.

-Both resistors in a matched pair should have identical properties and environment. Properties include width, length, number and spacing of elements in the bank. Environment includes (but is not limited to) proximity to unrelated metal, metal fill blocking using METDIS (GDS layer 63), etc.

-All resistors in a bank should be drawn parallel to each other.
-It is recommended (not checked) that all elements of a matched pair be equally spaced.
-It is recommended (not checked) that the heads of the dummy resistor be contacted and shorted through METAL1.

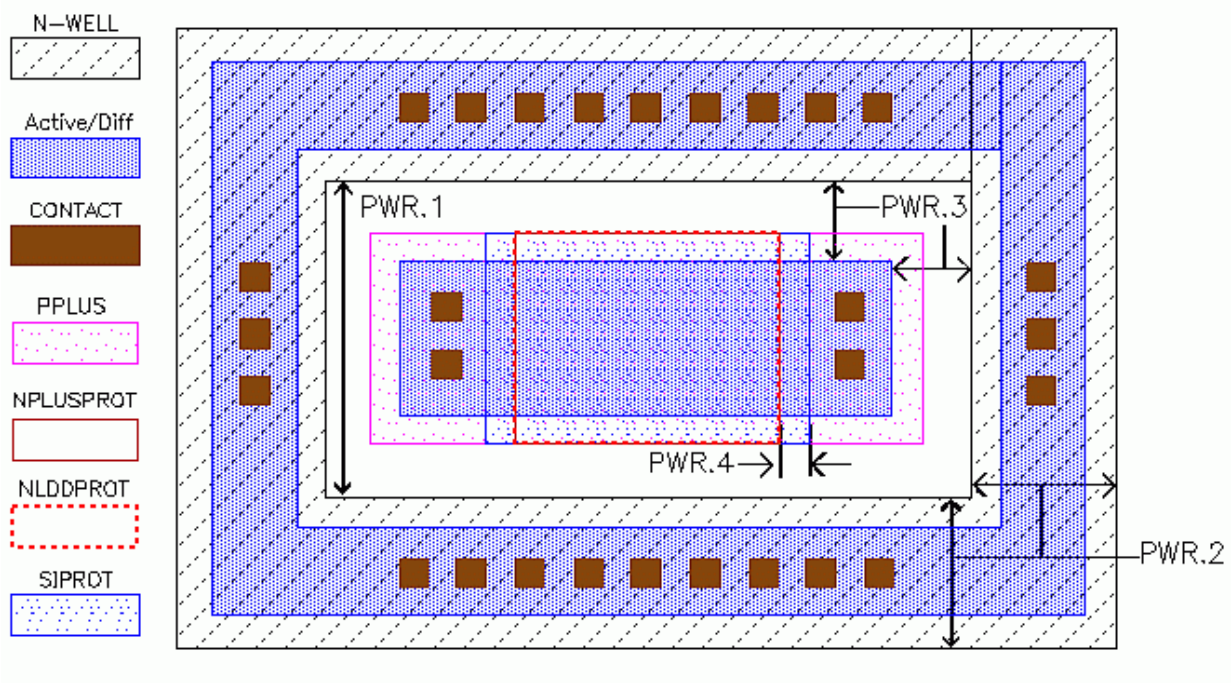
To disable checking for linearity and/or matching enclose the bank by LOWACC (GDS layer 108).

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
13.25	Minimum poly width of matched resistor	2.00	µm	*	
13.26	Minimum poly width of dummy resistor	2.00	µm	*	
13.30	All characterization work has been done on resistors without bends; matched resistors cannot have bends.			*	
13.31	Maximum spacing between polysilicon resistors and the closest related dummy resistors	3.00	µm	*	
17.23	Minimum resistor length for matched resistors	5.00	µm	*	
26.11	Minimum hipo enclosure of POLY of matched HIPO resistors	2.50	µm	*	
23.11	METAL1 over body of matched polysilicon resistors is not allowed			*	Matching can only be guaranteed for matched resistors covered by METDIS (GDS layer 63). METDIS prevents generation of dummy metal structures.
23.12	Minimum metal 1 distance to body of matched polysilicon resistor(Except on contact head)	2.00	µm	*	
23.13	Minimum metal 1 distance to related resistor	0.70	µm	*	
27.7	METAL2 over body of matched polysilicon resistors is not allowed			*	Matching can only be guaranteed for matched resistors covered by METDIS (GDS layer 63). METDIS prevents generation of dummy metal structures.
27.8	Minimum metal 2 distance to body of matched polysilicon resistor	2.50	µm	*	
34.7	METAL3 over body of matched polysilicon resistors is not allowed			*	Matching can only be guaranteed for matched resistors covered by METDIS (GDS layer 63). METDIS prevents generation of dummy metal structures.
34.8	Minimum metal 3 distance to body of matched polysilicon resistor	2.50	µm	*	
36.7	METAL4 over body of matched polysilicon resistors is not allowed			*	Matching can only be guaranteed for matched resistors covered by METDIS (GDS layer 63). METDIS prevents generation of dummy metal structures.

36.8	Minimum metal 4 distance to body of matched polysilicon resistor	2.50	µm	*	
53.7	METAL5 over body of matched polysilicon resistors is not allowed			*	Matching can only be guaranteed for matched resistors covered by METDIS (GDS layer 63). METDIS prevents generation of dummy metal structures.
53.8	Minimum metal 5 distance to body of matched polysilicon resistor	2.50	µm	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

C035U (0.35 Micron) PWELL ACTIVE RESISTOR Layout Rules



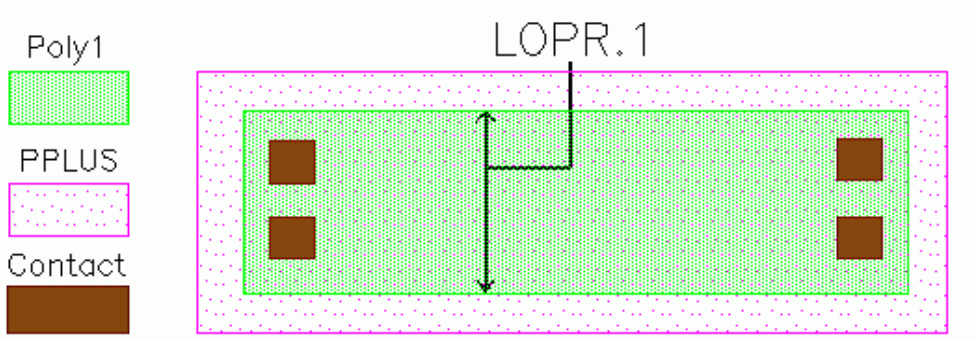
Note 1: PWell Active Resistor surrounded by NWell guardring (PWARNW) is a common C035U P-WELL resistor, useable to a max bias of 3.6 volts. The resistor is formed by drawing a ring of N-WELL (with active strap) that encloses a rectangle of ACTIVE area. The ends of the resistor are highly doped by drawing rectangles of PPLUS. PPLUS rectangles on both ends are line on line with a rectangle of SIPROT, NLDDPROT and NPLUSPROT, all of which cover the body of the resistor.

The length of the resistor is defined as the spacing between PPLUS rectangles parallel to current flow. The width of resistor is defined as the opening of the N-WELL ring perpendicular to current flow. The resistor must be marked using MRES (GDS layer 7) with "pwarnw".

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
PWR.1	Minimum width of PWELL resistor	5.00	µm	*	
PWR.2	Each PWELL resistor must be surrounded by a N+/Nwell guard ring			*	
PWR.3	Fixed Pwell implant enclosure of active area (resistor body and heads)	0.50	µm	*	
PWR.4	Fixed intersection of SIPROT on PPLUS implant of the resistor heads	0.40	µm	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

C035U (0.35 Micron) LOW OHMIC POLY RESISTOR Layout Rules



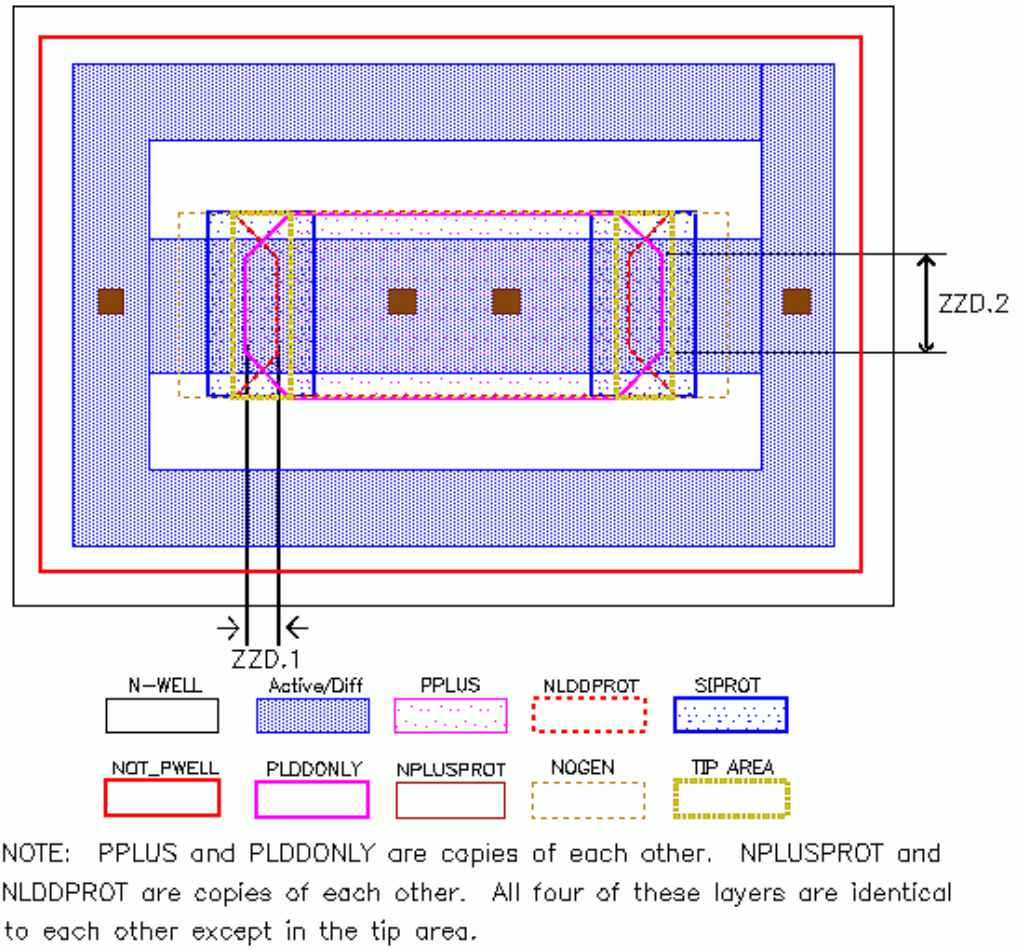
Note 1: Low Ohmic POlysilicon Resistor (LOPOR) is constructed by siliciding PPLUS doped POLYSILICON. The resistor is marked using MRES (GDS layer 7). Length of the resistor is defined by the distance between contacts on both ends in the direction of the current flow. Width of the resistor is defined by the size of POLYSILICON perpendicular to current flow.

The resistor is considered to be a LOW ACCuracy resistor by default.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
LOPR.1	Minimum width of LOPOR resistor	0.80	µm	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

C035U (0.35 Micron) ZENER ZAP DIODE (ZZD) Layout Rules



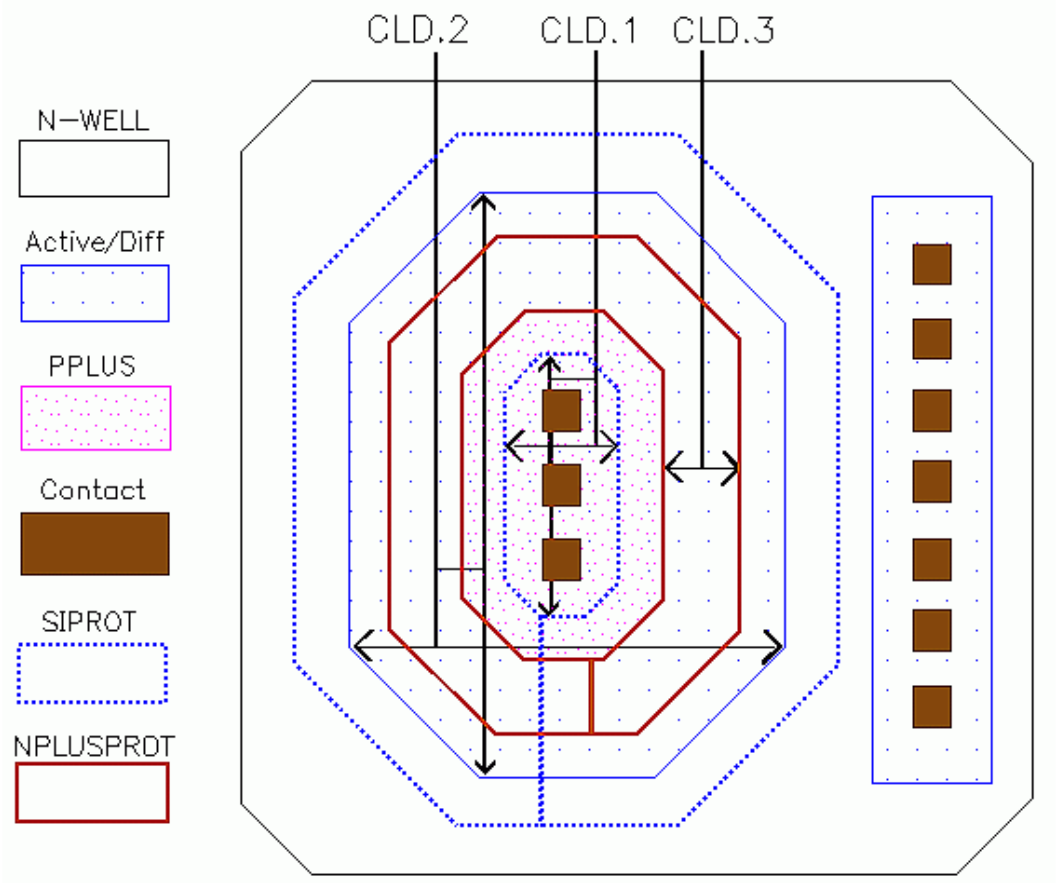
Note 1: The Zener Zap Diode (ZZD) represent unitary bit of One Time Programmable (OTP) memory. The diode is formed in a region defined as the tip. Each diode has two tips, placed with mirror symmetry around the anode. The following rules include exceptions that are valid only in the tip region.

UZZD represents the device prior to zapping, whereas ZZD represents a zapped device. From a layout perspective there is no difference between the two cells.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
ZZD.1	Fixed extension of PPLUS over NPLUS and NLDD at both side of the zapping junction (parameter “D”, version Z224)	0.20	µm	*	
ZZD.2	Fixed width of edge of zapping junction (parameter “T”, vers. Z224)	0.40	µm	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

C035U (0.35 Micron) PPLUS/NLDD CLAMPING DIODE Layout Rules



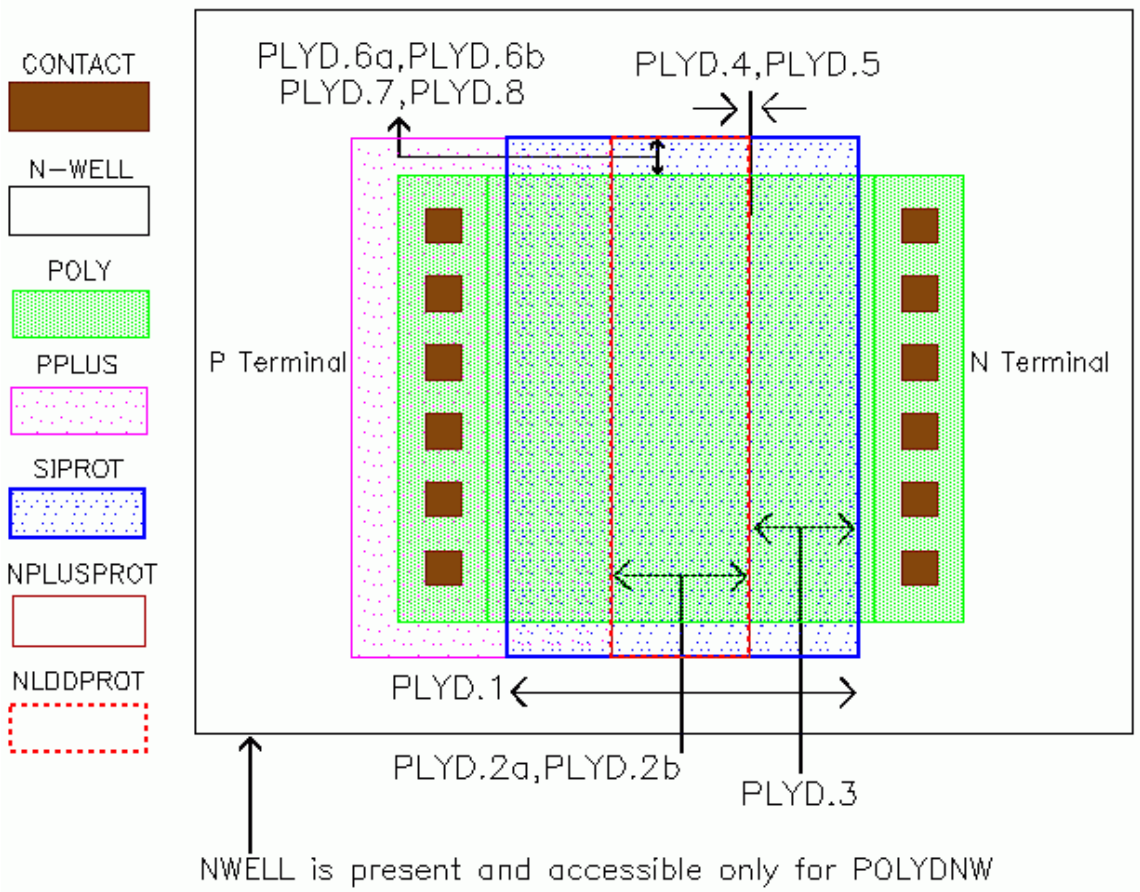
Note 1: PPLUS/NLDD Clamping Diode (CLIOD7) is constructed by surrounding a PPLUS ACTIVE region by an abutted NLDD ACTIVE region. This is a fixed layout device. The device is marked using MDIODE (GDS layer 4) with diode name cliod7. The marker completely encloses anode of the device. NPLUS implant is blocked by placing a ring of NPLUSPROT line on line with PPLUS of the anode. NPLUSPROT encloses the cathode active area completely. Silicide is blocked fully in the cathode region and is blocked partially in the anode region.

The shape of the diode is a stretched octagon. The diode is enclosed by N-WELL and the N-WELL strap serves as the cathode of the diode. NPLUSPROT does not enclose the well strap.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
CLD.1	Minimum P+ doped active area width (except 45° corners)	1.90	µm	*	
CLD.2	Minimum size (edge to edge) of diode active area (except 45° sides)	5.30	µm	*	
CLD.3	Fixed extension of NPLUSPROT ring outside the P+/Nldd junction: applied with a tolerance of ± 0.1 um	1.20	µm	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

C035U (0.35 Micron) POLY DIODE Layout Rules



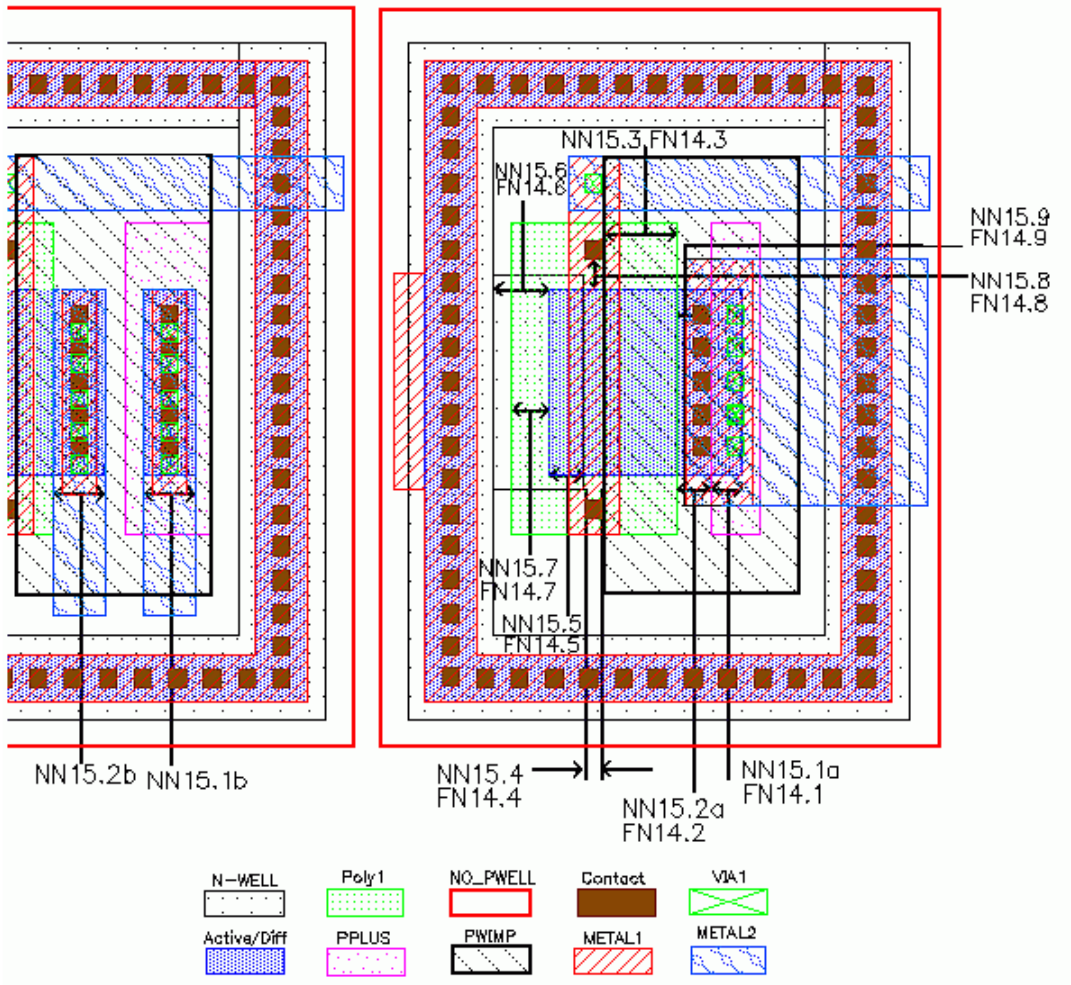
Note 1: The two implementations of poly diode, i.e. POLYD and POLYDNW differ in the presence of N-Well underneath the diode. The diode is never placed on an ACTIVE region. POLYD/POLYDNW model performance is guaranteed only for widths greater than or equal to 5µm.

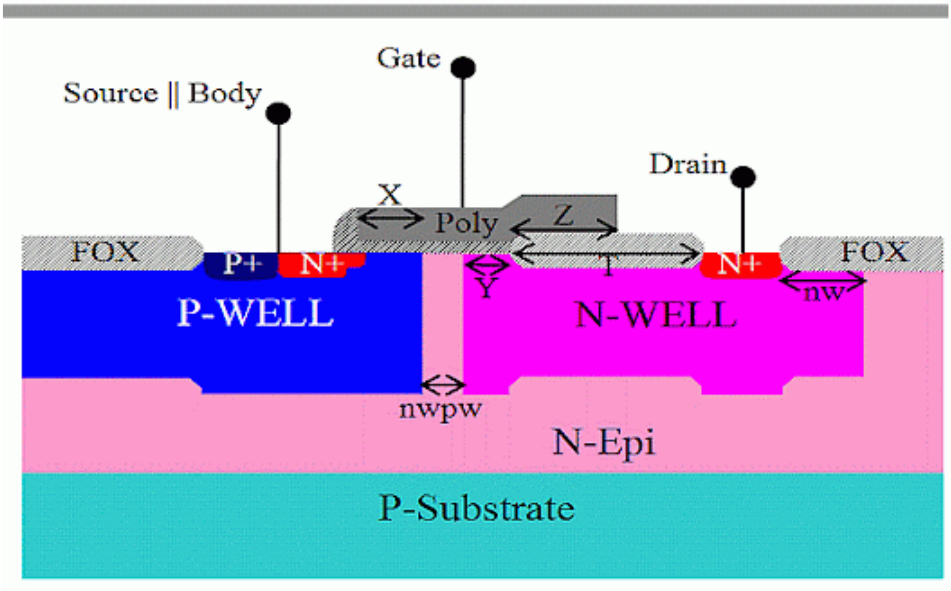
Rule Name	Rule Description	Rule	Units	Rule Type	Notes
PLYD.1	Fixed length of SIPROT intersection with POLY strip	3.40	µm	*	
PLYD.2a	Fixed overlap of NPLUSPROT with SIPROT (parameter Ldiode)	1.40	µm	*	
PLYD.2b	Fixed overlap of NLDDPROT with SIPROT (parameter Ldiode)	1.40	µm	*	
PLYD.3	Fixed overlap of PPLUS with SIPROT (P-terminal side)	1.00	µm	*	
PLYD.4	Fixed NPLUSPROT spacing to PPLUS of related P+/N- diode	0.00	µm	*	
PLYD.5	Fixed NLDDPROT spacing to PPLUS of related P+/N- diode	0.00	µm	*	
PLYD.6a	Minimum extension of NPLUSPROT on POLY	0.50	µm	*	

PLYD.6b	Minimum extension of NLDDPROT on POLY	0.50	µm	*	
PLYD.7	Minimum extension of SiPROT on POLY	0.50	µm	*	
PLYD.8	Minimum extension of PPLUS on POLY	0.50	µm	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

C035U (0.35 Micron) LNNDM15 AND LFNDM14 Layout Rules





Note 1: LNNDM15 and LFNDM14 both have identical core rules. The relationship between the two devices is as follows: LNNDM15 = LFNDM14 with W=8µm. LNNDM15 is application limited and is only used in the One Time Programmable (OTP) memory. LFNDM14 is a general use device.

For both these devices, isolation scheme depends on specific technology in the C035U family.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
NN15.1a	Minimum width of P+ ACTIVE (bulk), perpendicular to poly finger, when abutted to source active.	0.50	µm	*	Rule for LNNDM15
NN15.1b	Minimum width of P+ ACTIVE (bulk), perpendicular to poly finger, when not abutted to source active.	0.80	µm	*	Rule for LNNDM15
NN15.2a	Fixed width N+ ACTIVE source, perpendicular to poly finger, when abutted to the P+ active (bulk connection)	0.80	µm	*	Rule for LNNDM15
NN15.2b	Fixed width N+ ACTIVE source, perpendicular to poly finger, when not abutted to the P+ active (bulk connection)	1.00	µm	*	Rule for LNNDM15
NN15.3	Fixed POLY intersection with PWELL (perpendicular to poly finger). => X	1.00	µm	*	Rule for LNNDM15
NN15.4	Fixed spacing between NWELL drain and PWELL (perpendicular to poly finger) at the side covered by the poly gate => nwpw	0.50	µm	*	Rule for LNNDM15
NN15.5	Fixed ACTIVE intersection with NWELL, perpendicular to poly => Y	0.50	µm	*	Rule for LNNDM15
NN15.6	Fixed spacing N+ ACTIVE source and drain => T	1.20	µm	*	Rule for LNNDM15
NN15.7	Fixed Poly extension beyond ACTIVE (towards drain) => Z	0.60	µm	*	Rule for LNNDM15
NN15.8	Minimum POLY contact spacing to active area (derived from r19.6)	0.40	µm	*	Rule for LNNDM15
NN15.9	Minimum POLY edge to source contact spacing (derived from r19.5)	0.40	µm	*	Rule for LNNDM15
FN14.1	Minimum width of P+ ACTIVE (bulk), perpendicular to poly finger; the P+ ACTIVE is always abutting.	0.50	µm	*	Rule for LFNDM14
FN14.2	Fixed width N+ ACTIVE source, perpendicular to poly finger; the N+ ACTIVE source is always abutting to the P+ ACTIVE (bulk connection)	0.80	µm	*	Rule for LFNDM14
FN14.3	Fixed POLY intersection with PWELL (perpendicular to poly finger). => X	1.00	µm	*	Rule for LFNDM14
FN14.4	Fixed spacing between NWELL drain and PWELL (perpendicular to poly finger) at the side covered by the poly gate => nwpw	0.50	µm	*	Rule for LFNDM14

FN14.5	Fixed ACTIVE intersection with NWELL, perpendicular to poly => Y	0.50	µm	*	Rule for LFNDM14
FN14.6	Fixed spacing N+ ACTIVE source and drain => T	1.20	µm	*	Rule for LFNDM14
FN14.7	Fixed Poly extension beyond ACTIVE (towards drain) => Z	0.60	µm	*	Rule for LFNDM14
FN14.8	Minimum POLY contact spacing to active area (derived from r19.6)	0.40	µm	*	Rule for LFNDM14
FN14.9	Minimum POLY edge to source contact spacing (derived from r19.5)	0.40	µm	*	Rule for LFNDM14

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

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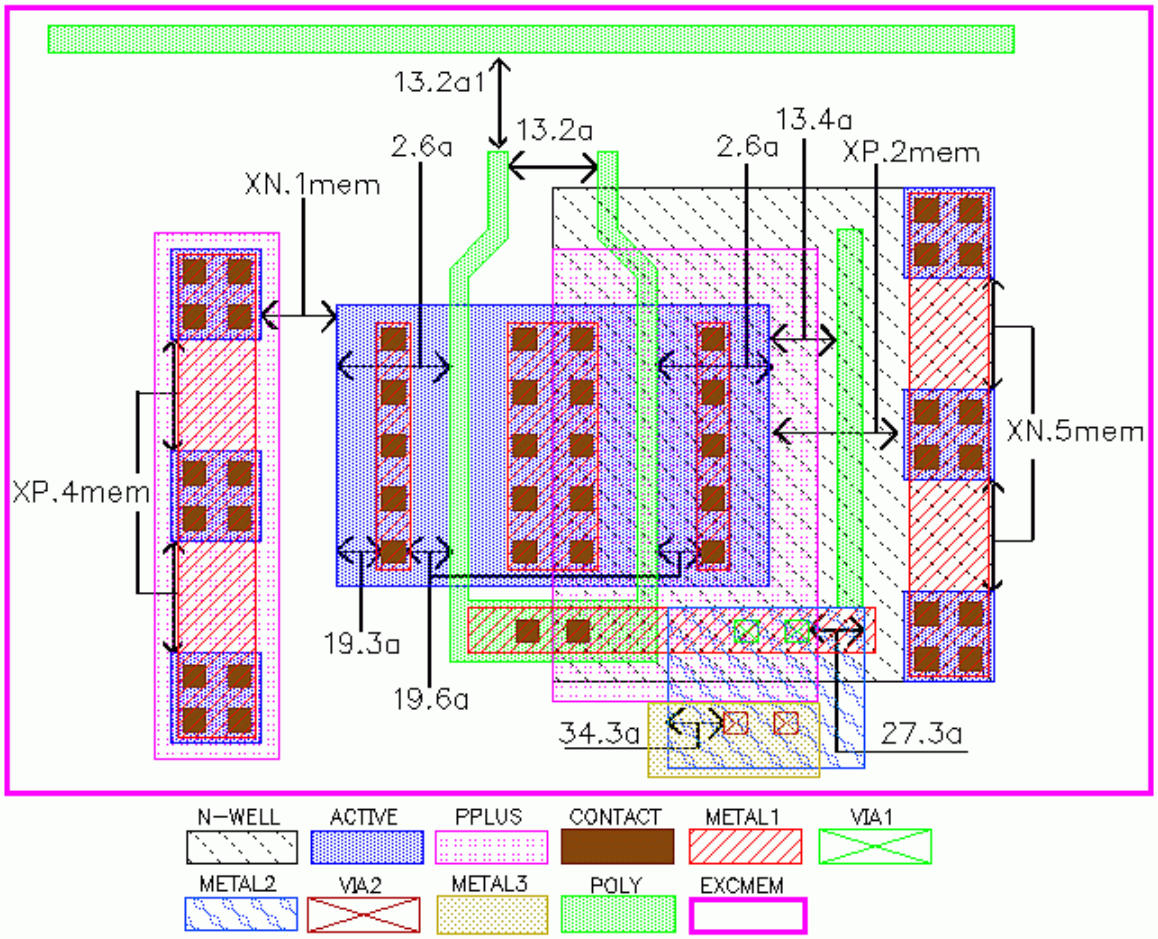
C035U (0.35 Micron) HIGH-DENSITY MEMORIES Layout Rules



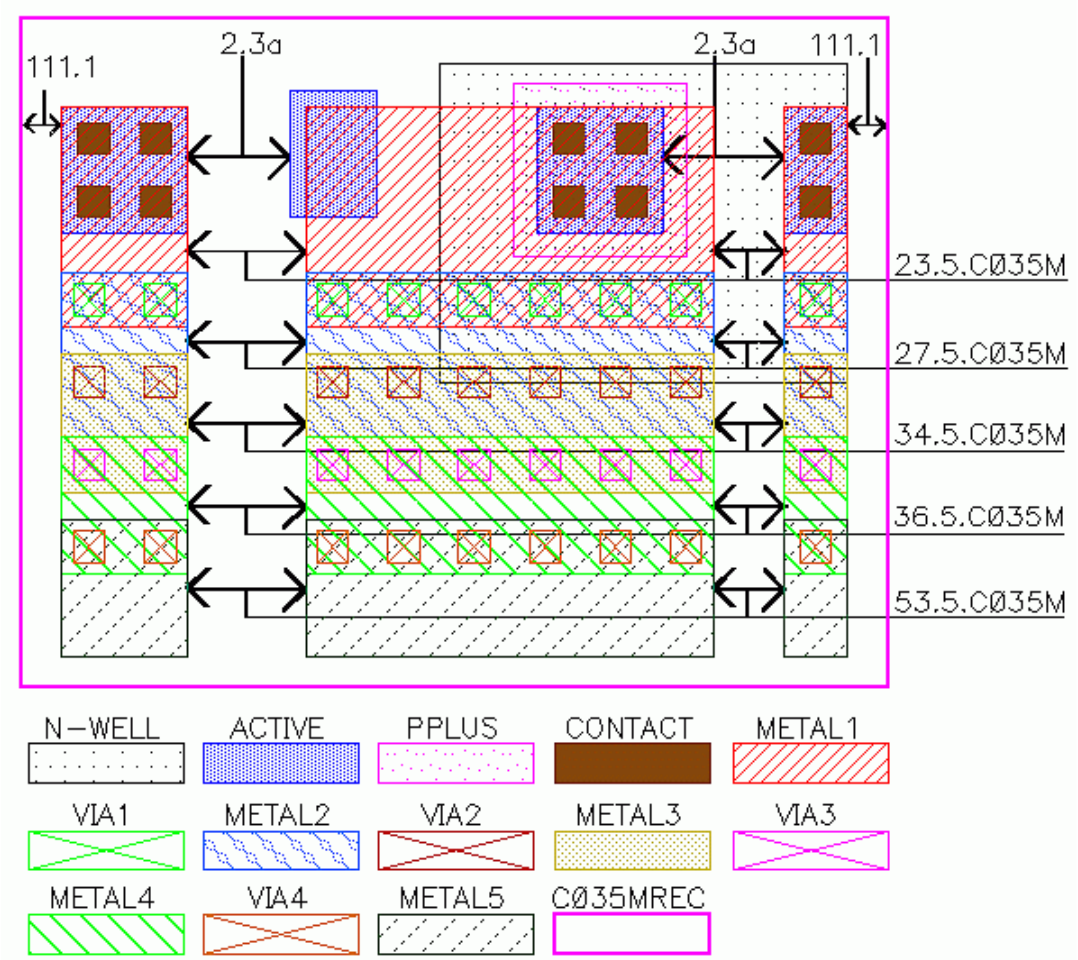
Note 1: In C035U high density memories some of the normal layout rules are violated to achieve competitive bit cell sizes. GDS layer 97 (excmem) is used for recognition. excmem applies to both core and peripheral circuitry of the memory.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
2.6a	Minimum active area enclosure of polysilicon in high-density memories (under excmem)	0.625	µm	*	
13.2a1	Minimum polysilicon spacing between the outside edge of an endcap of a narrow transistor (Length less than or equal to 0.5 um) and any other polysilicon (under excmem)	0.35	µm	*	
13.4a	Minimum polysilicon spacing to active area in high-density memories (under excmem)	0.15	µm	*	
19.3a	Minimum active area enclosure of contact in high-density memories (under excmem)	0.15	µm	*	

19.6a	Minimum active area contact spacing to polysilicon gate (under excmem)	0.275	µm	*	
27.3a	Minimum metal 2 enclosure of via 1 in high-density memories (under excmem)	0.10	µm	*	
34.3a	Minimum metal 3 enclosure of via 2 in high-density memories (under excmem)	0.10	µm	*	
XP.2mem	Maximum distance between connected P+ active area in NWELL from NWELL strap (under excmem)	50.00	µm	*	Latch-Up Rules
XP.4mem	Maximum spacing of p-active in p-wells (when the p-well contains n-active), when the well is in memories marked with excmem.	71.00	µm	*	Latch-Up Rules
XN.1mem	Maximum distance between connected N+ active area in PWELL from PWELL strap (under excmem)	50.00	µm	*	Latch-Up Rules
XN.5mem	Maximum spacing of n-active in n-wells (when the n-well contains p-active), when the well is in memories marked with excmem.	100.00	µm	*	Latch-Up Rules

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

C035U (0.35 Micron) USING C035M IP Layout Rules



Note 1: For backward compatibility and IP re-use, the feature of C035M layout port into C035U is available. Given IP in C035M may be used by simply dropping in the layout into a C035U design. To ensure functionality, the following set of guidelines must be followed.

-C035M layout in C035U design must be completely enclosed by C035MREC (GDS layer 111).
-If a schematic is ported and simulated with C035U models, C035MREC must not be drawn.
-C035MREC is not necessary on HV or ESD components.
-FLASH EEPROM circuit (not the memory cell matrix) must be enclosed by C035MREC.
-Any N-WELL regions, RNWELL regions and n-well resistors in a C035M layout are no longer electrically isolated after move to C035U.

Mask generation is adapted to take into account differences in ACTIVE area pitch between C035M and C035U. ACTIVE area biased depending on scenario are as follows:

-If enclosed in MFLASH (only for memory cell matrix), a bias of 0.100µm/side.
-If enclosed in C035MREC, a bias of 0.075µm/side unless covered by MFLASH
-All other cases, a bias of 0.050µm/side.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
2.3a	Minimum active area spacing under layer c035mrec	0.70	µm	*	
111.1	Minimum c035mrec enclosure of active area	0.70	µm	*	
C035U.1	NWELL and RNWELL regions inside the same n-epi pocket must be at the same potentional			*	
23.5.C035M	Minimum wide metal 1 spacing (metal width > 10um) to any metal 1 under c035mrec	0.60	µm	*	WIDE METAL SPACING
27.5.C035M	Minimum wide metal 2 spacing (metal width > 10um) to any metal 2 under c035mrec	0.70	µm	*	WIDE METAL SPACING
34.5.C035M	Minimum wide metal 3 spacing (metal width > 10um) to any metal 3 under c035mrec	0.70	µm	*	WIDE METAL SPACING
36.5.C035M	Minimum wide metal 4 spacing (metal width > 10um) to any metal 4 under c035mrec	0.70	µm	*	WIDE METAL SPACING
53.5.C035M	Minimum wide metal 5 spacing (metal width > 10um) to any metal 5 under c035mrec	2.00	µm	*	WIDE METAL SPACING

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

C035U (0.35 Micron) Core CMOS Design Rules

Bonding PADs

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BONDING PADS

Introduction

PASSIVATION (GDS layer 31) defines the cut-out areas for bonding pads and test pads that results in an opening in the nitride passivation. No openings are allowed except over bonding pads and test pads. Minimum pad opening and minimum pad spacing is defined by assembly layout rules (1000033).

PAD is defined as the top metal area covered by NITRIDE (GDS layer 31). Build-up of a PAD is as shown below:

Triple Metal Process: METAL1 → VIA1 array → METAL2 → VIA2 array → METAL3
Quadruple Metal Process: Triple Metal Process → VIA3 array → METAL4
Pentuple Metal Process: Quadruple Metal Process → VIA4 array → METAL5

One of the Above → NITRIDE

Even number VIA are superimposed on each other. Odd number VIA are superimposed on each other. Even and odd VIA are shifted by 1.0µm from each other in both X- and Y- directions.

ACTIVE is not allowed under PAD. POLYSILICON is not allowed under PAD. Only rectangular shape PAD is allowed.

The minimum pad opening and the minimum pad spacing are package type specific and are defined by the assembly layout rules (1000033).

It is recommended that a PAD to interconnect metal transition be handled through a fillet and lead away. The related rules are given under Bonding Pad Layout Rules. Please refer to 1000033 for additional information.

Rules in 1000033 apply to bonding pads as well as manual probing pads. Manual probing pads are used for direct probing on wafer, and are typically used for engineering development test chips and prototyping applications. In special cases additional layout rules are introduced (for example, manual probing, Focused Ion Beam drilling and probing, etc.).

All of PAD rules refer to pads with single bond. For specifications regarding double or triple bonding, please refer to 1000033.

Reliability Considerations:

Whenever die size and area considerations allow, a larger than minimum PAD should be used placed on a larger pitch than minimum allowed for a package. This is especially valid for products with high reliability requirements, such as automotive, high power, etc. This also allows use of thicker wires that can be made longer, hence simplifying the process of chip assembly.

Active and passive components with precision requirements must be located as far away from bonding pads as possible. This practice reduces parametric shifts due to mechanical stress of the package.

Large metal busses should be avoided at the edge of the die, especially in the corners. 45° corners should be used in such cases.

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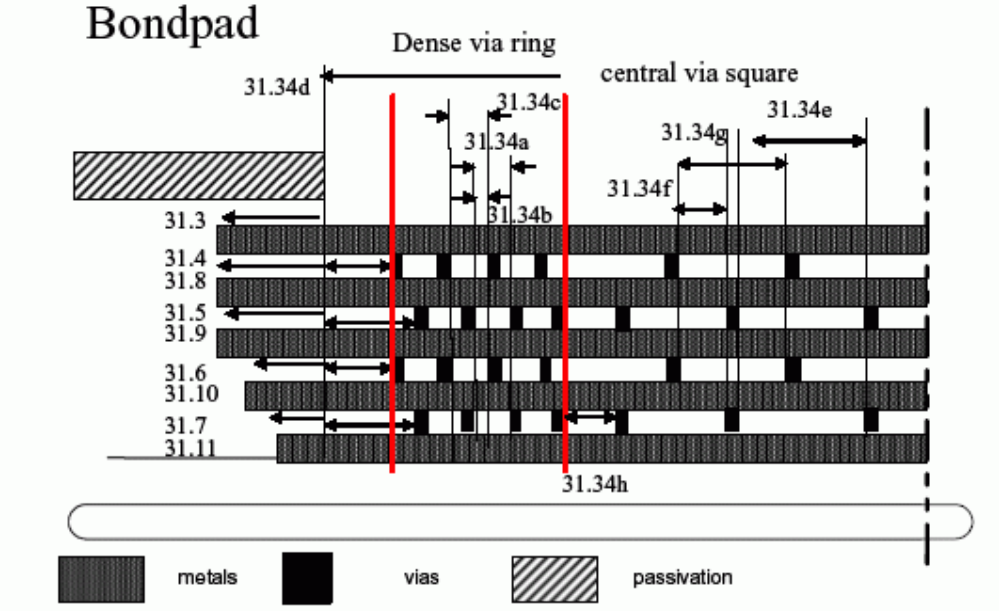
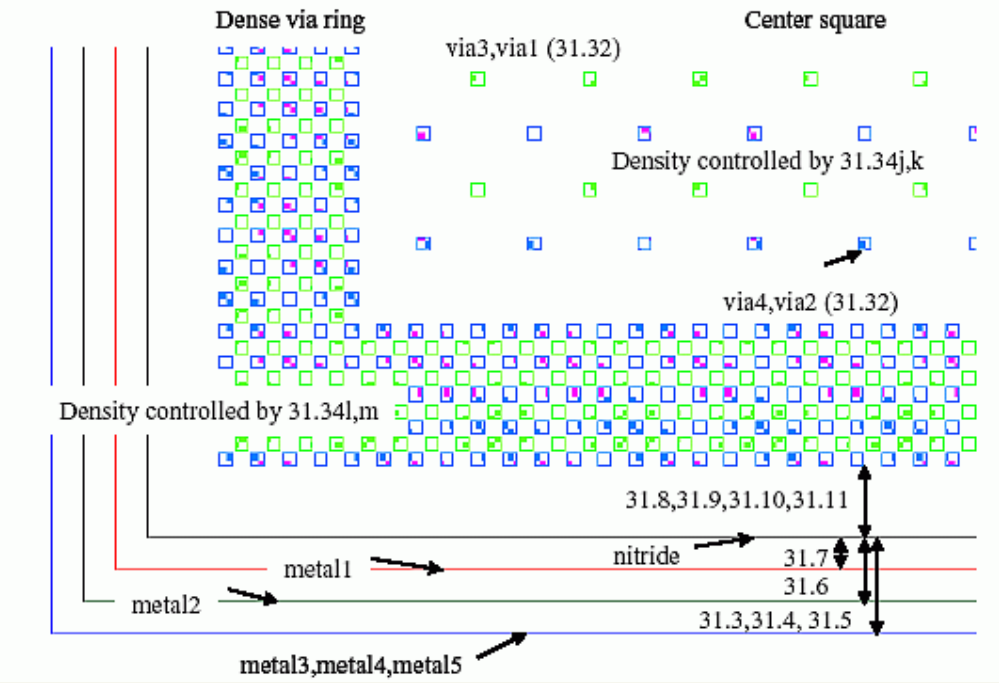
C035U (0.35 Micron) BONDING PADS Layout Rules





Rule Name	Rule Description	Rule	Units	Rule Type	Notes
31.1	Minimum nitride opening for bondpads: this is a package related rule, refer to doc. 1000033; absolute minimum value	2.00	µm	*	See Assembly spec 1000033. Value H

31.1b	Minimum nitride opening for manual probepads	2.00	µm	*	See Assembly spec 1000033. Values P2-H, P1-H
31.2a	Minimum pad window spacing (nitride): this is a package related rule, refer to doc. 1000033; absolute minimum value	10.00	µm	*	See Assembly spec 1000033. Value K
31.2c	Minimum spacing between manual probepads	11.00	µm	*	See Assembly spec 1000033. Value K
31.3	Minimum metal 5 enclosure of pad	3.00	µm	*	See Assembly spec 1000033. Value K
31.3b	Minimum related metal enclosure of manual probepads	3.00	µm	*	
31.4	Minimum metal 4 enclosure of pad	3.00	µm	*	
31.5	Minimum metal 3 enclosure of pad	3.00	µm	*	
31.6	Minimum metal 2 enclosure of pad	2.00	µm	*	
31.7	Minimum metal 1 enclosure of pad	1.00	µm	*	
31.8	Minimum nitride enclosure of pad via 4	2.00	µm	*	Checked for layout with METAL5
31.9	Minimum nitride enclosure of pad via 3	2.00	µm	*	Checked for layout with METAL4 and above
31.10	Minimum nitride enclosure of pad via 2	2.00	µm	*	
31.11	Minimum nitride enclosure of pad via 1	2.00	µm	*	
31.20	Minimum n-well enclosure of pad (note that the presence of a n-well is not mandatory)	8.00	µm	*	Exception for power metal bondpad
31.21	Minimum rnwell enclosure of pad (note that the presence of a rnwell is not mandatory)	8.00	µm	*	Exception for power metal bondpad
31.22	Minimum metal fillet width along the pad; assembly rules require that the minimum fillet width is at least 50% of the pad size; only specific	30.00	µm	*	A requirement from MIL-STD 883/2010 is to have a fillet as large as at least half of the bondpad width, to minimise the electrical stress at the connection area.
31.23	Minimum metal fillet length	15.00	µm	*	
31.24	Minimum metal leadaway width	8.00	µm	*	
31.25	Minimum metal leadaway length	15.00	µm	*	
31.26	Contact under pad is not allowed; minimum pad spacing to contact	11.00	µm	*	Exception for power metal bondpad
31.27	Polysilicon under pad is not allowed; minimum pad spacing to poly	11.00	µm	*	Exception for power metal bondpad
31.28b	Minimum pad metal to pad metal spacing = package related rule, refer to doc. 1000033; absolute minimum	3.00	µm	*	See Assembly spec 1000033. Value F
31.28c	Minimum manual probing pad spacing to any metal	5.00	µm	*	
31.29	Minimum pad spacing to any via	11.00	µm	*	
31.30	Active area under pad is not allowed; minimum pad spacing to active	11.00	µm	*	

31.32	Via 3 and Via 1 array must be superimposed in the pad			*	Checked for layout with METAL4 and above; both for dense via ring and center square
31.33	Via 4 and Via 2 array must be superimposed in the pad			*	Checked for layout with METAL5; both for dense via ring and center square
31.34a	Fixed spacing of via 1 in the dense via ring	0.60	µm	*	
31.34b	Fixed spacing between via 1 and via 2 in the dense via ring. They must be staggered in both rows and columns.	0.10	µm	*	
31.34c	Fixed spacing of via 2 in the dense via ring.	0.60	µm	*	
31.34d	Maximum enclosure central square by nitride	6.70	µm	***	This rule is not checked directly, but is used as a reference for other pad rules.
31.34e	Fixed spacing between via 1 in the center square of the bondpad.	3.10	µm	*	
31.34f	Minimum spacing between via 1 and via 2 in the central square of the bondpad. They must be staggered in both rows and columns.	1.35	µm	*	
31.34g	Fixed spacing between via 2 in the central square of the bondpad.	3.10	µm	*	
31.34h	Minimum spacing of via 1 in the dense via ring to via 1 in the center square.	0.60	µm	*	
31.34j	Minimum Via 1 density in the center square (%)	0.80		*	
31.34k	Minimum Via 2 density in the center square (%)	0.80		*	
31.34l	Minimum Via 1 density in the dense via ring (%)	13.00		*	
31.34m	Minimum Via 2 density in the dense via ring (%)	13.00		*	
31.35a	Minimum nitride spacing to unrelated metal 5 = package related rule, refer to doc. 1000033; absolute minimum	6.00	µm	*	See Assembly spec 1000033. Value F
31.35b	Minimum nitride spacing to unrelated metal 4 = package related rule, refer to doc. 1000033; absolute minimum	6.00	µm	*	See Assembly spec 1000033. Value F
31.35c	Minimum nitride spacing to unrelated metal 3 = package related rule, refer to doc. 1000033; absolute minimum	6.00	µm	*	See Assembly spec 1000033. Value F
31.35d	Minimum nitride spacing to unrelated metal 2 = package related rule, refer to doc. 1000033; absolute minimum	7.00	µm	*	See Assembly spec 1000033. Value F
31.35e	Minimum nitride spacing to unrelated metal 1 = package related rule, refer to doc. 1000033; absolute minimum	8.00	µm	*	See Assembly spec 1000033. Value F

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

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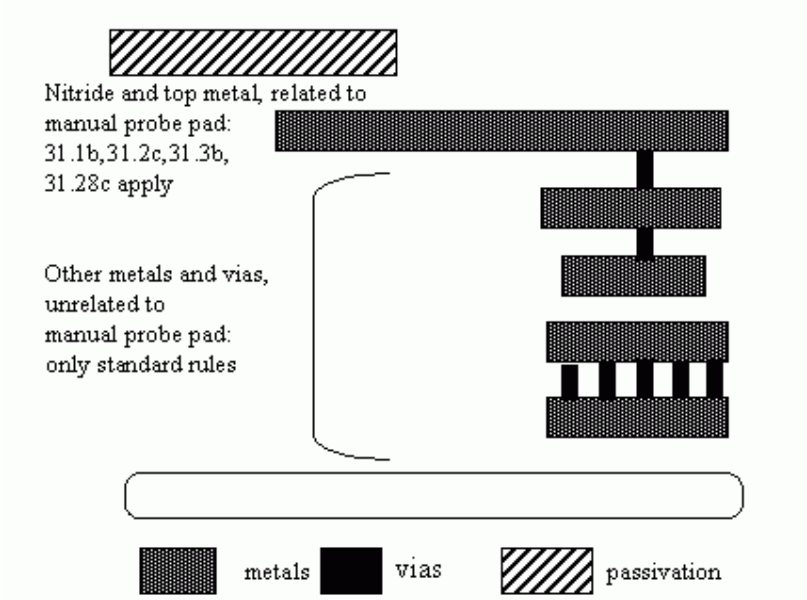
(Confidential)
DES-0005 Rev: 11.0, 05-Oct-2010

C035U (0.35 Micron) MANUAL PROBE PADS Layout Rules



Note 1: Manual probe pads are built with typically only one single drawn metal plate enclosing the NITRIDE layer. Generation of metal fill must be prevented by drawing METDIS enclosing the drawn metal plate. The pad is marked by "mxprobe" using NREC (GDS layer 118) where x is the metal level being used to probe. Additionally the following rules apply to manual probe pads.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
PAD.1	WARNING: These manual probe pads are allowed only for manual probing and FIB: verify abuse via bonding checker!			*	
PAD.2	WARNING: Manual probe pads must be opened only at the level of the top metal: verify if the metal level of this pad is the highest used in the chip			*	
PAD.3	Manual probe pads must be enclosed by NORING layer			*	
PAD.4	Manual probe pads must be enclosed by METDIS layer			***	
PAD.5	There should be no open manual probe pads on the final production version of the product			*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

This information is Confidential and Controlled. The current revision of this information will only be available on this intranet page.

Power Metal Bond Pad Layout Rules

A power metal bondpad is a standard bondpad covered with power metal.

A dedicated assembly CAD set up must be used for the generation of Bond Pads. The setup is described in Application Note: “BDS-GDS flow Rev. 2.6 (pages 21-23).” These rules are checked by “Bonding Diagram Checker” and not by the DRC.

Bonding-on-Active

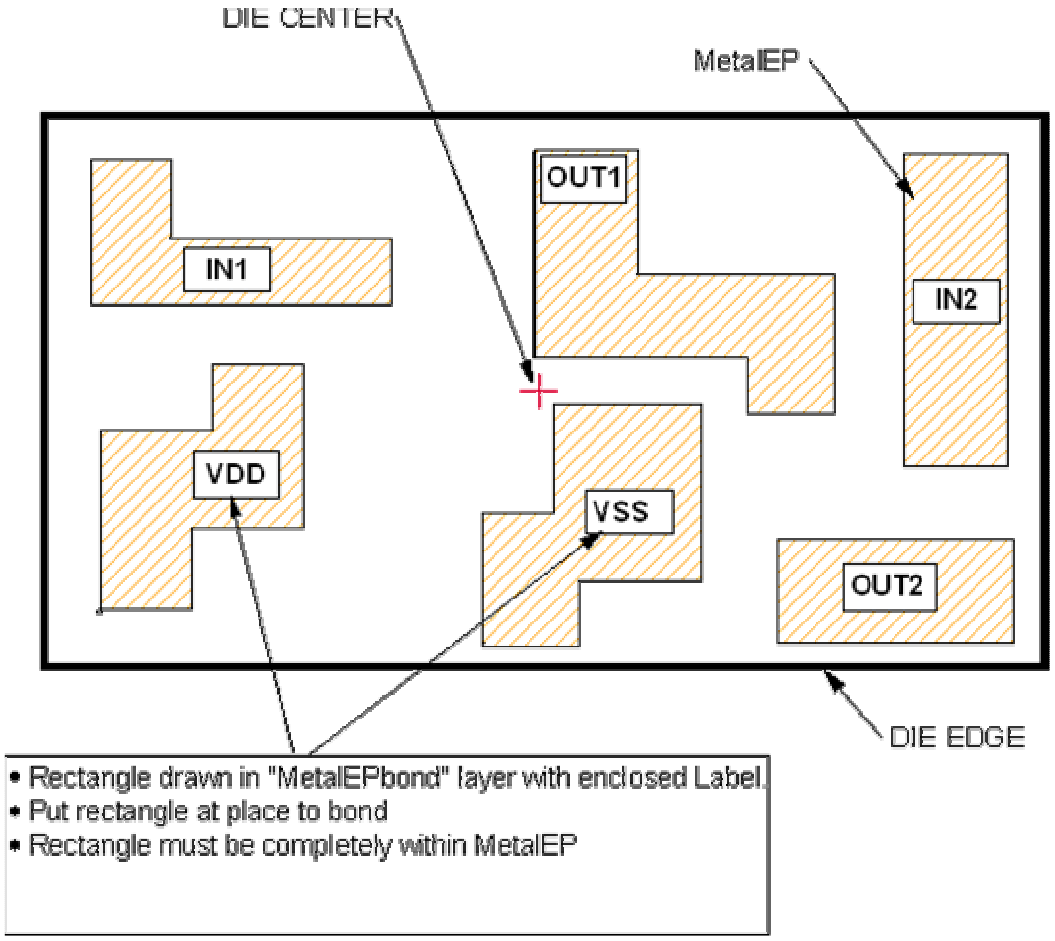
- Bonding-on-Active is allowed. Use of power metal allows “Bonding-On-Active (aka, Circuits Under Pad)”; that is, bonding can be done anywhere on Power Metal.

Bond Pad and Probe Pad Location Indicator

To assure correct bond location on MetalEP pads and to enable the sort process, the following schemes are put in place:

Each location for wirebonding, or test probe placement for Sorting, is identified by a rectangle drawn in layer “MetalEPbond”.

A netlist (a bonding pin out file) must be generated in Excel file format with the X,Y coordinates of center of these Text rectangles from the center of the die along with its function name. This netlist is used for wafer test Probe card generation and for bonding diagram.

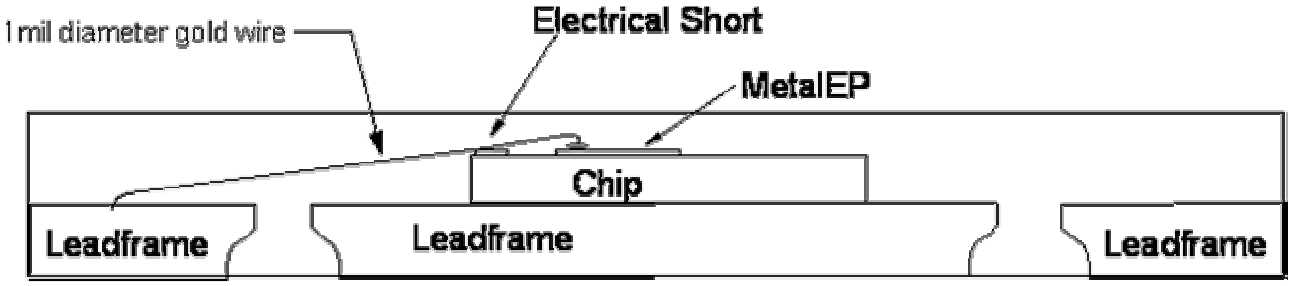


The minimum MetalEP Bond Pad size is dependent on the wire diameter (D) and the number of bonds:

For single bond: X: 100+3D µm; Y: 100+3D µm
For double bond: X: 100+3D µm; Y: 100+6.8D µm
For triple bond: X: 100+3D µm; Y: 100+10.6D µm

Bond Wire Loop Shape for power metal BoA:

Warning: there exists a risk of electrical short between a wire bond loop and a power metal plate or track at the periphery of the circuit. This is because the power metal is not passivated. Designers must review their assembly requirements versus their layout, with Assembly engineering.



C035U (0.35 Micron) Core CMOS Design Rules

Scribe Lane and Edge of Die

DES-0005 Rev: 11.0

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SCRIBE LANE AND EDGE OF DIE

Introduction

This section covers the process layout rules for the scribe lane and the edge of die. The introduction covers definitions and general requirements.

- The purpose of this section is to define a scribe lane and an edge of die, which will give a moisture resistant die, without the possibility that cracks generated during sawing can propagate into the die.
- For the following rules, all dimensions are in microns and refer to the inner edge of the die seal ring. The seal ring width is 10 µm. In the table (see section Layout of Edge of Die below), 0 means internal edge of the die seal ring (near the circuit), and 10 is the outer edge of the die seal ring (towards scribe lane).
- Interconnection of the metal layers in the seal ring is through 0.4 µm wide contact or via trenches (fixed contact and via size rules 19.1, 25.1, 32.1, 35.1 and 52.1 are not applicable in the die seal ring). For the layers contact, via2 and via 4, three parallel trenches are used; for via 1 and via 3, two parallel trenches are used. The distance between the trenches is 2.2 µm.
- These rules are taken into consideration AFTER the circuit has been delivered to the MaskPrep Group, therefore they are not checked in the design and layout verification process.
- REFER TO ON SEMICONDUCTOR DOC. 1000033 FOR ASSEMBLY RELATED RULES (see drawing of cross-section of die seal ring):

Rule Name	Rule description	Rule	Notes
AssyRule.1:	Minimum distance between outer seal ring edges of neighbouring die	M	
AssyRule.2:	Minimum bond pad metal spacing to scribe edge (outer seal ring edge)	E	
AssyRule.3:	Minimum bond pad metal spacing to unrelated metal	F	
AssyRule.4:	Minimum opening between passivation edge of the die and passivation edge of test patterns in scribe lane.	N	

Layout of Edge of Die

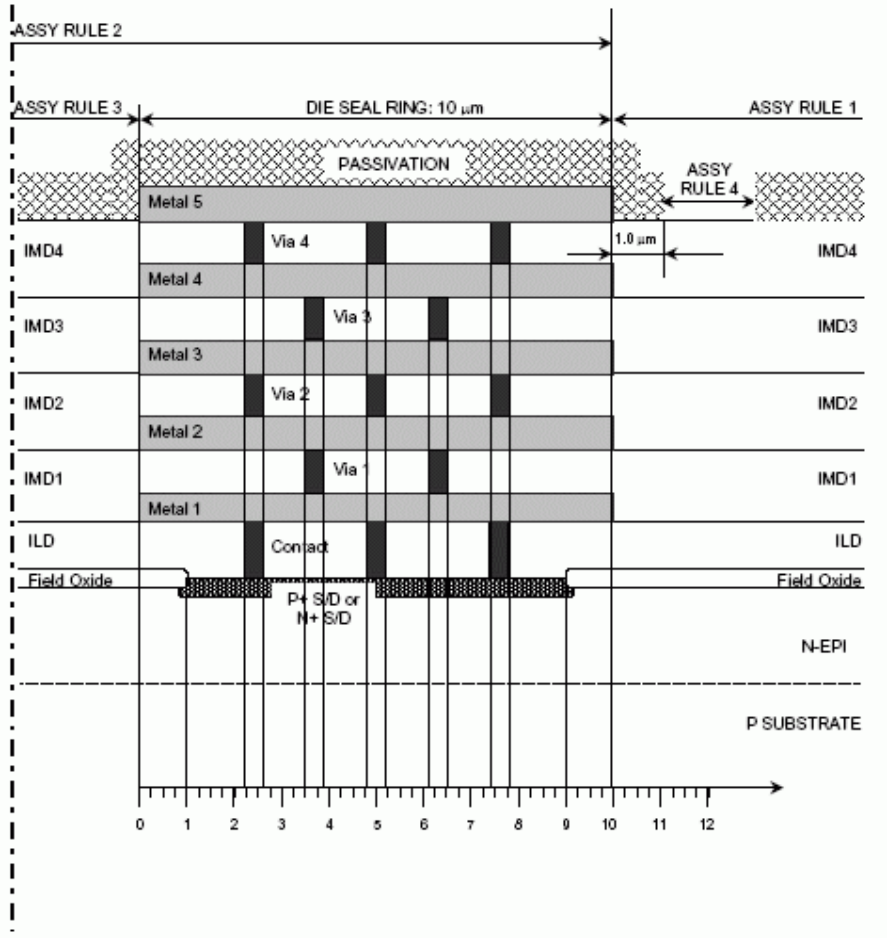
The information hereafter is limited to the core CMOS of the C035U-based technology family. For each individual process technology, e.g. I3T80U, additional layers may have to be defined.

Also, the presence or absence of common CMOS layers nwell and pplus, and their derived layers pwell and nplus, is technology dependent .

These rules are taken into consideration AFTER the circuit has been delivered to the MaskPrep Group, therefore they are not checked in the design and layout verification process.

Rule Name	Layer	Drawn ?	From	To
DSR.1a.	nwell:	**Process Technology dependent rule**		
DSR.1b.	not_pwell:	**Process Technology dependent rule**		
DSR.2.	active	yes	1.0	9.0
DSR.3.	poly	no		
DSR.4a.	pplus:	**Process Technology dependent rule**		
DSR.4b.	nplus:	**Process Technology dependent rule**		
DSR.5.	siprot	no		
DSR.6.	contact	yes (3 trenches)	2.2 4.8 7.4	2.6 5.2 7.8
DSR.7.	metal 1	yes	0.0	10.0
DSR.8	via 1	Yes (2 trenches)	3.5 6.1	3.9 6.5
DSR.9.	metal 2	yes	0.0	10.0
DSR.17	mimc	no		
DSR.10.	via 2	Yes (3 trenches)	2.2 4.8 7.4	2.6 5.2 7.8
DSR.11.	metal 3	yes	0.0	10.0
DSR.12.	via 3	Yes (2 trenches)	3.5 6.1	3.9 6.5
DSR.13.	metal 4	yes	0.0	10.0
DSR.14.	via 4	Yes (3 trenches)	2.2 4.8 7.4	2.6 5.2 7.8
DSR.15.	metal 5	yes	0.0	10.0
DSR.16.	nitride	no		

Layout of Edge of Die - CROSS SECTION



EDGE OF DIE - PLACEMENT RULES

To drive the placement of circuit element in an optimised layout of the final die, a special system layer is considered ("y9" IGS #0, type 63 – from now on called ENDCIRC) which is always used as outline of the layout data. It should enclose all drawn data according to the rules below and assuming that a VSS bus ring is present.

At the moment the Outlineparamscribe frame is placed around the die, the shape of this layer is the inner edge of this frame. The real Paramscribe will be then added during the mask preparation, and only at that moment each side will be rounded to a multiple of 10 µm, so that the final Paramscribe will never cross the ENDCIRC ("y9") perimeter.

The use of ENDCIRC ("y9") during the layouting phase allows also an easy calculation of the coverage of some critical layers (POLY, METAL) to decide whether dummy patterns must be added to have a better process control during related lithography and etching steps.

For the placement of ENDCIRC ("y9") perimeter around the circuit, the presence and extension of TEXT and other labels is usually neglected. The DRC has to be run when the Outlineparamscribe cell is placed around the top cell of the chip, before mask preparation.

In the case of engineering testchip, often not provided with paramscribe, this layer must be drawn as chosen outer perimeter of the drawn area.

Two options are available in the ParamScribe: "Closed guardring" (like a VSS bus) and "Other".

Their choice is verified at mask preparation and results in a different extension of the zone "A" in the DSR cross-section of the previous page: this will be respectively min (5+2.5) µm and min (11.5+2.5) µm, therefore the ENDCIRC profile can be always abutted to the outer circuit data.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
END.1	Minimum ENDCIRC enclosure of any physical layout data (excluding marker layers) Check not needed for layer viax, nitride	0.00	µm	*	
END.2	Minimum ENDCIRC corner truncation	86.00	µm	*	
END.3	Minimum ENDCIRC enclosure of nitride (rule K)	3.00	µm	*	
END.7a	Minimum ENDCIRC enclosure of poly, for matched or high accuracy CMOS transistors and poly resistors	30.00	µm	*	
END.7b	Minimum ENDCIRC enclosure of poly, with no electrical constraints	8.00	µm	*	
END.9	Minimum MIMC spacing to ENDCIRC	100.00	µm	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

VSS bus

The VSS bus is a (multi) metal connection to the lowest voltage digital supply.

The VSS ring is recommended to have a minimal metal width of 8 µm.

In a circuit, there could be more than one VSS bus (digital, analogue…) and each one need to be directly grounded to the substrate via contact below the metal strip. Sometimes, they are placed just around the related circuit block, as guardrings; often they are at the periphery of the chip. To be effective and avoid soft connections with adjacent substrate connections and other VSS buses tight to another supply, a certain spacing must be taken between them (several tens of µm).
However, even if each VSS bus is shortened to the common silicon substrate, they are not directly connected each other by means of any metal tracks. They are usually left separated by few µm or a pair of antiparallel diodes are connected between two adjacent VSS metals. This strongly reduces the capacitive coupling between them and allows to separate the bus for digital and analogue blocks, for instance.
No VSS ring is closed, to avoid any inductive reactance.
To respectively apply the correct metal spacing rules and avoid soft connections via LVS, the use of HVROUTE and MSUB on top of the VSS bus is suggested.

The VSS bus is not part of the scribe lane, but it should be designed inside the circuit area all around. Depending on its presence, some options can be set for the standard paramscribe, which will result in different dimensions and spacing between die sealing ring and circuit.

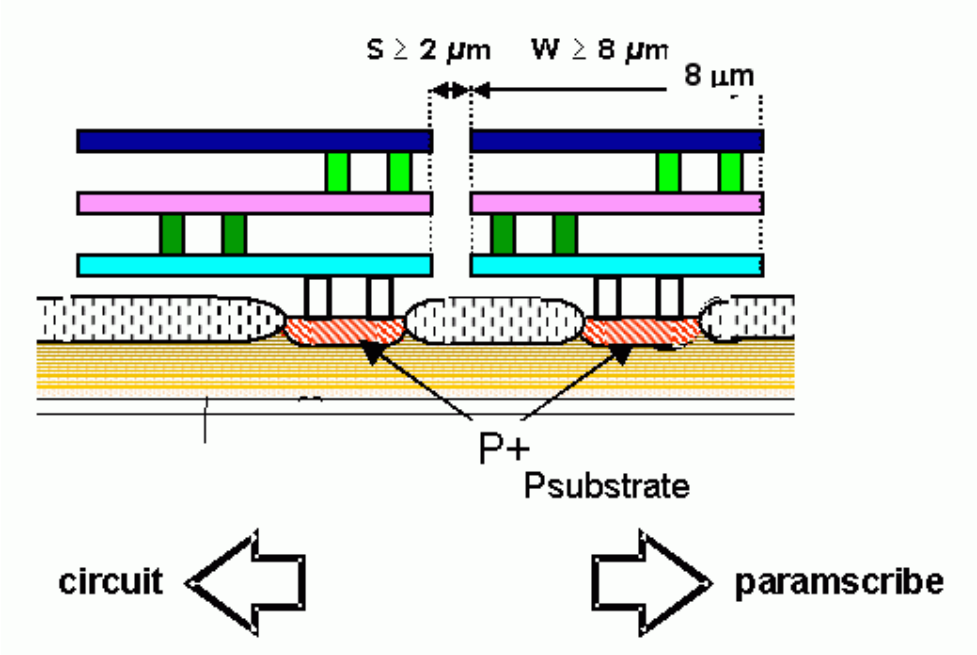
The VSS bus used in C035-I3T is usually made as a wide ring of overlapped METAL1-5 tracks. The minimal width is not tightly defined, but it should be at least 8 µm wide. However, depending on the current it might carry, a much wider bus is advised.
A double ring of VIAs is at made at the edges the ring to connect the top metal layers. Usually, these rings of VIAs are staggered from one metal to the following one. At the inner perimeter, a double ring of CONTACT is enclosed in a trench of P^+ active area.
If two or more VSS buses must surround a part of the circuit, they should run parallel one to each other. If the head of two different VSS buses meets along the ring, the edges of the related metal tracks should overlap alternatively with a minimum spacing and extension: only in this case the VSS bus is considered “closed”.

GUIDELINES:

- all metal layers must be used and they should overlap each other as much as possible; a double row of VIAs must be drawn for the whole length of each VSS bus;
- any gap between metal tracks of the VSS buses must be covered on top AND beneath by the consecutive metal layers;
- any VSS bus must be connected to the p-substrate underneath via a dense double row of contacts.
- Each VSS bus must be not more than few tens of µm closer to any other P-substrate connection or VSS bus, if linked to a different supply: a good decoupling between adjacent P-susbtrate strap or VSS buses is realized when there is a resistance in between of few kΩ.
- A local guardring surrounding the circuit block for which it supply the VSS signal, is more effective than a connection to a VSS bus placed at the outer perimeter of the chip.

The simplified cross-section of the following page should clarify this description. Notice that the crosssection of a VSS buss can slightly vary with the technology. If the substrate cannot be connected (f.i. by means of a Psinker/BLP combination), a connection to an n-type pocket could be made instead of to a p+/psinker/psubstrate combination.

orthogonal section of two parallel VSS buses:



C035U (0.35 Micron) Core CMOS Design Rules

Reliability Layout Rules

DES-0005 Rev: 11.0

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RELIABILITY LAYOUT RULES

CMOS Latch-Up and ESD

- I/O Cells

  Only standard I/O cells are allowed for latch-up and ESD protection. Any deviations from the standard I/O cells should be approved by the ON Semiconductor Lib&IP group.

- Core Cells

  - It is recommended to use as many n-well and p-well straps as possible.
  - Active area should be covered with contacts and metal straps as much as possible.

- Latch-Up Rules

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
XN.1	Maximum distance between the p+ strap and any part of a contacted n+ active in pwell implanted regions	20.00	µm	*	
XP.2	Maximum distance between the n+ strap and any point of the contacted p+ active in nwell outside blp	30.00	µm	*	
XP.4	Maximum spacing of p-active in p-wells (when the p-well contains n-active).	25.00	µm	*	
XN.5	In each nwell there should be enough n+ active areas connected to a common potential with this a maximum distance between them	50.00	µm	*	
XN.6	Each n-well should contain at least one n-well strap.			*	
XP.6	Each p-well should contain at least one p-well strap			*	rule NOT to be applied outside of y9, within the neighboorhood of y9

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

Electro-migration layout rules

The purpose of this section is to provide layout rules for interconnect line-widths and contacts and vias, such that the current densities are restricted to a level consistent with the failure rate goal of 1% failures in 10 years at the reference temperature of 125°C.

Contacts and vias

- Only minimum dimension contacts and vias are allowed.
- The minimum number of contacts or vias required for an equivalent current level is:

N = Kc x Ieq x f(T)

where

Kc = 1 / (max. current through single contact at 125°C)

f(T) = exp { 10.2 x (1 - 398/T) }

T is the absolute operating temperature (in Kelvin) determined for the worst case of each design.

Ieq is the equivalent current determined as specified in section 'Determination of Equivalent Current' below.

- The appropriate values for Kc and the maximum current per contact are given in the table below:

Parameter	Units	Contacts	Vias
size	µm	0.40	0.40
max current /contact	mA/ct	0.80	0.40
Kc	mA^{-1}	1.25	2.50

Conductors

- The minimum drawn line width for aluminium-alloy interconnections (metal layers) is given by:

  W = K x Ieq x f(T)

  where

  f(T) = exp { 10.2 x (1 - 398/T) }

  K = 1 / I_{use}(max)

  I_{use}(max) = maximum use current at reference temperature of 125°C

  T is the absolute operating temperature (in Kelvin) determined for the worst case of each design.

  Ieq is the equivalent current determined as specified in section 'Determination of Equivalent Current' below.

- The following table provides values for maximum use current for various resistivity metal layers:

Parameter	Units	Metal 1 70 mΩ/sq	Metals 55 mΩ/sq	Metal 34 mΩ/sq
I_{use}(max)	mA/µm	0.80	1.10	1.10

Determination of Equivalent Current

- Low frequencies (period > 200 nsec)

  For repetition frequencies less than 5 MHz, the RMS current equivalent should be used.

  DC current: the equivalent current is equal to the direct current.

  Pulse DC: the RMS current shall be calculated as:

$$I_{Eq} = \sqrt{\frac{\int_{T_0}^{T_0+T_c} i(t)^2 \times dt}{T_c}}$$

  The limits of the integral are T_0 to $T_0 + T_c$, or the equivalent derived from circuit simulations.

  AC current (Bi-directional): for AC current, each pulse shall be considered separately so each one shall be integrated over the full period, and the maximum value has to be taken.

- High frequencies (period = 200 nsec)

  For repetition frequencies greater than 5 MHz, the average of the absolute value of the current equivalent should be used.

  DC current: the equivalent current is equal to the direct current.

  Pulse DC: for pulse DC current, irregular current waveforms in one direction, and each direction component of AC current, the current shall be averaged over the worst case operating cycle.

  AC current (Bi-directional): for AC current, each pulse shall be considered separately so each one shall be integrated over the full period, and the maximum value has to be taken.

- Peak Current

  The table below summarizes the peak current to consider depending on the peak duration.

Peak Duration (ns)	= 5 ns	> 5ns < 100 ns	= 100 ns
Peak Current (mA/µm²)	200	100	50

ESD Protection

In previous generation processes, contact to poly space in output buffers was increased to avoid metal melting in the contacts during an ESD event. This was also reducing current crowding.

Five major design related parameters are critical for ESD performance:

Non-silicided active area

In C035U silicided active areas make current crowding more critical, so preventing silicide formation increases ESD performance. This is done with the silicide protect mask (GDS layer 18, siprot). Layout rule 18.6 is process related; it does not guarantee ESD performance. A larger value, in particular at the hot side of the transistor, is necessary to achieve the ESD performance required for each product.

Gate length of the transistor

Optimum ESD performance occurs for the minimum channel length, due to the better activation offered by the parasitic npn transistor. This is the reason why it is advised to use minimum gate length for ESD protection devices in I/O's.

Width of the transistor

Due to current density considerations, it is advised to use large transistors.

NLDD suppression

NMOS transistors have been proven to be efficient as clamping devices without NLDD structure. This can be done by using the nlddprotect layer (GDS layer 38).

N+ implant suppression

This feature is used to create P+/NLDD clamping diodes which are used in I/O protection circuitry.

Hot carrier injection constraints

- Introduction

  The hot carrier elementary device drift-time is conventionally defined by the time necessary to attain 10% degradation of typical MOS parameters:

  - gm, Vt (extrapolated, @ Vds=100 mV),
  - Idlin (@ Vds=100 mV, Vgs=3.3 V),
  - Idsat (@ Vgs=Vds=3.3 V, measured in both normal and reverse mode)

  under static worst case stress conditions.

  For NMOS transistors, the classical 10 years drift-time under nominal operating conditions (i.e. bias and gate length) for worst-case DC bias conditions is no longer guaranteed for all the parameters.

  While Vt and Idsat present drift-time higher than 10 years, this is not the case for other parameters. However, it is well known that actual product lifetime is much higher than worst-case DC elementary device drift-time, but the relation between them depends on each particular design.

  Worst-case DC bias conditions, for n-channel transistors corresponding to maximum substrate current conditions, are not realistic compared to the actual internal bias conditions inside logic circuits. For a given power supply voltage, there is a very high ratio of stress between worst DC case and actual circuit cases.

- AC Lifetime Calculation

  Transistors do not normally operate continuously in worst-case degradation conditions. The real lifetime (AC lifetime) can be calculated from the DC lifetime according to the following formula:

  $$\tau_{AC} = \tau_{DC} \times \frac{TotalPeriod}{Timecurrentnotzero}$$

  Where τ_{AC} = AC lifetime and τ_{DC} = DC lifetime.

  For digital circuits this can be approximated by:

  $$\tau_{AC} = \tau_{DC} \times \frac{TotalPeriod}{\tau_{rise} + \tau_{fall}}$$

- Hot carrier injection constraints for Analogue Applications

  In the case of analogue circuits where different parameter sensitivities and different bias schematics may be found compared to the logic circuits and for other technical reasons (e.g. matching), analogue transistors are designed with channel length larger than minimum value. This strongly reduces hot carrier induced device performance degradation.

In order to guarantee a drift time of ≥10 years for either gm or Idlin, the minimum gate-length needs to be adjusted .

The following table is based on DC measurements of I_{DLIN} drift (worst case). It may be used as a guide to choose a minimum gate length depending on the operation (V_{DS}/V_{GS}) conditions. This table is only valid for NMOS devices. PMOS channel length of 0.35µm meets the lifetime criteria.

V_{GS} (V) V_{DS} (V)	0.7 to 1	1.1	1.2	1.3	1.4 to 1.5	1.6 to 1.7	1.8 to 2.2	2.3 to 2.4	2.5 to 2.6	2.7 to 3.4	3.5	3.63
2.5 to 2.8	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35
2.9	0.45	0.45	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35
3.0	0.5	0.5	0.5	0.5	0.4	0.35	0.35	0.35	0.35	0.35	0.35	0.35
3.1	0.5	0.5	0.5	0.5	0.5	0.5	0.35	0.35	0.35	0.35	0.35	0.35
3.2	0.7	0.5	0.5	0.5	0.55	0.5	0.4	0.35	0.35	0.35	0.35	0.35
3.3	0.9	0.9	0.9	0.7	0.7	0.5	0.5	0.35	0.35	0.35	0.35	0.35
3.4	1.05	0.9	0.9	0.7	0.7	0.5	0.5	0.5	0.35	0.35	0.35	0.35
3.5	1.15	1.1	1.1	1.05	0.9	0.7	0.5	0.5	0.5	0.4	0.35	0.35
3.63	1.3	1.4	1.4	1.3	1.05	0.9	0.7	0.7	0.5	0.5	0.5	0.45

Plasma induced charging rules

- Introduction

  In today's deep-submicron technologies, more and more plasma enhanced process steps are used. It is the case for metal etch, polysilicon etch, via etch, resist ashing, oxide deposition, etc..

  Plasma steps are subject to non-uniformity across the wafer. This can lead to local non-equilibrium between ion flux and electron flux, creating either positive or negative charges to be abnormally generated. When collected by conducting wires directly connected to the gate of MOS devices, these charges can have several impacts of different damages:

  - Vt shift between metal 1 and metal 5 test
  - Oxide degradation
  - Hot carrier performance degradation

  It has been demonstrated that MOS devices connected to the routing metallization with high antenna ratio can have latent gate oxide defects which leads to degradation of the oxide lifetime.

  The following "antenna rules" should be considered in order to avoid reliability of the circuit being affected during lifetime.

- Antenna ratio definition

  The different metal layers wires can act as "antennas" for collection of charges. The antenna ratio for a polysilicon node is defined as:

$$AR = \frac{A_{m1} + A_{m2} + A_{m3} + A_{m4}}{A_{gate}}$$

  where

  Agate = gate area connected to the node

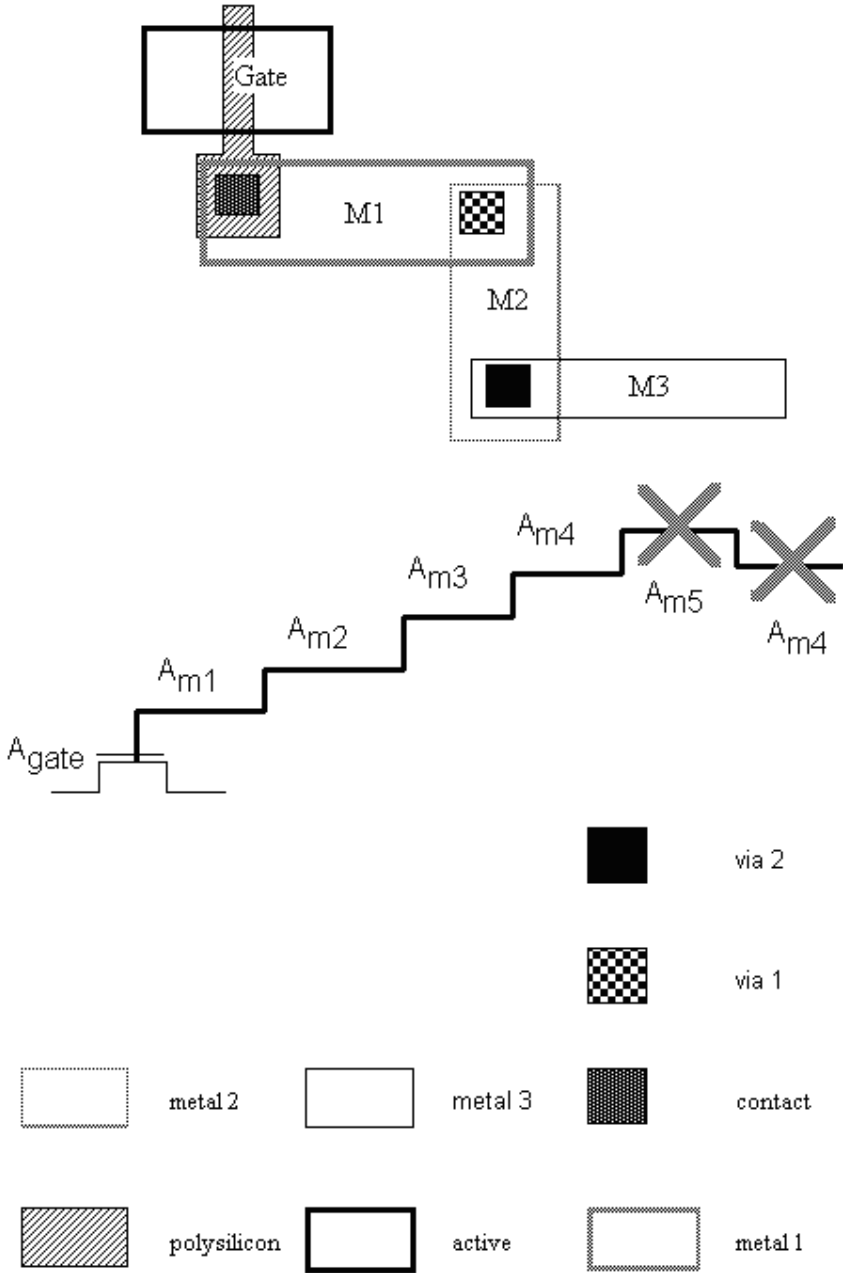
  Am1 = metal 1 area electrically connected to the node either directly or through a polysilicon line, and not connected to an active area

  Am2 = metal 2 area electrically connected to the node without using metal 3, and not connected to an active area at metal 1

  Am3 = metal 3 area electrically connected to the node without using metal 4, and not connected to an active area at metal 1 or metal 2

  Am4 = metal 4 area electrically connected to the node without using metal 5, and not connected to an active area at metal 1, metal 2 or metal 3

Following is an illustration of antenna ratio definition.



Following is a list of rules that apply to antenna ratio checks.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
ANT.1	Maximum allowed antenna ratio	300.00	µm	*	

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)

- Methods of decreasing the antenna ratio

  In all cases where it is possible in terms of silicon area availability, diode connection of metal lines to active area is recommended. The diodes act as a sink to the substrate for the charges created during following processing steps, preventing the transistor from subsequent damage.

  To be more efficient, such diode protection has to be connected to the gate and introduced at the metal 1 level if possible.

  Any error detected at the DRC must be corrected using one of the following design solutions:

  - Connect directly the node to the output of the driver with a lower metal level and reduce the metal area
  - Connect the node to a diode; n+/p-well is preferred
  - Connect the gate to the highest metal level as close to the gate as possible; this metal 5 can then be routed using the other metal layers.

  In cases where transistor matching is a concern, strong care has to be taken when designing the connection to the paired devices. In order to avoid mismatch between antenna ratio, metal lines must be as much symmetrical as possible. For the same reason, the connection lengths have to be minimized.

  Following is a list of additional considerations and good practices for multiple device types.

  - METAL CAPACITORS

    According to the understanding of the plasma damage mechanism, it is evident that the strength of the dielectric used in the metal capacitor is quite low and special precautions must be taken:

    - All the “antenna” layout rules given for MIMC (78.7-8-9) are valid, in first approximation, for all metal capacitors.
    - These rules are valid for each separate instance of a metal capacitor.
    - When two or more capacitors have a plate in common, they result in parallel for what concerns the plasma damage effect, i.e. the “antenna” rules 78.7-8a-9a must be applied to the sum of both separated and shortened plates.
    - In alternative, when two or more capacitors must be placed in parallel, rules 78.8b-9b can be fulfilled by sharing the same connection to the plate in common, only if this is a single “pillar”.
    - As general advice, it is recommended to connect each plate of a metal capacitor to a “discharging” junction. If only one is bond to a diode, there could be problems.

    Although no experimental evidences have been carried out on specific structures including metal capacitors

like “finger “ and “sandwich” capacitors, the rules above are applied to all of them.

- POLY GATE STACK

The case of a poly-oxide stack is quite different from the case of any metal capacitors, due to the larger dielectric strength of the gate oxide.

- The connection to a POLY gate (poly crossing active) is made through a TOP metal layer.

Indeed, one should avoid that a poly gate is connected with the smaller “antenna” area to the highest level of metal available before being routed too far, i.e. with a very large metal area connected. This extreme precaution prevents the possibility to form a wide plate which can then discharge through the gate oxide, regardless the ratio of the metal plate areas between the antenna connected to the gate and that one connected to the bulk underneath.

By reaching the top metal closed to the gate, the poly plate itself results disconnected from the remaining part of the routed metallisation till this is connected to its direct antenna by means of a bridge of the top metal, which is usually very small.

- In alternative, a better solution is to use a protective device, like a clamping diode at the base of the connectivity chain (“antenna”) connected to the gate. The poly gate has to be connected at the lowest metal level as possible to a diode with a terminal onto the local diffusion (see “antenna diode” option in ENM Pcell), which can discharge the excess of carriers before they damage the gate oxide itself.

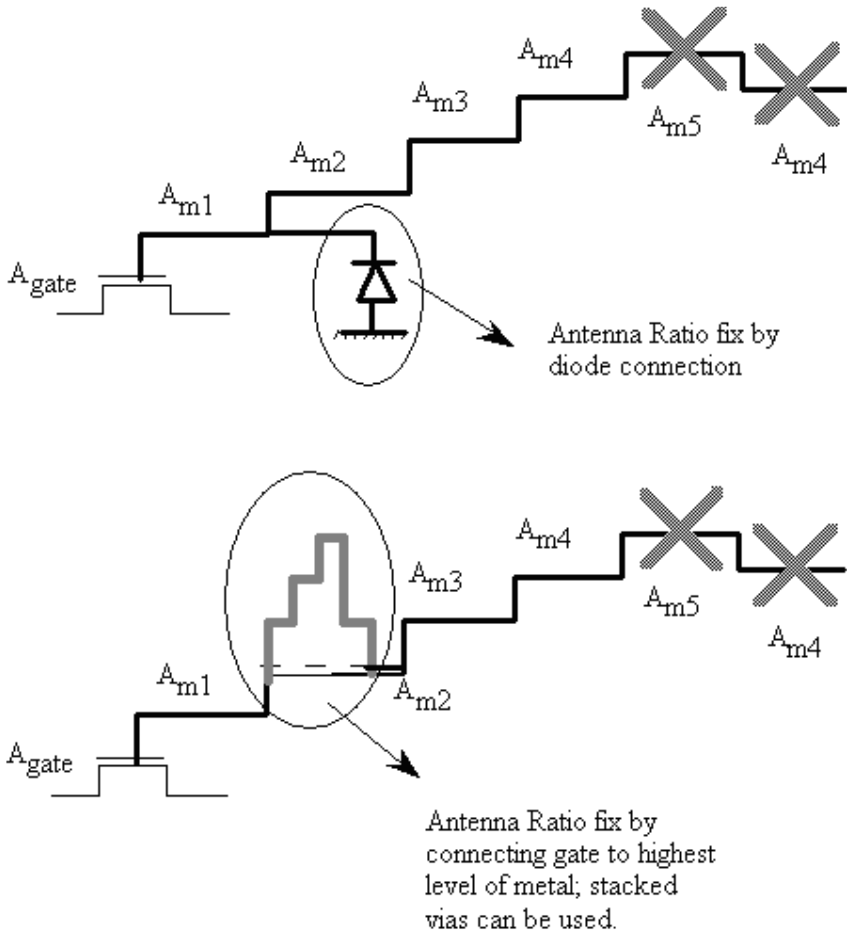
- One antenna diode” serves as discharging element for all poly gate directly connected to its cathode (N+ strap in the case of the diode in the ENM bulk) .

- DRC DECK FOR ANTENNA RULES

The DRC deck containing the antenna rules must be run for all C035U-based designs (digital / analogue / mixed / high voltage). Although the running time is very fast, there is also the way to disable the check once the layout has been verified.

When building IP blocks, this DRC check should be performed and diodes on each input of the block should be inserted, otherwise new errors can appear during the top level routing.

Following is an illustration of possible antenna ratio fixes.



C035U (0.35 Micron) Core CMOS Design Rules

Electrical Rules

DES-0005 Rev: 11.0

Confidential

ELECTRICAL DESIGN RULES

This section provides the designer with electrical design rules and process attributes that influence the electrical characteristics of a circuit.

Introduction

Only characterized devices are available for circuit design. These devices are routinely monitored, the data of which is used to provide the electrical rules hereafter. Other devices than those specified are not allowed. If a designer wishes to use a device that is possible in the technology but is not characterized, then the ON SEMICONDUCTOR Technology R&D Department must be consulted before the actual design of the product. Refer to section Mask Identification - Characterized Devices for Circuit Design for the list of available characterized devices.

All dimensions given in this section are as drawn dimensions on the IGS system.

All values of the parameters given hereafter are measured at room temperature (300°K) unless specified otherwise.

All values of the parameters are valid for all device dimensions except where these dimensions are specified.

A brief description of the measurement conditions is given for each parameter. Refer to ON SEMICONDUCTOR BELGIUM BVBA specification GP10800 for the details of the measurement procedures.

IMPORTANT NOTE: all electrical parameters given for active transistors are for assistance in preliminary calculations for circuit design and are not a substitute for circuit simulation.

- **Temperature Coefficients**

All temperatures are in Kelvin. All formulas given below are valid over the temperature range from 218K to 423K (-55C to 150C).

MOS Threshold Voltage (Vt(0))

$V_t(0)(T) = V_t(0)(300) + TC_{Vt(0)} \times (T - 300)$

MOS Linear Transconductance (ßlin)

$Blin(T)=Blin(1+Tc1\_b \times (T-300)+Tc2\_b \times (T-300)^2)$

MOS Saturation Current (Idsat)

$I_{dsat}(T) = I_{dsat}(300) \times [1 + TCIY \times (T - 300)]$

Sheet Resistance (ρ_s)

$\rho_s(T) = \rho_{s(}300) \times [1 + TC_L \times (T-300) + TC_Q \times (T-300)^2]$

- **Diode Leakage**

  Diode leakage is given as the sum of two components: area leakage and periphery leakage:

  $$I_{leak} = I_a \text{ x diode area} + I_p \text{ x diode periphery}$$

  I_a and I_p are characterised at 30C, 85C and 150C.

- **Junction Capacitance**

  Junction capacitance as a function of reverse bias is given by:

  $$C(V) = C(0) / [\ 1 + V/P_b\ ]^{Mj}$$

  where: C(V) = junction capacitance under reverse bias

  C(0) = zero bias junction capacitance

  V = applied reverse bias voltage

  Pb = built in potential

  Mj = capacitance gradient factor

NMOS Transistors

IMPORTANT: THE ELECTRICAL PARAMETERS HEREAFTER ARE EXTRACTED FROM THE MOS MODELS RELEASED IN WW 2004-20; THE EXTRACTION IS DONE AS IF THE PARAMETER WOULD BE MEASURED AT ETEST.

THE TYPICAL MODEL, WHICH IS THE BASIS OF THE CORNERS, HAS LIMITED ACCURACY FOR THE PREDICTION OF THE MAXIMUM GM (TRANSCONDUCTANCE). THE MODEL SYSTEMATICALLY UNDERESTIMATES THE MAXIMUM TRANSCONDUCTANCE.

The temperature coefficients of Vt in this table was extracted from the integration measurement verified between -40 and 200 C as released in WW2008-26, based on I3T50 material.

Device W/L	Parameter	Units	MIN	TYP	MAX	Condition
Nch 10/10	$V_t(0)$	mV	542	599	656	V_{ds} = 100 mV, V_{bs} = 0 V
	ßlin	µA/V^2	138.6	166.1	197.2	V_{ds} = 100 mV, V_{bs} = 0 V
	I_{dsat}	µA	384.7	428.7	495.2	V_{ds} = V_{gs} = 3.3 V, V_{bs} = 0 V
	Gamma	√ V	0.49	0.55	0.61	V_{ds} = 100 mV, Sweep V_{bs}
	BVDSS	V	7			V_{gs} = 0 V, V_{bs} = 0V, V_{ds} @ 1 µA
	TC [$V_t(0)$]	mV/C		-0.99		V_{ds} = 100 mV, V_{bs} = 0 V
	TC [$_{ßlin}$]	N/A		-1.85		V_{ds} = 100 mV, V_{bs} = 0 V
	TC [I_{dsat}]	%/C		-0.36		V_{ds} = V_{gs} = 3.3 V, V_{bs} = 0 V
Nch 10/0.35	Vt(0)	V	466	593	709	V_{ds} = 100 mV, V_{bs} = 0 V
	ßlin	µA/V^2	3724	5066	5961	V_{ds} = 100 mV, V_{bs} = 0 V
	I_{dsat}/W	µA/µm	431	538	622	V_{ds} = V_{gs} = 3.3 V, V_{bs} = 0 V
	I_{leak}/W	pA/µm		1	50	V_{ds} = V_{dmax} = 3.63 V, V_{gs} = 0 V
	BVDSS	V	7			V_{gs} = 0 V, V_{bs} = 0V, V_{ds} @ 1 µA
	TC [$V_t(0)$]	mV/C		-0.98		V_{ds} = 100 mV, V_{bs} = 0 V
	TC [I_{dsat}]	%/C		-0.16		V_{ds} = V_{gs} = 3.3 V, V_{bs} = 0 V
Nch 0.5/10	Vt(0)	V	515	582	652	V_{ds} = 100 mV, V_{bs} = 0 V
	ßlin	µA/V^2	4.33	6.22	8.31	V_{ds} = 100 mV, V_{bs} = 0 V
	I_{dsat}	µA	11.44	15.68	20.79	V_{ds} = V_{gs} = 3.3 V, V_{bs} = 0 V
	TC [$V_t(0)$]	mV/C		-0.99		V_{ds} = 100 mV, V_{bs} = 0 V
Nch 0.5/0.35	Vt(0)	V	427	615	799	V_{ds} = 100 mV, V_{bs} = 0 V
	ßlin	µA/V^2	132	210	276	V_{ds} = 100 mV, V_{bs} = 0 V
	I_{dsat}	µA	167	258	346	V_{ds} = V_{gs} = 3.3 V, V_{bs} = 0 V
	TC [$V_t(0)$]	mV/C		-0.92		V_{ds} = 100 mV, V_{bs} = 0 V

The temperature coefficients of Vt and Beta in this table was extracted from the MOS models verified between -40 and 200 C as released in WW2008-26, based on I3T50 material.

Device W/L	Parameter	Units	MIN	TYP	MAX	Condition
Nch 7/7	Vt(0)	mV		618		V_{ds} = 100 mV, V_{bs} = 0 V
	TC [V_t(0)]	mV/C		-1.03		V_{ds} = 100 mV, V_{bs} = 0 V
	ßlin	µA/V^2		168		V_{ds} = 100 mV, V_{bs} = 0 V
	Tc1_b	10^{-3}/C		-5.7		V_{ds} = 100 mV, V_{bs} = 0 V
	Tc2_b	$10^{-6}/C^2$		15.0		V_{ds} = 100 mV, V_{bs} = 0 V
Nch 7/0.35	Vt(0)	mV		601		V_{ds} = 100 mV, V_{bs} = 0 V
	TC [V_t(0)]	mV/C		-0.95		V_{ds} = 100 mV, V_{bs} = 0 V
	ßlin	µA/V^2		3285		V_{ds} = 100 mV, V_{bs} = 0 V
	Tc1_b	10^{-3}/C		-4.0		V_{ds} = 100 mV, V_{bs} = 0 V
	Tc2_b	$10^{-6}/C^2$		5.9		V_{ds} = 100 mV, V_{bs} = 0 V
Nch 0.5/7	Vt(0)	mV		615		V_{ds} = 100 mV, V_{bs} = 0 V
	TC [V_t(0)]	mV/C		-0.99		V_{ds} = 100 mV, V_{bs} = 0 V
	ßlin	µA/V^2		8.91		V_{ds} = 100 mV, V_{bs} = 0 V
	Tc1_b	10^{-3}/C		-4.7		V_{ds} = 100 mV, V_{bs} = 0 V
	Tc2_b	10^{-6}/C2		10.6		V_{ds} = 100 mV, V_{bs} = 0 V
Nch 0.5/0.35	Vt(0)	mV		614		V_{ds} = 100 mV, V_{bs} = 0 V
	TC [V_t(0)]	mV/C		-0.89		V_{ds} = 100 mV, V_{bs} = 0 V
	ßlin	µA/V^2		208		V_{ds} = 100 mV, V_{bs} = 0 V
	Tc1_b	10^{-3}/C		-4.1		V_{ds} = 100 mV, V_{bs} = 0 V
	Tc2_b	10^{-6}/C^2		7.1		V_{ds} = 100 mV, V_{bs} = 0 V

PMOS Transistors

IMPORTANT: THE ELECTRICAL PARAMETERS HEREAFTER ARE EXTRACTED FROM THE MOS MODELS RELEASED IN WEEK 04-20; THE EXTRACTION IS DONE AS IF THE PARAMETER WOULD BE MEASURED AT ETEST.

The temperature coefficients of Vt in this table was extracted from the integration measurement verified between -40 and 200 C as released in WW2008-26, based on I3T50 material.

Device W/L	Parameter	Units	MIN	TYP	MAX	Condition
Pch 10/10	$V_t(0)$	V	-0.681	-0.598	-0.519	V_{ds} = -100 mV, V_{bs} = 0 V
	ßlin	$\mu A/V^2$	32.9	38.9	41	V_{ds} = -100 mV, V_{bs} = 0 V
	I_{dsat}	µA	-99	-89.2	-76.8	V_{ds} = V_{gs} = -3.3 V, V_{bs} = 0 V
	Gamma	√ V	-0.73	-0.69	-0.65	V_{ds} = -100 mV, Sweep V_{bs}
	BVDSS	V			-7	V_{gs} = 0 V, V_{bs} = 0V, V_{ds} @ -1 µA
	TC [$V_t(0)$]	mV/C		1		V_{ds} = -100 mV, V_{bs} = 0 V
	TC [I_{dsat}]	%/C		-0.2		V_{ds} = V_{gs} = -3.3 V, V_{bs} = 0 V
Pch 10/0.35	Vt(0)	V	-0.726	-0.594	-0.493	V_{ds} = -100 mV, V_{bs} = 0 V
	ßlin	$\mu A/V^2$	803	1095	1378	V_{ds} = -100 mV, V_{bs} = 0 V
	I_{dsat}/W	µA/µm	-319	-246	-173	V_{ds} = V_{gs} = -3.3 V, V_{bs} = 0 V
	I_{leak}/W	pA/µm	-50	-1		V_{ds} = V_{dmax} = -3.63 V, V_{gs} = 0 V
	BVDSS	V			-7	V_{gs} = 0 V, V_{bs} = 0V, V_{ds} @ -1 µA
	TC [$V_t(0)$]	mV/C		1		V_{ds} = -100 mV, V_{bs} = 0 V
	TC [I_{dsat}]	%/C		-0.11		V_{ds} = V_{gs} = -3.3 V, V_{bs} = 0 V
Pch 0.5/10	Vt(0)	V	-0.719	-0.627	-0.544	V_{ds} = -100 mV, V_{bs} = 0 V
	ßlin	$\mu A/V^2$	0.9	1.41	1.73	V_{ds} = -100 mV, V_{bs} = 0 V
	I_{dsat}	µA	-4.19	-3.25	-2.12	V_{ds} = V_{gs} = -3.3 V, V_{bs} = 0 V
	TC [$V_t(0)$]	mV/C		0.971		V_{ds} = -100 mV, V_{bs} = 0 V
Pch 0.5/0.35	Vt(0)	V	-0.753	-0.601	-0.451	V_{ds} = -100 mV, V_{bs} = 0 V
	ßlin	$\mu A/V^2$	26.4	43.6	60.3	V_{ds} = -100 mV, V_{bs} = 0 V
	I_{dsat}	µA	-156	-105	-60	V_{ds} = V_{gs} = -3.3 V, V_{bs} = 0 V
	TC [$V_t(0)$]	mV/C		1		V_{ds} = -100 mV, V_{bs} = 0 V

THE TYPICAL MODEL, WHICH IS THE BASIS OF THE CORNERS, HAS LIMITED ACCURACY FOR THE PREDICTION OF THE MAXIMUM GM (TRANSCONDUCTANCE). THE MODEL SYSTEMATICALLY UNDERESTIMATES THE MAXIMUM TRANSCONDUCTANCE.

The temperature coefficients of Vt and Beta in this table was extracted from the MOS models verified between -40 and 200 C as released in WW2008-26, based on I3T50 material.

Device W/L	Parameter	Units	MIN	TYP	MAX	Condition
Pch 7/7	Vt(0)	mV		-597		V_{ds} = 100 mV, V_{bs} = 0 V
	TC [V_t(0)]	mV/C		1		V_{ds} = 100 mV, V_{bs} = 0 V
	ßlin	µA/V^2		43.41		V_{ds} = 100 mV, V_{bs} = 0 V
	Tc1_b	10^{-3}/C		-3.6		V_{ds} = 100 mV, V_{bs} = 0 V
	Tc2_b	$10^{-6}/C^2$		8.6		V_{ds} = 100 mV, V_{bs} = 0 V
Pch 7/0.35	Vt(0)	mV		-648		V_{ds} = 100 mV, V_{bs} = 0 V
	TC [V_t(0)]	mV/C		0.97		V_{ds} = 100 mV, V_{bs} = 0 V
	ßlin	µA/V^2		2.063		V_{ds} = 100 mV, V_{bs} = 0 V
	Tc1_b	10^{-3}/C		-3.8		V_{ds} = 100 mV, V_{bs} = 0 V
	Tc2_b	$10^{-6}/C^2$		8.8		V_{ds} = 100 mV, V_{bs} = 0 V
Pch 0.5/7	Vt(0)	mV		-621		V_{ds} = 100 mV, V_{bs} = 0 V
	TC [V_t(0)]	mV/C		1.07		V_{ds} = 100 mV, V_{bs} = 0 V
	ßlin	µA/V^2		782.80		V_{ds} = 100 mV, V_{bs} = 0 V
	Tc1_b	10^{-3}/C		-3.4		V_{ds} = 100 mV, V_{bs} = 0 V
	Tc2_b	10^{-6}/C2		6.2		V_{ds} = 100 mV, V_{bs} = 0 V
Pch 0.5/0.35	Vt(0)	mV		-627		V_{ds} = 100 mV, V_{bs} = 0 V
	TC [V_t(0)]	mV/C		1.09		V_{ds} = 100 mV, V_{bs} = 0 V
	ßlin	µA/V^2		36.34		V_{ds} = 100 mV, V_{bs} = 0 V
	Tc1_b	10^{-3}/C		-3.7		V_{ds} = 100 mV, V_{bs} = 0 V
	Tc2_b	10^{-6}/C^2		8.2		V_{ds} = 100 mV, V_{bs} = 0 V

lnndm15 /lfndm14

Main electrical features

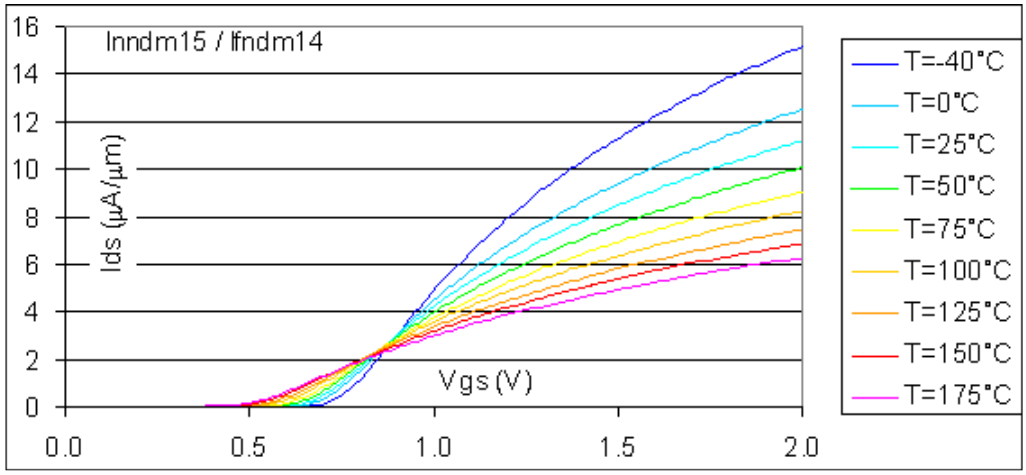
Parameters	Min	Nom	Max	Units
Vt0 (W=4*40µm)	0.5		0.66	V
TC[Vt0] (W=4*40µm)		-1.1		mV/K
Betalin	100		170	µA/µm V^2
Ron	26	32	38	mΩ/mm^2
TC[Ron] (W=4*40µm)		0.16		mΩ/mm^2 /K
Idsat/W (Vd=5V, Vg=3.3V)	215		275	µA/µm
Idsat/W (Vd=13V, Vg=1.5V)	38		72	µA/µm
Subths (mV/dec)	78		91	µA/µm
Vbd	14			V
Vabsmax			12	V

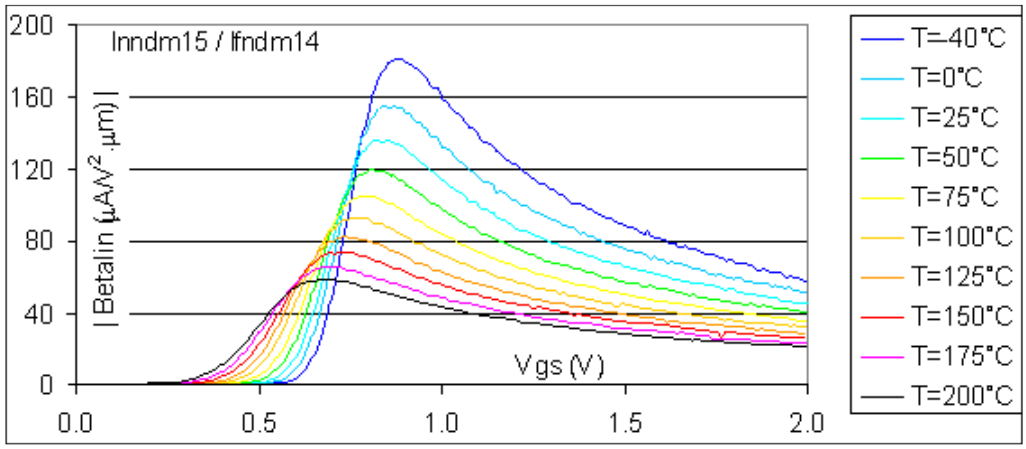
Electrical characteristics

The following data is measured on I3T50U material, relevant for the C35U-based processes covered in this manual. The data is valid for the devices sharing the same core devices, independent from the isolation or guard rings.

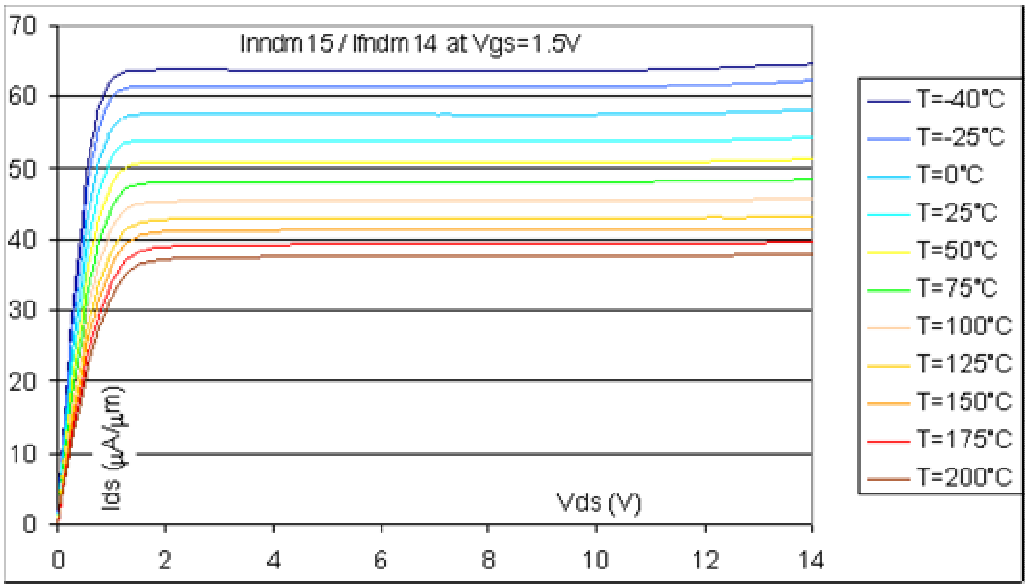
The detailed SOA is process dependent and is shown in the electrical manual of the derived technology. The Vabs max is applicable generally.

Ids-Vgs at Vds=0.1V (transfert characteristic).

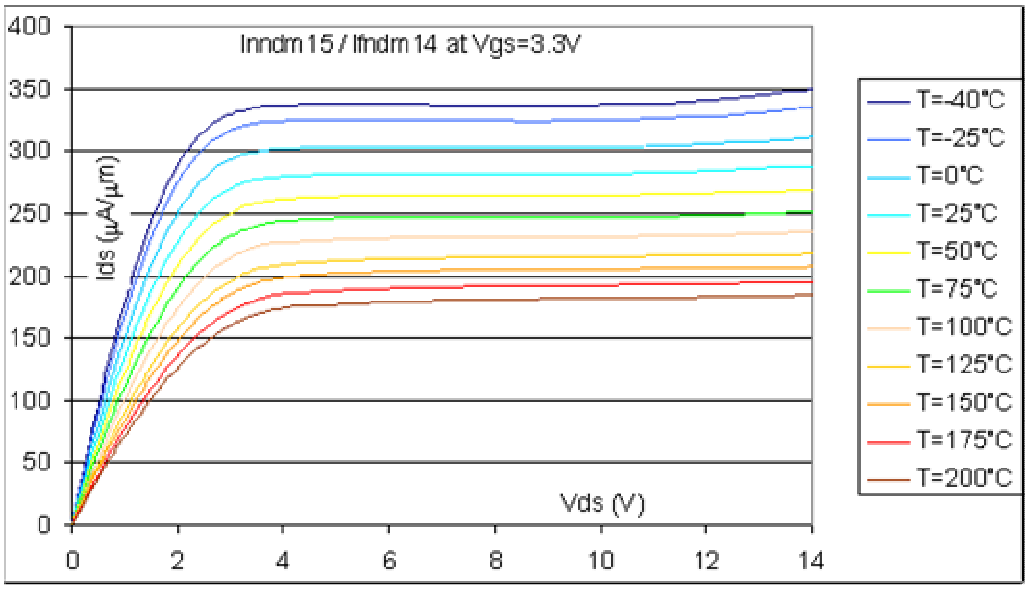




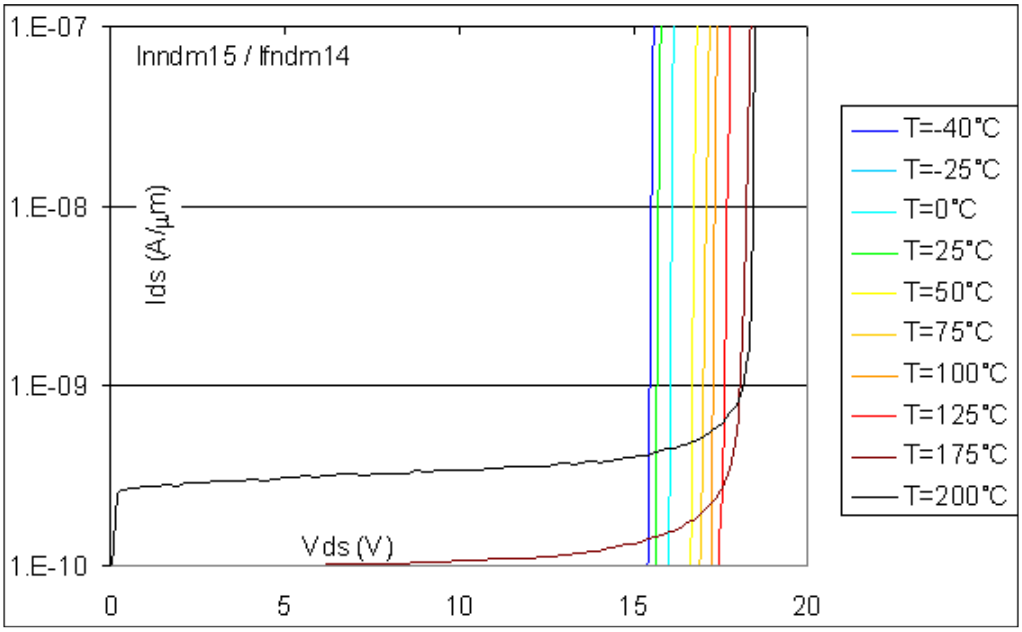
Ids-Vds for Vgs = 1.5V versus temperature

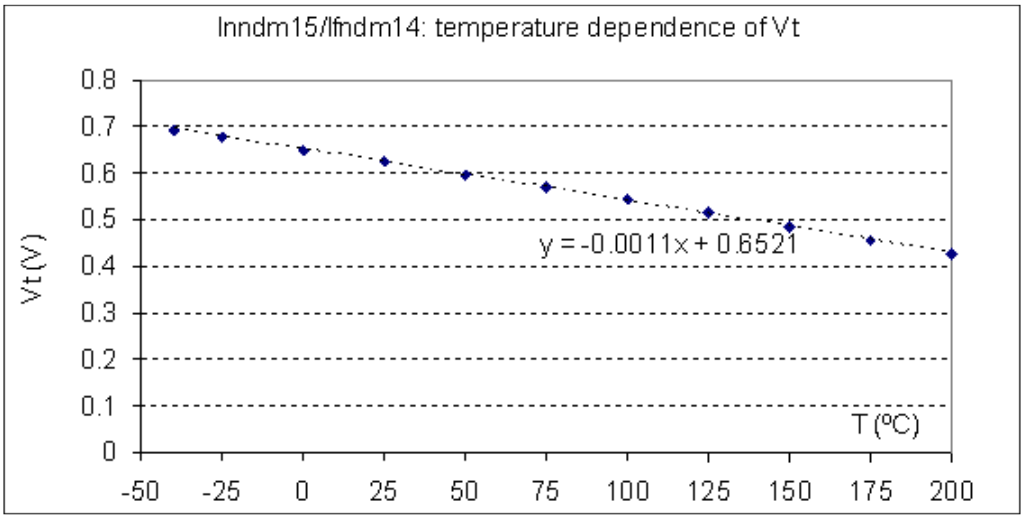


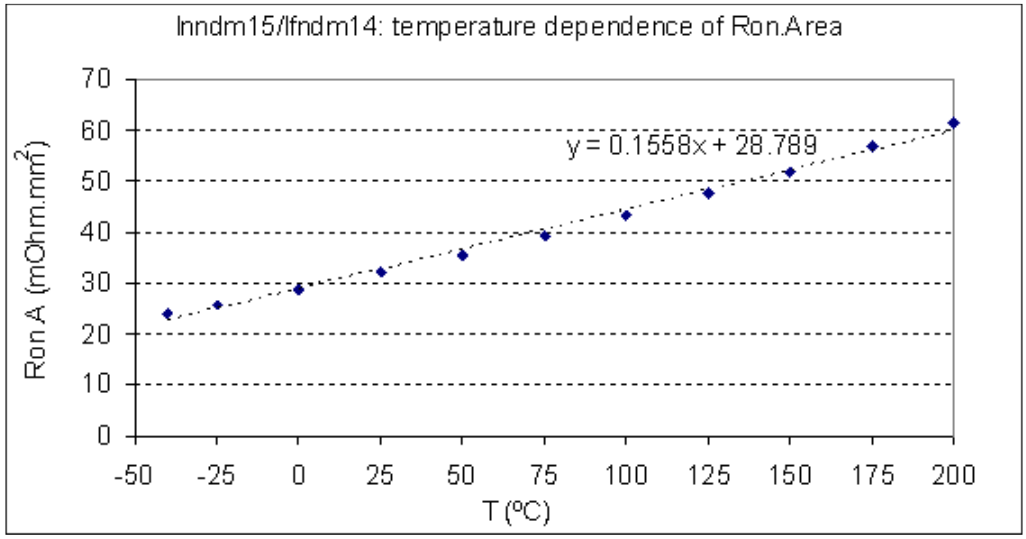
Ids-Vds for Vgs = 3.3V versus temperature



Vbd characteristic for lnndm15/lfndm14 versus temperature







Matching of LFNDM14 matching:

The current mismatch of LFNDM14 transistors is defined as the standard deviation (σ) of (Id1-Id2)*200/ (Id1+Id2) and can be model by the following equation:

$$\sigma\left(\frac{\Delta I_d}{I_d}\right)^2 = \frac{A_\beta^2}{WL} + C_\beta^2 + \left(\frac{g_m}{I_d}\right)^2 * \left(\frac{A_{V_T}^2}{WL} + C_{V_T}^2\right)$$

The V_T matching is characterized by parameters $A_{V_T}^2$ and $C_{V_T}^2$ and the β-matching by parameters A_β^2 and C_β^2.

The standard deviation of Vth and Beta can be express in term of mismatch parameters ($A_{VT,}$ $C_{VT,}$ A_β, $C_{\beta)}$ using the following equations:

$$\sigma(\Delta VT) = \frac{A_{VT}}{\sqrt{WL}} + C_{VT}$$ A_{VT} (mV*um) and C_{VT} (mV)

$$\sigma\left(\frac{\Delta\beta}{\beta}\right) = \frac{A_\beta}{\sqrt{WL}} + C_\beta$$ A_β (%*um) and C_β (%)

LFNDM14

LFNDM14			
ΔVt		Δ β /β	
A	C	A	C
9.59	0.22	1.53	0.04

OTP Specific

- **LNNDM15**

Device	Parameter	Units	MIN	TYP	MAX	Condition
LNNDM15	WIDTH	µm	8	8	8	
	$V_t(0)$	V	0.498	0.580	0.661	V_{ds} = 100 mV, V_{bs} = 0 V
	ßlin/W	µA/µm/V^2	103	133	173	V_{ds} = 100 mV, V_{bs} = 0 V
	I_{dsat}/W	µA/µm	236.4	282.6	331.0	V_{ds} = 10V, V_{gs} = 3.3 V, V_{bs} = 0 V
	RON*W	KΩ*µm	5.48	6.59	7.95	V_{ds} = 100 mV, V_{gs} = 3.3 V, V_{bs} = 0 V
	BVDSS	V	12	-	-	V_{gs} = 0 V, V_{bs} = 0V, V_{ds} @ 10 nA

- **UZZD (Un-Zapped Zener Diode)**

Device	Parameter	Units	MIN	TYP	MAX	Condition
UZZD	VZ (10)	V	1.2	1.7	2.2	V @ I = 10 µA
	VZ (50)	V	2.0	2.5	3.0	V @ I = 50 µA
	ILEAK	µA	0.1	1.0	1.9	I @ V = 1 V

- **ZZD (Zapped Zener Diode)**

For specifics of zapping of OTP in C035U, please contact ON SEMICONDUCTOR Lib&IP group.

Polydiode

Refer to the technology specific electrical documentation to get the exact performance of this diode.

Interconnect Metal Capacitors (MMCHB / MMCHP)

a **MMCHB on Nwell capacitor of 1mm^2 (std metals)**, which is made of 714 fingers of 1 mm length per level, gives:
The presence of fingers in poly contributes 60pF/m/finger (Cf).

C (poly + M1/M3)	C (M1/M3)	C (M1/M4)	C (M1/M5)	C_{WELL} (parasitic)	Unit
236	195	259	320	~47	pF
0.236	0.195	0.259	0.32	~0.047	fF/um^2

a **MMCHP on Nwell capacitor of 1mm^2 (std metals)** gives a total Ca of:
The presence of fingers in poly contributes 40uF/m^2 (Ca).

C (poly + M1/M3)	C (M1/M3)	C (M1/M4)	C (M1/M5)	C_{WELL} (parasitic)	Unit
140	102	149	190	~90	pF
0.14	0.102	0.149	0.19	~0.09	fF/um^2

Matching of transistors

Current mismatch observed between identically designed MOS transistors is linked to the statistical variations of the MOS characteristic parameters, which are mainly the threshold voltage V_t and the current factor ß.

Generally, matching in a parameter P (=I_D, V_t or ß) is defined as the standard deviation (=1σ) of the distribution of the differences of P between the matched devices. The mean of the parameter differences is supposed to be zero and independent of distance, implying that there is neither systematic offset nor gradient. For this reason, the values of the matching parameters given in the next section are valid only for designs respecting the following conditions:

- Identical design
- Identical orientation
- Identical direction of the current from source to drain
- Distance between matched transistors < 100 µm
- Identical surroundings (equal distance to field, to capacitors, to metal lines etc.)
- No crossover by unrelated metal (metals 1 to 5). In the case of metal coverage, a degradation-in matching is observed which is most severe for metal 1 coverage and least severe for metal 5 coverage. As mentioned in section Mask Identification - Pattern Density Requirements and Dummy Metal Procedure of this document, extra (dummy) metal features will be generated on all metal layers. This can lead to degradation in the matching performance. The matching

models given below are only valid in the case that this dummy metal generation is blocked in the areas where transistor matching is required. In order to block generation of dummy metal, the metdis layer (63) must be used. Rules for the use of this in conjunction with matched transistors are given in section Mask Identification - Pattern Density Requirements and Dummy Metal Procedure of this document.
It is strongly advised to keep the use of metdis to a minimum. Large areas of unequal metal density inevitably lead to a loss of planarization uniformity, which can influence parasitic capacitances and/or yield.

Due to plasma induced charge degradation it is greatly advised to

- Protect the gate of the matched pairs by a diode,
- Take care of the symmetry of the metal routing to the transistors.

Matching Coefficients

The model used for the gate voltage dependence of the current matching is

$$\sigma^2\left(\frac{\Delta I_D}{I_D}\right) = \sigma^2\left(\frac{\Delta\beta}{\beta}\right) + \frac{4\sigma^2(\Delta V_T)}{(V_{gs}-V_T)^2}$$

valid in the strong inversion region (V_{gs}-V_T > 0.25V).

This equation applies for devices with L ≥ 2 µm and WxL < 600 µm^2). For shorter channels, the matching behaviour of MOS transistors is deteriorated by extra mismatch causes such as CD control, source series resistance and short/narrow channel effects. It is therefore strongly advised not to use minimum channel lengths for matched MOS transistors. For transistors with area greater than 600 µm^2, no matching data are available; however, the possibility exists of some degradation due to longer distance non-uniformity.

Under the above conditions, the matching parameters $\sigma^2(\Delta VT)$ and $\sigma^2(\Delta ß/ß)$ have the following dependence on transistor width (W) and length (L):

$$\sigma^2 = \frac{A^2}{WL} + B^2$$

The coefficients A^2 for $\sigma^2(\Delta VT)$ and $\sigma^2(\Delta ß/ß)$ are given in the tables below for NMOS and PMOS for $|V_{DS}|$ = 3.3V and bulk bias V_{BS}=0V. Due to the dependence of the matching on the specific measurement conditions used and the limited amount of data used to derive these figures, it is advised to use a 4-5 σ approach for the final calculation.

	NMOS	PMOS
A_{vt} [mV*um]	12	9.45
B_{vt} [mV]	0	0
$A_ß$ [%*um]	2.56	1.5
$B_ß$ [%]	0	0

Field Transistors

The field transistors are designed as finger structures with minimum active area spacing.

Device	Parameter	Units	MIN	MAX	Condition
NField Poly Gate	Vgsat	V	7		Vds = 6V, Ramp Vgs, Vgsat = Vgs @ 1 µA
NField Poly Gate	Ileak	pA/µm		1.0	Vds = Vgs = Vdmax = 3.63V, Vbs = 0 V
PField Poly Gate	Vgsat	V		-7	Vds = -6V, Ramp Vgs, Vgsat = Vgs @ -1 µA
PField Poly Gate	Ileak	pA/µm	-1.0		Vds = Vgs = Vdmax = -3.63V, Vbs = 0 V
NField Metal Gate	Vgsat	V	7		Vds = 6V, Ramp Vgs, Vgsat = Vgs @ -1 µA
NField Metal Gate	Ileak	pA/µm		1.0	Vds = Vgs = Vdmax = 3.63V, Vbs = 0 V
PField Metal Gate	Vgsat	V		-7	Vds = -6V, Ramp Vgs, Vgsat = Vgs @ -1 µA
PField Metal Gate	Ileak	pA/µm	-1.0		Vds = Vgs = Vdmax = -3.63V, Vbs = 0 V

Resistors

- **Resistance Values (excluding interconnect metal)**

  IMPORTANT: THE USE OF SILICIDED FEATURES FOR RESISTORS SHOULD BE AVOIDED DUE TO LARGE DIFFERENCES THAT CAN EXIST BETWEEN DIFFERENT MANUFACTURING UNITS (FAB 2 AND FAB 10).

Device	Parameter	Units	MIN	TYP	MAX	Condition
n+ active silicided	ρ_s	Ω/sq	1.5		4.0	I = 1 mA/µm
p+ active silicided	ρ_s	Ω/sq	1.5		4.0	I = 1 mA/µm
n+ silicided poly on field oxide	ρ_s	Ω/sq	1.0		4.0	I = 1 mA/µm, W > 1.0 µm
n+ silicided poly on field oxide	ρ_s	Ω/sq	1.0		10.0	I = 1 mA/µm, W < 1.0 µm
p+ silicided poly on field oxide	ρ_s	Ω/sq	1.5		5.0	I = 1 mA/µm
n+ active non-silicided	ρ_s	Ω/sq	40	50	60	I = 100 µA/µm
p+ active non-silicided	ρ_s	Ω/sq	50	70	90	I = 100 µA/µm

- **Metal Resistance Values**

  C035U-based technologies offer flexible metallization schemes. Minimum number of metal layers is 3, maximum number of metal layers is 5. The top layer metal can be either thin or thick. The tables below give an overview of the qualified metallization modules available for product design.

  - **Typical Values**

Level	Option 1	Option 2	Option 3	Option 4	Option 5	Option 6
Metal 1	72 mΩ/sq	72 mΩ/sq	72 mΩ/sq	72 mΩ/sq	72 mΩ/sq	72 mΩ/sq
Metal 2	55 mΩ/sq	55 mΩ/sq	55 mΩ/sq	55 mΩ/sq	55 mΩ/sq	55 mΩ/sq
Metal 3	55 mΩ/sq	55 mΩ/sq	55 mΩ/sq	34 mΩ/sq	55 mΩ/sq	55 mΩ/sq
Metal 4	-	55 mΩ/sq	55 mΩ/sq	-	34 mΩ/sq	55 mΩ/sq
Metal 5	-	-	55 mΩ/sq	-	-	34 mΩ/sq

  - **Minimum Values**

Level	Option 1	Option 2	Option 3	Option 4	Option 5	Option 6
Metal 1	57 mΩ/sq	57 mΩ/sq	57 mΩ/sq	57 mΩ/sq	57 mΩ/sq	57 mΩ/sq
Metal 2	44 mΩ/sq	44 mΩ/sq	44 mΩ/sq	44 mΩ/sq	44 mΩ/sq	44 mΩ/sq
Metal 3	44 mΩ/sq	44 mΩ/sq	44 mΩ/sq	27 mΩ/sq	44 mΩ/sq	44 mΩ/sq
Metal 4	-	44 mΩ/sq	44 mΩ/sq	-	27 mΩ/sq	44 mΩ/sq
Metal 5	-	-	44 mΩ/sq	-	-	27 mΩ/sq

- **Maximum Values**

Level	Option 1	Option 2	Option 3	Option 4	Option 5	Option 6
Metal 1	87 mΩ/sq	87 mΩ/sq	87 mΩ/sq	87 mΩ/sq	87 mΩ/sq	87 mΩ/sq
Metal 2	66 mΩ/sq	66 mΩ/sq	66 mΩ/sq	66 mΩ/sq	66 mΩ/sq	66 mΩ/sq
Metal 3	66 mΩ/sq	66 mΩ/sq	66 mΩ/sq	39 mΩ/sq	66 mΩ/sq	66 mΩ/sq
Metal 4	-	66 mΩ/sq	66 mΩ/sq	-	39 mΩ/sq	44 mΩ/sq
Metal 5	-	-	66 mΩ/sq	-	-	39 mΩ/sq

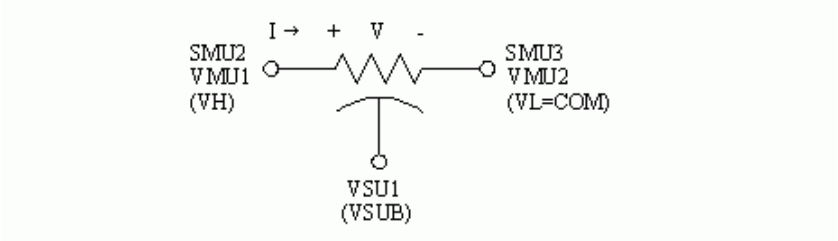
Matched Resistors (Analog option)

The following is the SPECTRE physical resistor (phys_res) model:

$$R = R_{sh}\left(\frac{L - 2.Etchl}{W - 2.Etch}\right).\left[1 + T_{C1}(T - T_{nom}) + T_{C2}(T - T_{nom})^2\right]$$

where

R_{sh} = sheet resistance
L = drawn length
W = drawn width
etchl = length reduction
etch = width reduction due to etching
T = TRISE + TEMP
T_{nom} = nominal temperature
T_{C1} = linear temperature coefficient
T_{C2} = quadratic temperature coefficient



Experimental setup schematic showing HP4155B source module and voltage module connections for a 4-point measurement where $0<|V_H|\leq 4V$ and $0<|V_{SUB}|\leq 3.6V$

- **Extraction of Thermal coefficients**

Thermal coefficients were extracted using measurements performed at 25, 80, 120 and 160°C using a four-point probe method. Linear and quadratic temperature coefficients were extracted using least squares regression.

- **Extraction of sheet resistance, device-size parameters, and voltage coefficients**

For all the modelled resistors, the sheet resistance, the device-size parameters, and the voltage coefficients were extracted utilizing non-linear regression to minimize the sum-of-squares (SSE) error for the SPECTRE model. This non-linear regression used the previously obtained temperature coefficients as constants.

- **Extraction of Pelgrom coefficients for Poly Resistors**

The percent of resistor mismatch is defined as

$$\%Mismatch = 200\frac{R_1 - R_2}{R_1 + R_2}$$

where R_1 and R_2 are the two resistors in a matching pair.

The mismatching of resistors is modelled with Pelgrom's law which linearly links the variation of a parameter of a device to the inverse of its area (see eq. 1) :

$$\sigma^2\left(\frac{\Delta R}{R}\right) = \frac{A^2}{area} + C^2$$

	A [%*um]	C [%]
HIPOR model	2.45	0
PPOR model	2.5495	0
NPOR model	5.71	0. 000225

All matching data was taken using an automated-probe technique. To minimize the effects of contact resistance, matching data was obtained by first varying the applied current to obtain either a 0.1V drop or a 3.3V drop across the resistor. The chosen current was then forced through the resistor with the resistor voltage being measured. Data used in the extraction of the Pelgrom coefficients was filtered using an extreme outlier filter followed by a standard 1.5 inner-quartile-range filter. This resulted in near-normal distributions, which validates use of the Pelgrom model. Pelgrom coefficients were then extracted at both 0.1V and 3.3V.

- **Extraction of Drennon coefficients for Active Resistors**

For diffused resistors matching is described by the formula of P.G. Drennan:

(2)
$$\sigma^2\left(\frac{\Delta R}{R}\right) = p_d + \frac{p_L}{L^2} + \frac{p_W}{W^2} + \frac{p_{WL}}{WL}$$

	Pd	Pl	Pw	Pwl
NPRPW model	0.0043	11.3030	0.0	7.6944
PPRNW model	0.0	42.277	0.0	7.992

- **Resistor Parameters**

<u>IMPORTANT</u>: TYPICAL POLY RESISTOR PARAMETERS WERE CALCULATED SUCH THAT THE RESULTING MODEL FORMS THE BEST FIT FOR BOTH FAB 2 AND FAB 10. IN ORDER TO GUARANTEE LESS THAN 5 % ERROR BETWEEN THE MODEL AND SILICON FROM BOTH MANUFACTURING UNITS, THE FOLLOWING LIMITATIONS APPLY FOR THE GEOMETRIES OF THE POLYSILICON RESISTORS.

HIPOR: Minimum width = 1.2 µm, Minimum length = 3.6 µm

NPOR: Minimum width = 1.2 µm, Minimum length = 3.6 µm

PPOR: Minimum width = 1.2 µm, Minimum length = 9.0 µm

MODEL PARAMETERS

Model names	Description	Model parameters	MIN	TYP	MAX
HIPOR HIPORXWBB HIPORXWNL	HIgh Ohmic POly Resistor (Silicide Blocked)	R_{sh} (Ω/sq)	775	975	1175
		etch (m)	8.11E-08	8.11E-08	8.11E-08
		etchl (m)	-4.54E-08	-4.54E-08	-4.54E-08
		T_{c1} (K^{-1})	-1.42E-03	-1.42E-03	-1.42E-03
		T_{c2} (K^{-2})	2.87E-06	2.87E-06	2.87E-06
LOPOR LOPORXWBB LOPORXWNL	Low Ohmic POly Resistor (Silicided)	R_{sh} (Ω/sq)	1.5	2.4	4
		etch (m)	-2.50E-08	-2.50E-08	-2.50E-08
		etchl (m)	-3.60E-08	-3.60E-08	-3.60E-08
		T_{c1} (K^{-1})	3.47E-03	3.47E-03	3.47E-03
		T_{c2} (K^{-2})	-2.57E-06	-2.57E-06	-2.57E-06
NPOR NPORXWBB NPORXWNL	Nplus POly Resistor (Silicide Blocked)	R_{sh} (Ω/sq)	232	292	352
		etch (m)	7.88E-09	7.88E-09	7.88E-09
		etchl (m)	-2.33E-07	-2.33E-07	-2.33E-07
		T_{c1} (K^{-1})	-1.97E-03	-1.97E-03	-1.97E-03
		T_{c2} (K^{-2})	4.03E-06	4.03E-06	4.03E-06
PPOR PPORXWBB PPORXWNL	Pplus POly Resistor (Silicide Blocked)	R_{sh} (Ω/sq)	180	240	300
		etch (m)	4.94E-09	4.94E-09	4.94E-09
		etchl (m)	-6.75E-07	-6.75E-07	-6.75E-07
		T_{c1} (K^{-1})	-2.30E-04	-2.30E-04	-2.30E-04
		T_{c2} (K^{-2})	9.92E-07	9.92E-07	9.92E-07
NPRPW NPRPWBB NPRPWNL	NPlus Resistor in Pwell (Silicide Blocked)	R_{sh} (Ω/sq)	37.5	47.5	57.5
		etch (m)	4.67E-08	4.67E-08	4.67E-08
		etchl (m)	-6.08E-07	-6.08E-07	-6.08E-07
		T_{c1} (K^{-1})	1.39E-03	1.39E-03	1.39E-03
		T_{c2} (K^{-2})	4.96E-07	4.96E-07	4.96E-07
PPRNW PPRNWBB PPRNWNL	PPlus Resistor in Nwell (Silicide Blocked)	R_{sh} (Ω/sq)	54	64	74
		etch (m)	1.06E-07	1.06E-07	1.06E-07
		etchl (m)	-7.40E-07	-7.40E-07	-7.40E-07
		T_{c1} (K^{-1})	1.69E-03	1.69E-03	1.69E-03
		T_{c2} (K^{-2})	3.72E-07	3.72E-07	3.72E-07
PWARNW PWARNWBB PWARNWNL	PWell Active Resistor surrounded by Nwell (Silicide Blocked)	R_{sh} (Ω/sq)	1555	1755	1955
		etch (m)	5.00E-07	5.00E-07	5.00E-07
		etchl (m)	-2.78E-07	-2.78E-07	-2.78E-07
		T_{c1} (K^{-1})	3.65E-03	3.65E-03	3.65E-03
		T_{c2} (K^{-2})	6.55E-06	6.55E-06	6.55E-06

ETEST PARAMETERS

With the model parameters given above, the following ETEST limits are extracted, given the dimensions W & L of the specific resistors in the ETEST SLM's.

			Model Extraction			ETEST limits		
RESISTOR	**W [µm]**	**L [µm]**	**MIN**	**TYP**	**MAX**	**LSL**	**Target**	**USL**
HIPOR	8	37	794.0	997.6	1201.2	800	1000	1200
	16	72	784.9	986.2	1187.5	800	1000	1200
	8	72	793.1	996.4	1199.8	800	1000	1200
NPOR (**)	0.35	35	N/A; ETEST "R_{sh}" PARAMETER			210	270	330
	0.70	70	IS EXTRACTED (*)					
PPOR	0.35	35	N/A; ETEST "R_{sh}" PARAMETER			140	240	340
	0.70	70	IS EXTRACTED (*)					
NPRPW (**)	0.80	40	N/A; ETEST "R_{sh}" PARAMETER			40	50	60
	1.60	80	IS EXTRACTED (*)					
PPRNW (**)	0.80	40	N/A; ETEST "R_{sh}" PARAMETER			50	70	90
	1.60	80	IS EXTRACTED (*)					

* The ETEST parameter "R_{sh}" , along with the CD, is extracted from 2 resistance measurements.

** ETEST limits not fully aligned with model limits, because of model accuracy limitations for narrow resistors; also, the extraction algorithm at ETEST does not take into account the parameter "etchl".

MIM Capacitor (Analogue Option)

Maximum voltage: 3.63 volts (limited by reliability constraints).

- **Definitions**

  The voltage dependence of the MIM capacitors is fitted to the following equation:

  $$C(V) = C_0\left[1 + C_1 x(V) + C_2 x(V)^2\right]$$

  where V is the voltage across the MIM capacitor.

  The temperature dependence of the MIM capacitor is fitted to the following equation. In this equation, C refers to the unit area capacitance. Measurements have been performed at temperatures in the range +25°C / +125°C.

  $$C(T) = C_0(T_{REF}) + Bx(T - T_{REF})$$

  Capacitor matching parameters is described by the formula:

  $$\sigma^2\left(\frac{\Delta C}{C}\right) = \frac{A^2}{WxL}$$

  where A = matching coefficient

- **Parameters**

Parameter	Units	MIN	TYP	MAX
$C_a(0)$	fF/µm^2	1.3	1.5	1.7
$C_p(0)$	fF/µm	0.28 10^{-6}	0.34 10^{-6}	0.40 10^{-6}
V_{BD}	Volts	25	35	
C_1	ppm/V	-100	-32	+100
C_2	ppm/V^2	-30	18.5	+30
T_{C1}	ppm/K	20	45.5	60
T_{C2}	ppm/K^2	0	0	0
A	% µm	-	1.48	-

Contact Resistance

Device	Parameter	Units	MIN	TYP	MAX	Condition
n+ active	ρ_c	Ω/ct	1.5	4.5	12.0	I = 20 µA/contact
p+ active	ρ_c	Ω/ct	2.5	5.5	12.0	I = 20 µA/contact
n+ poly	ρ_c	Ω/ct	3.0	5.5	12.0	I = 20 µA/contact
p+ poly	ρ_c	Ω/ct	3.0	6.5	12.0	I = 20 µA/contact
via 1	ρ_c	Ω/ct	0.4	1.5	4.0	I = 0.2 mA/via
via 2	ρ_c	Ω/ct	0.4	1.5	4.0	I = 0.2 mA/via
via 3	ρ_c	Ω/ct	0.4	1.5	4.0	I = 0.2 mA/via
via 4	ρ_c	Ω/ct	0.4	1.5	4.0	I = 0.2 mA/via

Gate Oxide and Junction Capacitance

- **Gate Oxide Capacitance**

Device	Parameter	Units	MIN	TYP	MAX	Condition
N Channel Gate Oxide	Tox	nm	6.5	7.1	7.7	Optical measurement
			7	7.4	-	Calculated from Cplate
	Cplate	F/m	-	4.66E-3	-	V=-4 Volts
	V_{BD}	V	-	-	-	I = 1mA/cm²
P Channel Gate Oxide	Tox	nm	6.5	7.1	7.7	Optical measurement
			7	7.4	-	Calculated from Cplate
	Cplate	F/m	-	4.66E-3	-	V=+4 Volts
	V_{BD}	V	-	-	-	I = 1mA/cm²

- **Junction Capacitance**

Device	Parameter	Units	MIN	TYP	MAX	Condition
n+/p-well	Cj	F/m²	-	8.92E-4	-	V=0 Volts
	Mj	F/m	-	0.450	-	Fitted
	Pb	V	-	0.950	-	Fitted
	Cjsw	F/m	-	3.11E-10	-	V=0 Volts
	Mjsw		-	0.200	-	Fitted
	Pbsw		-	0.800	-	Fitted
	Cjc		-	-	-	V=0 Volts
p+/n-well	Cj	F/m²	-	1.24E-3	-	V=0 Volts
	Mj	F/m	-	0.4600	-	Fitted
	Pb	V	-	0.9000	-	Fitted
	Cjsw	F/m	-	2.24E-10	-	V=0 Volts
	Mjsw		-	0.163	-	Fitted
	Pbsw		-	0.800	-	Fitted
	Cjc		-	-	-	V=0 Volts

Interconnect Capacitance

Interconnect capacitances are calculated from the dielectric and conductor thicknesses.

- **Dielectric Thicknesses**

  For a planarised technology the dielectric thickness varies depending upon the layout and conductor density. For example: the metal 2 to metal 1 oxide thickness is less for an isolated metal 1 line than for an array of closely spaced metal 1 lines.

  The dielectric thicknesses given in the table below correspond to the most probable conditions: thickness over an array of lines at minimum spacing.

  To avoid unrealistically pessimistic worst cases, for capacitance calculations the process spread on these dielectric thicknesses may be set to ± 10%.

Description	Units	TYP
Poly - well	µm	0.30
Metal 1 - active	µm	1.22
Metal 1 - poly	µm	0.80
Metal (i+1) - metal (i) [i = 1,2,3,4]	µm	0.90
Metal 2.5 - metal 2	µm	0.042
Passivation	µm	1.10

The above values can be used together with the conductor thickness listed below to calculate all distances between the various layers.

- **Conductor Thicknesses**

The conductor thicknesses, as deposited, are as follows:

Layer	Constituent Layers	Units	MIN	FAB2 TYP	FAB10 TYP	MAX
Poly		µm	0.270	0.300	0.300	0.330
Metal 1	All Layers	µm	0.567	0.630	0.630	0.693
	Ti/TiN barrier	nm	-	20/80	15/25	-
	Al-alloy	µm	-	0.50	0.50	-
	TiN ARC	nm	-	30	100	-
Metal 55 mΩ/sq	All Layers	µm	0.648	0.72	0.72	0.792
	Ti/TiN barrier	nm	-	20/80	15/25	-
	Al-alloy	µm	-	0.59	0.59	-
	TiN ARC	nm	-	30	100	-
Top Metal 55 mΩ/sq	All Layers	µm	0.648	0.72	0.72	0.792
	Ti/TiN barrier	nm	-	20/80	15/25	-
	Al-alloy	µm	-	0.59	0.66	-
	TiN ARC	nm	-	30	30	-
Metal 34 mΩ/sq	All Layers	µm	0.918	1.02	N/A	1.122
	Ti/TiN barrier	nm	-	20/80	N/A	-
	Al-alloy	µm	-	0.89	N/A	-
	TiN ARC	nm	-	30	N/A	-
Metal 2.5	All Layers	µm	0.234	0.260	0.260	0.286
	Ti/TiN barrier	nm	-	30	30	-
	Al-alloy	µm	-	0.20	0.20	-
	TiN ARC	nm	-	30	30	-

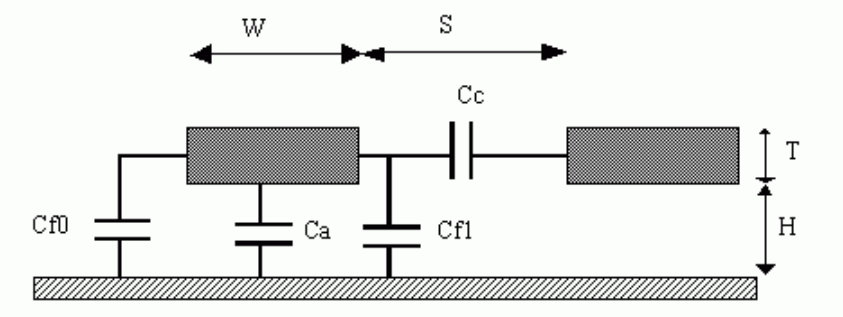
- **Dielectric permittivity**

The physical nature of the different dielectrics used in the process can differ greatly from one process step to another. It is especially true for the isolation between transistors (locos, oxide thermally grown), and isolation between metal lines (a sandwich of gap filling oxide and PECVD oxide).

The relative dielectric permittivities to be used are summarized in the table below.

Layer	Units	MIN	TYP	MAX
LOCOS	N/A	3.8	3.9	4.0
Metal(i) to Metal(i) [i = 1,2,3,4,5]	N/A	3.8	4.0	4.2
Metal(i) to metal(i+1) [i = 1,2,3,4]	N/A	3.8	4.1	4.4
Metal 2 to Metal2.5	N/A		7.12	

- **Interconnect capacitance calculation**
  - **Schematic and description**



W = conductor width
S = conductor spacing
T = conductor thickness
H = dielectric thickness
C = total capacitance per unit length
Ca = area capacitance
Cf0 = fringing capacitance to underlying conductor for single line
Cf1 = fringing capacitance to underlying conductor in case of adjacent line
Cc = coupling capacitance in case of adjacent line

  - **Capacitance calculation**

a) case of single line:
C = W * Ca + 2 * Cf0

b) case of two lines
C = W * Ca + Cf0 + Cf1 + Cc

c) case of three lines
C = W * Ca + 2 * Cf1 + 2 * Cc

In the following tables, Cc is given for the minimum spacing, corresponding to the worst case.

  - **Strategy**

Case	H	T	S	W
Nominal	Nominal	Nominal	Nominal	Nominal
Slow (maximum capacitance)	Minimum	Maximum	Minimum	Maximum
Fast (minimum capacitance)	Maximum	Minimum	Maximum	Minimum

- **Capacitance look-up tables**

Capacitance values given in this section are approximate values; refer to STAR-XT extraction decks.

5-layer metal process with thick (34 mΩ/sq) top metal

NOMINAL INTERCONNECT CAPACITANCE

Layer	H [µm]	T [µm]	S [µm]	W [µm]	Ca [fF/µm^2]	Cf0 [fF/µm]	Cf1 [fF/µm]	Cc [fF/µm]
Poly1 - well	0.300	0.300	0.500	0.350	0.1151	0.0514	0.0250	0.0402
M1 - well	1.400	0.630	0.500	0.500	0.0247	0.0414	0.0061	0.0800
M1 - active	1.250	0.630	0.500	0.500	0.0276	0.0426	0.0070	0.0792
M1 - poly	0.800	0.630	0.500	0.500	0.0432	0.0475	0.0116	0.0751
M2 - well	2.930	0.720	0.500	0.600	0.0118	0.0359	0.0024	0.0921
M2 - active	2.780	0.720	0.500	0.600	0.0124	0.0364	0.0026	0.0921
M2 - poly	2.330	0.720	0.500	0.600	0.0148	0.0379	0.0033	0.0917
M2 - M1	0.900	0.720	0.500	0.600	0.0384	0.0477	0.0106	0.0840
M3 - well	4.550	0.720	0.500	0.600	0.0076	0.0324	0.0013	0.0902
M3 - active	4.400	0.720	0.500	0.600	0.0078	0.0327	0.0014	0.0905
M3 - poly	3.950	0.720	0.500	0.600	0.0087	0.0335	0.0016	0.0913
M3 - M1	2.520	0.720	0.500	0.600	0.0137	0.0372	0.0030	0.0919
M3 - M2	0.900	0.720	0.500	0.600	0.0384	0.0477	0.0106	0.0840
M4 - well	6.170	0.720	0.500	0.600	0.0056	0.0303	0.0009	0.0858
M4 - active	6.020	0.720	0.500	0.600	0.0057	0.0304	0.0009	0.0863
M4 - poly	5.570	0.720	0.500	0.600	0.0062	0.0310	0.0010	0.0877
M4 - M1	4.140	0.720	0.500	0.600	0.0083	0.0332	0.0015	0.0910
M4 - M2	2.520	0.720	0.500	0.600	0.0137	0.0372	0.0030	0.0919
M4 - M3	0.900	0.720	0.500	0.600	0.0384	0.0477	0.0106	0.0840
M5 - well	7.790	1.020	0.700	0.700	0.0044	0.0310	0.0010	0.0882
M5 - active	7.640	1.020	0.700	0.700	0.0045	0.0312	0.0010	0.0886
M5 - poly	7.190	1.020	0.700	0.700	0.0048	0.0316	0.0011	0.0894
M5 - M1	5.760	1.020	0.700	0.700	0.0060	0.0332	0.0015	0.0916
M5 - M2	4.140	1.020	0.700	0.700	0.0083	0.0359	0.0024	0.0926
M5 - M3	2.520	1.020	0.700	0.700	0.0137	0.0403	0.0046	0.0908
M5 - M4	0.900	1.020	0.700	0.700	0.0384	0.0517	0.0151	0.0797

MINIMUM INTERCONNECT CAPACITANCE

Layer	H	T	S	W	Ca	Cf0	Cf1	Cc
	in µm	in µm	in µm	in µm	in fF/µm2	in fF/µm	in fF/µm	in fF/µm
Poly1 - well	0.330	0.270	0.535	0.315	0.1046	0.0487	0.0233	0.0371
M1 - well	1.480	0.567	0.550	0.450	0.0233	0.0399	0.0061	0.0690
M1 - active	1.330	0.567	0.550	0.450	0.0260	0.0409	0.0069	0.0685
M1 - poly	0.880	0.567	0.550	0.450	0.0392	0.0452	0.0111	0.0656
M2 - well	3.037	0.648	0.560	0.540	0.0114	0.0348	0.0026	0.0764
M2 - active	2.887	0.648	0.560	0.540	0.0120	0.0352	0.0027	0.0765
M2 - poly	2.437	0.648	0.560	0.540	0.0142	0.0366	0.0034	0.0766
M2 - M1	0.990	0.648	0.560	0.540	0.0349	0.0454	0.0102	0.0719
M3 - well	4.675	0.648	0.560	0.540	0.0074	0.0315	0.0014	0.0736
M3 - active	4.525	0.648	0.560	0.540	0.0076	0.0317	0.0015	0.0739
M3 - poly	4.075	0.648	0.560	0.540	0.0085	0.0325	0.0017	0.0749
M3 - M1	2.628	0.648	0.560	0.540	0.0131	0.0360	0.0031	0.0766
M3 - M2	0.990	0.648	0.560	0.540	0.0349	0.0454	0.0102	0.0719
M4 - well	6.313	0.648	0.560	0.540	0.0055	0.0294	0.0009	0.0688
M4 - active	6.163	0.648	0.560	0.540	0.0056	0.0295	0.0010	0.0693
M4 - poly	5.713	0.648	0.560	0.540	0.0060	0.0301	0.0011	0.0707
M4 - M1	4.266	0.648	0.560	0.540	0.0081	0.0321	0.0016	0.0745
M4 - M2	2.628	0.648	0.560	0.540	0.0131	0.0360	0.0031	0.0766
M4 - M3	0.990	0.648	0.560	0.540	0.0349	0.0454	0.0102	0.0719
M5 - well	7.951	0.918	0.770	0.630	0.0043	0.0301	0.0011	0.0723
M5 - active	7.801	0.918	0.770	0.630	0.0044	0.0303	0.0011	0.0727
M5 - poly	7.351	0.918	0.770	0.630	0.0047	0.0307	0.0012	0.0736
M5 - M1	5.904	0.918	0.770	0.630	0.0058	0.0323	0.0016	0.0761
M5 - M2	4.266	0.918	0.770	0.630	0.0081	0.0348	0.0025	0.0779
M5 - M3	2.628	0.918	0.770	0.630	0.0131	0.0389	0.0047	0.0775
M5 - M4	0.990	0.918	0.770	0.630	0.0349	0.0492	0.0144	0.0696

MAXIMUM INTERCONNECT CAPACITANCE

Layer	H	T	S	W	Ca	Cf0	Cf1	Cc
	in µm	in µm	in µm	in µm	in fF/µm2	in fF/µm	in fF/µm	in fF/µm
Poly1 - well	0.270	0.330	0.465	0.385	0.1279	0.0542	0.0269	0.0436
M1 - well	1.320	0.693	0.450	0.550	0.0262	0.0430	0.0060	0.0936
M1 - active	1.170	0.693	0.450	0.550	0.0295	0.0443	0.0070	0.0924
M1 - poly	0.720	0.693	0.450	0.550	0.0480	0.0499	0.0122	0.0865
M2 - well	2.823	0.792	0.440	0.660	0.0122	0.0371	0.0023	0.1128
M2 - active	2.673	0.792	0.440	0.660	0.0129	0.0375	0.0024	0.1125
M2 - poly	2.223	0.792	0.440	0.660	0.0155	0.0392	0.0031	0.1114
M2 - M1	0.810	0.792	0.440	0.660	0.0426	0.0502	0.0109	0.0993
M3 - well	4.425	0.792	0.440	0.660	0.0078	0.0334	0.0012	0.1123
M3 - active	4.275	0.792	0.440	0.660	0.0081	0.0336	0.0013	0.1125
M3 - poly	3.825	0.792	0.440	0.660	0.0090	0.0345	0.0015	0.1130
M3 - M1	2.412	0.792	0.440	0.660	0.0143	0.0385	0.0028	0.1120
M3 - M2	0.810	0.792	0.440	0.660	0.0426	0.0502	0.0109	0.0993
M4 - well	6.027	0.792	0.440	0.660	0.0057	0.0311	0.0008	0.1083
M4 - active	5.877	0.792	0.440	0.660	0.0059	0.0313	0.0008	0.1088
M4 - poly	5.427	0.792	0.440	0.660	0.0064	0.0318	0.0009	0.1101
M4 - M1	4.014	0.792	0.440	0.660	0.0086	0.0341	0.0014	0.1128
M4 - M2	2.412	0.792	0.440	0.660	0.0143	0.0385	0.0028	0.1120
M4 - M3	0.810	0.792	0.440	0.660	0.0426	0.0502	0.0109	0.0993
M5 - well	7.629	1.122	0.630	0.770	0.0045	0.0319	0.0009	0.1084
M5 - active	7.479	1.122	0.630	0.770	0.0046	0.0320	0.0010	0.1087
M5 - poly	7.029	1.122	0.630	0.770	0.0049	0.0325	0.0011	0.1094
M5 - M1	5.616	1.122	0.630	0.770	0.0061	0.0342	0.0014	0.1111
M5 - M2	4.014	1.122	0.630	0.770	0.0086	0.0369	0.0023	0.1110
M5 - M3	2.412	1.122	0.630	0.770	0.0143	0.0416	0.0045	0.1074
M5 - M4	0.810	1.122	0.630	0.770	0.0426	0.0544	0.0159	0.0918

4-layer metal process with thick (34 mΩ/sq) top metal

NOMINAL INTERCONNECT CAPACITANCE

Layer	H	T	S	W	Ca	Cf0	Cf1	Cc
	[µm]	[µm]	[µm]	[µm]	[fF/µm^2]	[fF/µm]	[fF/µm]	[fF/µm]
Poly1 - well	0.300	0.300	0.500	0.350	0.1151	0.0514	0.0250	0.0402
M1 - well	1.400	0.630	0.500	0.500	0.0247	0.0414	0.0061	0.0800
M1 - active	1.250	0.630	0.500	0.500	0.0276	0.0426	0.0070	0.0792
M1 - poly	0.800	0.630	0.500	0.500	0.0432	0.0475	0.0116	0.0751
M2 - well	2.930	0.720	0.500	0.600	0.0118	0.0359	0.0024	0.0921
M2 - active	2.780	0.720	0.500	0.600	0.0124	0.0364	0.0026	0.0921
M2 - poly	2.330	0.720	0.500	0.600	0.0148	0.0379	0.0033	0.0917
M2 - M1	0.900	0.720	0.500	0.600	0.0384	0.0477	0.0106	0.0840
M3 - well	4.550	0.720	0.500	0.600	0.0076	0.0324	0.0013	0.0902
M3 - active	4.400	0.720	0.500	0.600	0.0078	0.0327	0.0014	0.0905
M3 - poly	3.950	0.720	0.500	0.600	0.0087	0.0335	0.0016	0.0913
M3 - M1	2.520	0.720	0.500	0.600	0.0137	0.0372	0.0030	0.0919
M3 - M2	0.900	0.720	0.500	0.600	0.0384	0.0477	0.0106	0.0840
M4 - well	6.170	1.020	0.700	0.700	0.0056	0.0327	0.0014	0.0911
M4 - active	6.020	1.020	0.700	0.700	0.0057	0.0329	0.0014	0.0913
M4 - poly	5.570	1.020	0.700	0.700	0.0062	0.0335	0.0016	0.0918
M4 - M1	4.140	1.020	0.700	0.700	0.0083	0.0359	0.0024	0.0926
M4 - M2	2.520	1.020	0.700	0.700	0.0137	0.0403	0.0046	0.0908
M4 - M3	0.900	1.020	0.700	0.700	0.0384	0.0517	0.0151	0.0797

MINIMUM INTERCONNECT CAPACITANCE

Layer	H	T	S	W	Ca	Cf0	Cf1	Cc
	in µm	in µm	in µm	in µm	in fF/µm2	in fF/µm	in fF/µm	in fF/µm
Poly1 - well	0.330	0.270	0.535	0.315	0.1046	0.0487	0.0233	0.0371
M1 - well	1.480	0.567	0.550	0.450	0.0233	0.0399	0.0061	0.0690
M1 - active	1.330	0.567	0.550	0.450	0.0260	0.0409	0.0069	0.0685
M1 - poly	0.880	0.567	0.550	0.450	0.0392	0.0452	0.0111	0.0656
M2 - well	3.037	0.648	0.560	0.540	0.0114	0.0348	0.0026	0.0764
M2 - active	2.887	0.648	0.560	0.540	0.0120	0.0352	0.0027	0.0765
M2 - poly	2.437	0.648	0.560	0.540	0.0142	0.0366	0.0034	0.0766
M2 - M1	0.990	0.648	0.560	0.540	0.0349	0.0454	0.0102	0.0719
M3 - well	4.675	0.648	0.560	0.540	0.0074	0.0315	0.0014	0.0736
M3 - active	4.525	0.648	0.560	0.540	0.0076	0.0317	0.0015	0.0739
M3 - poly	4.075	0.648	0.560	0.540	0.0085	0.0325	0.0017	0.0749
M3 - M1	2.628	0.648	0.560	0.540	0.0131	0.0360	0.0031	0.0766
M3 - M2	0.990	0.648	0.560	0.540	0.0349	0.0454	0.0102	0.0719
M4 - well	6.313	0.918	0.770	0.630	0.0055	0.0318	0.0015	0.0755
M4 - active	6.163	0.918	0.770	0.630	0.0056	0.0319	0.0015	0.0757
M4 - poly	5.713	0.918	0.770	0.630	0.0060	0.0325	0.0017	0.0764
M4 - M1	4.266	0.918	0.770	0.630	0.0081	0.0348	0.0025	0.0779
M4 - M2	2.628	0.918	0.770	0.630	0.0131	0.0389	0.0047	0.0775
M4 - M3	0.990	0.918	0.770	0.630	0.0349	0.0492	0.0144	0.0696

MAXIMUM INTERCONNECT CAPACITANCE

Layer	H	T	S	W	Ca	Cf0	Cf1	Cc
	in µm	in µm	in µm	in µm	in fF/µm2	in fF/µm	in fF/µm	in fF/µm
Poly1 - well	0.270	0.330	0.465	0.385	0.1279	0.0542	0.0269	0.0436
M1 - well	1.320	0.693	0.450	0.550	0.0262	0.0430	0.0060	0.0936
M1 - active	1.170	0.693	0.450	0.550	0.0295	0.0443	0.0070	0.0924
M1 - poly	0.720	0.693	0.450	0.550	0.0480	0.0499	0.0122	0.0865
M2 - well	2.823	0.792	0.440	0.660	0.0122	0.0371	0.0023	0.1128
M2 - active	2.673	0.792	0.440	0.660	0.0129	0.0375	0.0024	0.1125
M2 - poly	2.223	0.792	0.440	0.660	0.0155	0.0392	0.0031	0.1114
M2 - M1	0.810	0.792	0.440	0.660	0.0426	0.0502	0.0109	0.0993
M3 - well	4.425	0.792	0.440	0.660	0.0078	0.0334	0.0012	0.1123
M3 - active	4.275	0.792	0.440	0.660	0.0081	0.0336	0.0013	0.1125
M3 - poly	3.825	0.792	0.440	0.660	0.0090	0.0345	0.0015	0.1130
M3 - M1	2.412	0.792	0.440	0.660	0.0143	0.0385	0.0028	0.1120
M3 - M2	0.810	0.792	0.440	0.660	0.0426	0.0502	0.0109	0.0993
M4 - well	6.027	1.122	0.630	0.770	0.0057	0.0336	0.0013	0.1107
M4 - active	5.877	1.122	0.630	0.770	0.0059	0.0338	0.0014	0.1109
M4 - poly	5.427	1.122	0.630	0.770	0.0064	0.0344	0.0015	0.1112
M4 - M1	4.014	1.122	0.630	0.770	0.0086	0.0369	0.0023	0.1110
M4 - M2	2.412	1.122	0.630	0.770	0.0143	0.0416	0.0045	0.1074
M4 - M3	0.810	1.122	0.630	0.770	0.0426	0.0544	0.0159	0.0918

3-layer metal process with thick (34 mΩ/sq) top metal

NOMINAL INTERCONNECT CAPACITANCE

Layer	H	T	S	W	Ca	Cf0	Cf1	Cc
	[µm]	[µm]	[µm]	[µm]	[fF/µm^2]	[fF/µm]	[fF/µm]	[fF/µm]
Poly1 - well	0.300	0.300	0.500	0.350	0.1151	0.0514	0.0250	0.0402
M1 - well	1.400	0.630	0.500	0.500	0.0247	0.0414	0.0061	0.0800
M1 - active	1.250	0.630	0.500	0.500	0.0276	0.0426	0.0070	0.0792
M1 - poly	0.800	0.630	0.500	0.500	0.0432	0.0475	0.0116	0.0751
M2 - well	2.930	0.720	0.500	0.600	0.0118	0.0359	0.0024	0.0921
M2 - active	2.780	0.720	0.500	0.600	0.0124	0.0364	0.0026	0.0921
M2 - poly	2.330	0.720	0.500	0.600	0.0148	0.0379	0.0033	0.0917
M2 - M1	0.900	0.720	0.500	0.600	0.0384	0.0477	0.0106	0.0840
M3 - well	4.550	1.020	0.700	0.700	0.0076	0.0351	0.0021	0.0925
M3 - active	4.400	1.020	0.700	0.700	0.0078	0.0354	0.0022	0.0926
M3 - poly	3.950	1.020	0.700	0.700	0.0087	0.0363	0.0026	0.0926
M3 - M1	2.520	1.020	0.700	0.700	0.0137	0.0403	0.0046	0.0908
M3 - M2	0.900	1.020	0.700	0.700	0.0384	0.0517	0.0151	0.0797

MINIMUM INTERCONNECT CAPACITANCE

Layer	H	T	S	W	Ca	Cf0	Cf1	Cc
	in µm	in µm	in µm	in µm	in fF/µm2	in fF/µm	in fF/µm	in fF/µm
Poly1 - well	0.330	0.270	0.535	0.315	0.1046	0.0487	0.0233	0.0371
M1 - well	1.480	0.567	0.550	0.450	0.0233	0.0399	0.0061	0.0690
M1 - active	1.330	0.567	0.550	0.450	0.0260	0.0409	0.0069	0.0685
M1 - poly	0.880	0.567	0.550	0.450	0.0392	0.0452	0.0111	0.0656
M2 - well	3.037	0.648	0.560	0.540	0.0114	0.0348	0.0026	0.0764
M2 - active	2.887	0.648	0.560	0.540	0.0120	0.0352	0.0027	0.0765
M2 - poly	2.437	0.648	0.560	0.540	0.0142	0.0366	0.0034	0.0766
M2 - M1	0.990	0.648	0.560	0.540	0.0349	0.0454	0.0102	0.0719
M3 - well	4.675	0.918	0.770	0.630	0.0074	0.0340	0.0022	0.0776
M3 - active	4.525	0.918	0.770	0.630	0.0076	0.0343	0.0023	0.0777
M3 - poly	4.075	0.918	0.770	0.630	0.0085	0.0351	0.0027	0.0780
M3 - M1	2.628	0.918	0.770	0.630	0.0131	0.0389	0.0047	0.0775
M3 - M2	0.990	0.918	0.770	0.630	0.0349	0.0492	0.0144	0.0696

MAXIMUM INTERCONNECT CAPACITANCE

Layer	H	T	S	W	Ca	Cf0	Cf1	Cc
	in µm	in µm	in µm	in µm	in fF/µm2	in fF/µm	in fF/µm	in fF/µm
Poly1 - well	0.270	0.330	0.465	0.385	0.1279	0.0542	0.0269	0.0436
M1 - well	1.320	0.693	0.450	0.550	0.0262	0.0430	0.0060	0.0936
M1 - active	1.170	0.693	0.450	0.550	0.0295	0.0443	0.0070	0.0924
M1 - poly	0.720	0.693	0.450	0.550	0.0480	0.0499	0.0122	0.0865
M2 - well	2.823	0.792	0.440	0.660	0.0122	0.0371	0.0023	0.1128
M2 - active	2.673	0.792	0.440	0.660	0.0129	0.0375	0.0024	0.1125
M2 - poly	2.223	0.792	0.440	0.660	0.0155	0.0392	0.0031	0.1114
M2 - M1	0.810	0.792	0.440	0.660	0.0426	0.0502	0.0109	0.0993
M3 - well	4.425	1.122	0.630	0.770	0.0078	0.0361	0.0020	0.1113
M3 - active	4.275	1.122	0.630	0.770	0.0081	0.0364	0.0021	0.1112
M3 - poly	3.825	1.122	0.630	0.770	0.0090	0.0373	0.0024	0.1109
M3 - M1	2.412	1.122	0.630	0.770	0.0143	0.0416	0.0045	0.1074
M3 - M2	0.810	1.122	0.630	0.770	0.0426	0.0544	0.0159	0.0918

3, 4 and 5-layer metal process with thin (55 mΩ/sq) top metal

NOMINAL INTERCONNECT CAPACITANCE

Layer	H	T	S	W	Ca	Cf0	Cf1	Cc
	[µm]	[µm]	[µm]	[µm]	[fF/µm^2]	[fF/µm]	[fF/µm]	[fF/µm]
Poly1 - well	0.300	0.300	0.500	0.350	0.1151	0.0514	0.0250	0.0402
M1 - well	1.400	0.630	0.500	0.500	0.0247	0.0414	0.0061	0.0800
M1 - active	1.250	0.630	0.500	0.500	0.0276	0.0426	0.0070	0.0792
M1 - poly	0.800	0.630	0.500	0.500	0.0432	0.0475	0.0116	0.0751
M2 - well	2.930	0.720	0.500	0.600	0.0118	0.0359	0.0024	0.0921
M2 - active	2.780	0.720	0.500	0.600	0.0124	0.0364	0.0026	0.0921
M2 - poly	2.330	0.720	0.500	0.600	0.0148	0.0379	0.0033	0.0917
M2 - M1	0.900	0.720	0.500	0.600	0.0384	0.0477	0.0106	0.0840
M3 - well	4.550	0.720	0.500	0.600	0.0076	0.0324	0.0013	0.0902
M3 - active	4.400	0.720	0.500	0.600	0.0078	0.0327	0.0014	0.0905
M3 - poly	3.950	0.720	0.500	0.600	0.0087	0.0335	0.0016	0.0913
M3 - M1	2.520	0.720	0.500	0.600	0.0137	0.0372	0.0030	0.0919
M3 - M2	0.900	0.720	0.500	0.600	0.0384	0.0477	0.0106	0.0840
M4 - well	6.170	0.720	0.500	0.600	0.0056	0.0303	0.0009	0.0858
M4 - active	6.020	0.720	0.500	0.600	0.0057	0.0304	0.0009	0.0863
M4 - poly	5.570	0.720	0.500	0.600	0.0062	0.0310	0.0010	0.0877
M4 - M1	4.140	0.720	0.500	0.600	0.0083	0.0332	0.0015	0.0910
M4 - M2	2.520	0.720	0.500	0.600	0.0137	0.0372	0.0030	0.0919
M4 - M3	0.900	0.720	0.500	0.600	0.0384	0.0477	0.0106	0.0840
M5 - well	7.790	0.720	0.500	0.600	0.0044	0.0287	0.0006	0.0797
M5 - active	7.640	0.720	0.500	0.600	0.0045	0.0288	0.0006	0.0804
M5 - poly	7.190	0.720	0.500	0.600	0.0048	0.0292	0.0007	0.0821
M5 - M1	5.760	0.720	0.500	0.600	0.0060	0.0307	0.0010	0.0871
M5 - M2	4.140	0.720	0.500	0.600	0.0083	0.0332	0.0015	0.0910
M5 - M3	2.520	0.720	0.500	0.600	0.0137	0.0372	0.0030	0.0919
M5 - M4	0.900	0.720	0.500	0.600	0.0384	0.0477	0.0106	0.0840

MINIMUM INTERCONNECT CAPACITANCE

Layer	H	T	S	W	Ca	Cf0	Cf1	Cc
	in µm	in µm	in µm	in µm	in fF/µm2	in fF/µm	in fF/µm	in fF/µm
Poly1 - well	0.330	0.270	0.535	0.315	0.1046	0.0487	0.0233	0.0371
M1 - well	1.480	0.567	0.550	0.450	0.0233	0.0399	0.0061	0.0690
M1 - active	1.330	0.567	0.550	0.450	0.0260	0.0409	0.0069	0.0685
M1 - poly	0.880	0.567	0.550	0.450	0.0392	0.0452	0.0111	0.0656
M2 - well	3.037	0.648	0.560	0.540	0.0114	0.0348	0.0026	0.0764
M2 - active	2.887	0.648	0.560	0.540	0.0120	0.0352	0.0027	0.0765
M2 - poly	2.437	0.648	0.560	0.540	0.0142	0.0366	0.0034	0.0766
M2 - M1	0.990	0.648	0.560	0.540	0.0349	0.0454	0.0102	0.0719
M3 - well	4.675	0.648	0.560	0.540	0.0074	0.0315	0.0014	0.0736
M3 - active	4.525	0.648	0.560	0.540	0.0076	0.0317	0.0015	0.0739
M3 - poly	4.075	0.648	0.560	0.540	0.0085	0.0325	0.0017	0.0749
M3 - M1	2.628	0.648	0.560	0.540	0.0131	0.0360	0.0031	0.0766
M3 - M2	0.990	0.648	0.560	0.540	0.0349	0.0454	0.0102	0.0719
M4 - well	6.313	0.648	0.560	0.540	0.0055	0.0294	0.0009	0.0688
M4 - active	6.163	0.648	0.560	0.540	0.0056	0.0295	0.0010	0.0693
M4 - poly	5.713	0.648	0.560	0.540	0.0060	0.0301	0.0011	0.0707
M4 - M1	4.266	0.648	0.560	0.540	0.0081	0.0321	0.0016	0.0745
M4 - M2	2.628	0.648	0.560	0.540	0.0131	0.0360	0.0031	0.0766
M4 - M3	0.990	0.648	0.560	0.540	0.0349	0.0454	0.0102	0.0719
M5 - well	7.951	0.648	0.560	0.540	0.0043	0.0279	0.0007	0.0629
M5 - active	7.801	0.648	0.560	0.540	0.0044	0.0280	0.0007	0.0635
M5 - poly	7.351	0.648	0.560	0.540	0.0047	0.0284	0.0008	0.0652
M5 - M1	5.904	0.648	0.560	0.540	0.0058	0.0298	0.0010	0.0701
M5 - M2	4.266	0.648	0.560	0.540	0.0081	0.0321	0.0016	0.0745
M5 - M3	2.628	0.648	0.560	0.540	0.0131	0.0360	0.0031	0.0766
M5 - M4	0.990	0.648	0.560	0.540	0.0349	0.0454	0.0102	0.0719

MAXIMUM INTERCONNECT CAPACITANCE

Layer	H	T	S	W	Ca	Cf0	Cf1	Cc
	in µm	in µm	in µm	in µm	in fF/µm2	in fF/µm	in fF/µm	in fF/µm
Poly1 - well	0.270	0.330	0.465	0.385	0.1279	0.0542	0.0269	0.0436
M1 - well	1.320	0.693	0.450	0.550	0.0262	0.0430	0.0060	0.0936
M1 - active	1.170	0.693	0.450	0.550	0.0295	0.0443	0.0070	0.0924
M1 - poly	0.720	0.693	0.450	0.550	0.0480	0.0499	0.0122	0.0865
M2 - well	2.823	0.792	0.440	0.660	0.0122	0.0371	0.0023	0.1128
M2 - active	2.673	0.792	0.440	0.660	0.0129	0.0375	0.0024	0.1125
M2 - poly	2.223	0.792	0.440	0.660	0.0155	0.0392	0.0031	0.1114
M2 - M1	0.810	0.792	0.440	0.660	0.0426	0.0502	0.0109	0.0993
M3 - well	4.425	0.792	0.440	0.660	0.0078	0.0334	0.0012	0.1123
M3 - active	4.275	0.792	0.440	0.660	0.0081	0.0336	0.0013	0.1125
M3 - poly	3.825	0.792	0.440	0.660	0.0090	0.0345	0.0015	0.1130
M3 - M1	2.412	0.792	0.440	0.660	0.0143	0.0385	0.0028	0.1120
M3 - M2	0.810	0.792	0.440	0.660	0.0426	0.0502	0.0109	0.0993
M4 - well	6.027	0.792	0.440	0.660	0.0057	0.0311	0.0008	0.1083
M4 - active	5.877	0.792	0.440	0.660	0.0059	0.0313	0.0008	0.1088
M4 - poly	5.427	0.792	0.440	0.660	0.0064	0.0318	0.0009	0.1101
M4 - M1	4.014	0.792	0.440	0.660	0.0086	0.0341	0.0014	0.1128
M4 - M2	2.412	0.792	0.440	0.660	0.0143	0.0385	0.0028	0.1120
M4 - M3	0.810	0.792	0.440	0.660	0.0426	0.0502	0.0109	0.0993
M5 - well	7.629	0.792	0.440	0.660	0.0045	0.0295	0.0006	0.1022
M5 - active	7.479	0.792	0.440	0.660	0.0046	0.0296	0.0006	0.1029
M5 - poly	7.029	0.792	0.440	0.660	0.0049	0.0300	0.0006	0.1047
M5 - M1	5.616	0.792	0.440	0.660	0.0061	0.0316	0.0009	0.1096
M5 - M2	4.014	0.792	0.440	0.660	0.0086	0.0341	0.0014	0.1128
M5 - M3	2.412	0.792	0.440	0.660	0.0143	0.0385	0.0028	0.1120
M5 - M4	0.810	0.792	0.440	0.660	0.0426	0.0502	0.0109	0.0993

Junction Diode

- **Leakage**
- **Diode**

The measured values in this table are based on I3T50 material.

structure	test	Corner	Simulated	Measured
PPNWD Stripe (435.2*1.4*80)	Irev_3,6V (nA) T= 150 C	min typ max	20 40 78.2	N.A. 43.8 60
PPNWD Stripe (435.2*1.4*80)	Irev_3,6V (nA) T = 200C	min typ max	278 587 1169	N.A. 352 446
NPPWD Stripe (428*1.4*44)	Irev_3,6V (nA) T = 150 C	min typ max	12.2 23 50.7	N.A 25 27.9
NPPWD Stripe (428*1.4*44)	Irev_3,6V (nA) T = 200 C	min typ max	199 391 818	N.A. 315 348
PWLNED Stripe (432.8*6.2*44)	Irev_10V T = 150 C	min typ max	17 33 65	N.A. 40 45
PWLNED Stripe (432.8*6.2*44)	Irev_10V T = 200 C	min typ max	264 508 1007	N.A. 449 500
PWLNED Square (432.8*372*2)	Irev_10V T = 150C	min typ max	12 21.5 40.1	N.A. 16 18
PWLNED Square (432.8*372*2)	Irev_10V T = 200C	min typ max	260 466 910	N.A. 430 503

Breakdown Voltages

Junction	Units	MIN	TYP	MAX
N+/PWELL	Volts	6.0		
P+/NWELL	Volts			-6.0
P+/NLDD (CLIOD)	Volts	5.5	6.5	8.5

Power Metal Electrical Rules:

Power Metal electrical characteristics:

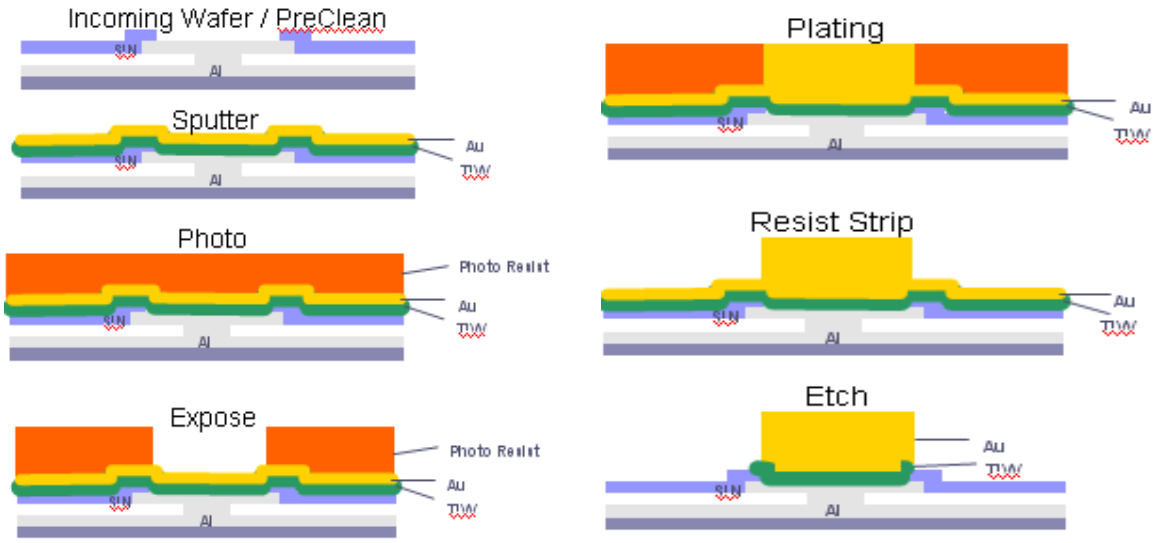
- MetalEP Sheet Resistivity: Mean=1.75m-ohm/,; Sigma=0.045
- MetalEP TCR : 4000/C^{o}
- Resistance per ViaEP (15um): 6.8 m-ohm
- Resistance per ViaEP (5um): 14.5 m-ohm

Electromigration Rules:

- For CMOS aluminum layers, follow the standard C35U electromigration rules
- MetalEP current carrying capability: Use the same current-density limitations as for the Al alloys.

Power Metal Process flow at subcon:

Power metal is comprised of a thin Titanium–Tungsten barrier layer and a thick Gold layer.



Power Metal Tolerances (for reference):

item	standard specification
1 Bump Height	+/- 3.0 um
1.1 Uniformity within wafer	</= 4.0 um
1.2 Co-planarity within Die	</= 2.0 um
2 Bump Size	width : +/- 3.0 um
	length : +/* 3.0 um
3 Roughness	</= 3.0 [rim included] as passivation thickness < 2.0 um
4 Shear Strength	>/= 4.9 g/mil^2 [7.2 e-3 g/um^2
5 Hardness	Target +/- 15 HV; Target 45 ~ 65 HV
6 Bumping sidewall	87 ~ 90 degree
7 Bumping method	Electroplating
8 Bump Material	99.9 + % pure gold
9 UBM Deposition Method	sputtering