I3T25 ESD Layout Rules Manual

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I3T25 ESD Layout Rules Manual

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Revision History

Revision	Requestor	Release Date	Description
2.0	JL	03-May-2010	Added exceptions for rules 50.11, XP.6 and 8.3. (This document is in-line with Rev2.7 of library amis350ucasea.)
1.0	JL	14-Jan-2008	New Document

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Introduction

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I3T25 ESD Layout Rules Manual - Introduction

PURPOSE

This Design Rule Manual provides the ON Semiconductor Belgium BVBA Specifications for ESD Layout Rules for 0.35 µm based CMOS Intelligent Interface Technology I3T25. The I3T25 technology is based on the C035U core CMOS, low voltage, mixed-signal C035U technology platform and, as such, incorporates all core C035U layout rules.

The CMOS process within the I3T25 technology is a single level poly, twin-tub CMOS process using a n-type epitaxial layer on top of a p-type substrate.

SCOPE

This document applies to Design Engineers, Technology Engineers, CAD Engineers, Process Engineers, Quality Assurance Engineers, Reliability Engineers and Product Engineers.

The set of rules presented in this document has to be combined with the basic list of rules described in the DES-0005 'DESIGN RULE MANUAL - Core CMOS in C035U-based Technologies' and the 1000115 'I3T25/C035U Specific (0.35 µm) Design Rules'.

REFERENCE DOCUMENTS

Layout Rules:

DES-0005	C035U (0.35 Micron) Core CMOS Design Rules
07-0104	C035U (0.35 Micron) Core ESD Layout Rules Manual
1000115	I3T25 (0.35 um) Design Rules
1000033	Assembly/Probe related Layout Rules

Electrical and Process Performance:

DES-0005	C035U (0.35 Micron) Core CMOS Design Rules
1000115	I3T25 (0.35 um) Design Rules
DES-0032	Reliability Requirement File - I3T Technologies
PTE-0024	Low voltage and Flash Parametric Test Structures for 80 um scribe inserts in I3Txx technologies
PTE-0031	Description of the Measured Structures, Parameters and Measurement Conditions for the 70 UM SLM'S, used in the Low voltage & Flash part of the I3TXX Technologies

GLOSSARY

DRC	Design Rule Check
GDS	Graphical Design System
LVS	Layout Versus Schematic
OTP	One Time Programmable
TD	Technology Development Department
TRD	Technology R&D Department

GENERAL REQUIREMENTS

Responsibilities

It is the responsibility of the ON Semiconductor TRD department to maintain this document and ensure its content is correct and up to date.
It is the responsibility of the ON Semiconductor TD/DST department to create and maintain technology files consistent with the information contained in this document; technology files include DRC, LVS and GDS layer stream tables.
Updates of this document are possible. It is the user's responsibility to consult the document control center on the availability of updated revisions of this specification.

Safety Requirements

NA.

Equipment and Material

NA.

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Exceptions Rules for ESD Components of the AMIS350UCASEA Library

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Exceptions Rules for ESD Components of the AMIS350UCASEA Library

Several exceptions are applied to these components; either because some of the common rules (in DES-0005), or some I3T25 specific rules (1000115), or some C035U ESD rules (07-0104) are violated.

An overview of the exceptions related to the following components is given in these tables:

Table 1: Exceptions related to the DES-0005 C035U (0.35 Micron) Core CMOS Design Rules document

Rule Name	Rule Description	Rule Value	Notes
1.6	See DES-0005	See DES-0005	Exception for : ESD18_IO
50.7	See DES-0005	See DES-0005	Exception for : ESD18_IO
50.11	See DES-0005	See DES-0005	Exception for: ESDCGNMOS_2kV, ESD5_SUP, ESD18_IO, ESD25_DIODE, ESD_OTPSEC
XP.6	See DES-0005	See DES-0005	Exception for: ESDCGNMOS, ESD18_SUP, ESD14_SUP

Table 2: Exceptions related to the 07-0104 C035U (0.35 Micron) Core ESD Layout Rules Manual

Rule Name	Rule Description	Rule Value	Notes
LE.3a	See 07-0104	See 07-0104	Exception for : ESDGATE_CLAMP
LNE.5	See 07-0104	See 07-0104	Exception for : ESDGATE_CLAMP
LNE.6	See 07-0104	See 07-0104	Exception for : ESDGATE_CLAMP
LNE.7	See 07-0104	See 07-0104	Exception for : ESDGATE_CLAMP
LE.9	See 07-0104	See 07-0104	Exception for : ESDGATE_CLAMP

Table 3: Exceptions related to the 1000115 I3T25 (0.35 um) Design Rules

Rule Name	Rule Description	Rule Value	Notes
8.3	See 1000115	See 1000115	Exception for: ESD18_IO, ESD_OTPSEC, ESDCGNMOS