C035U (0.35 Micron) Core ESD Layout Rules Manual

Owner: Technology Research & Development

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C035U (0.35 Micron) Core ESD Layout Rules Manual (07-0104)

Revision History

Revision	Requestor	Release Date	Description
3.0	GJ, HDV	02-Dec-2008	Rule value changes: -LE.3b changed from 70.00 to 100.00 -LNE.7 changed from 4.00 to 3.50
2.0	HDV,GJ	10-Jul-2007	-Introduce exception to LNE.7 on ENMIOCL
1.0	GJ, HDV	25-May-2007	-This new document contains the devices enmio/epmio which are now official ESD devices -Some rules were split up for enmio and enmiocl -Rule value adaptations were made for rules LE.3a, LE.4a, LE.4b -New rules LE.3cl, LE.4cl, LE.15cl specifically for enmiocl

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Introduction and Definitions

07-0104 Rev: 3.0

Confidential

Introduction and Definitions

PURPOSE

This document applies to Design Engineers, Technology Engineers, CAD Engineers, Process Engineers, Quality Assurance Engineers, Reliability Engineers and Product Engineers.
The set of rules presented in this document has to be combined with the basic list of rules described in the DES-0005 document 'C035U (0.35 Micron) Core CMOS Design Rules'.

SCOPE

This Design Rule Manual provides the AMIS Belgium BVBA Specifications for ESD Layout Rules for 0.35 µm CMOS Technologies. The CMOS process is a single level poly, twin-tub CMOS process using a n-type epitaxial layer on top of a p-type substrate.

REFERENCE DOCUMENTS

Layout Rules:

DES-0005	C035U (0.35 Micron) Core CMOS Design Rules
1000033	Assembly/Probe related Layout Rules

Electrical & Process Performance:

DES-0005	C035U (0.35 Micron) Core CMOS Design Rules

GLOSSARY

DRC	Design Rule Check
GDS	Graphical Design System
LVS	Layout Versus Schematic
OTP	One Time Programmable
PD	Product Development Department
TRD	Technology R&D Department

GENERAL REQUIREMENTS

Responsibilities

It is the responsibility of the AMIS TRD department to maintain this document and ensure its content is correct and up to date.
It is the responsibility of the AMIS PD/CAD department to create and maintain technology files consistent with the information contained in this document; technology files include DRC, LVS and GDS layer stream tables.
Updates of this document are possible. It is the user's responsibility to consult the document control center on the availability of updated revisions of this specification.

Safety Requirements

NA.

Equipment and Material

NA.

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Device Specific Layout Rules

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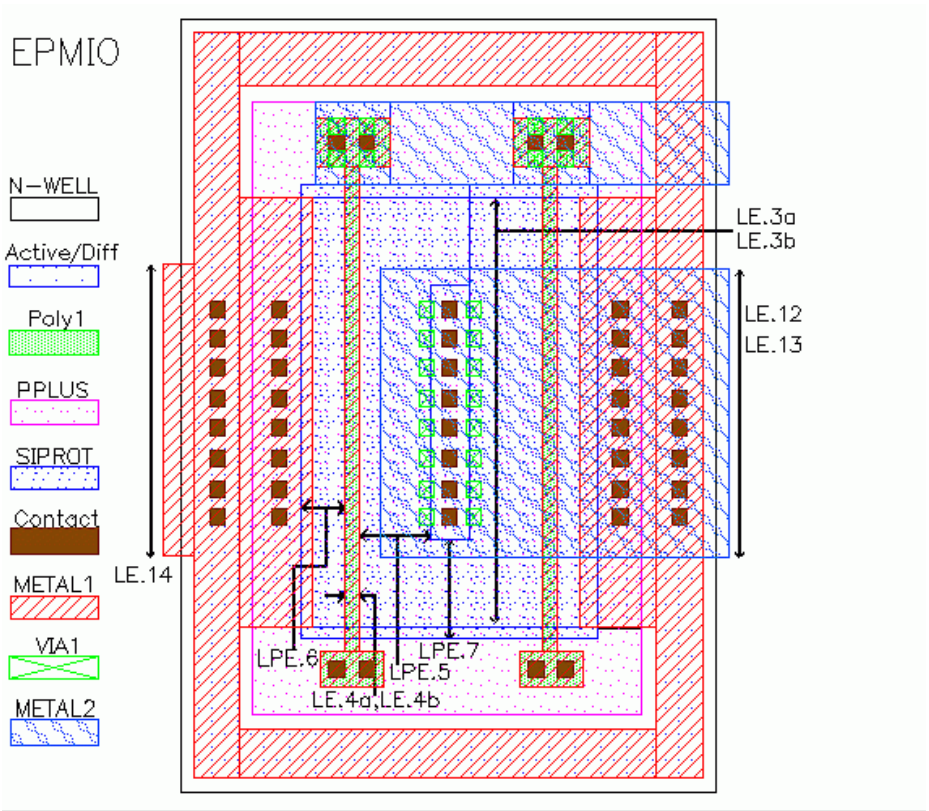
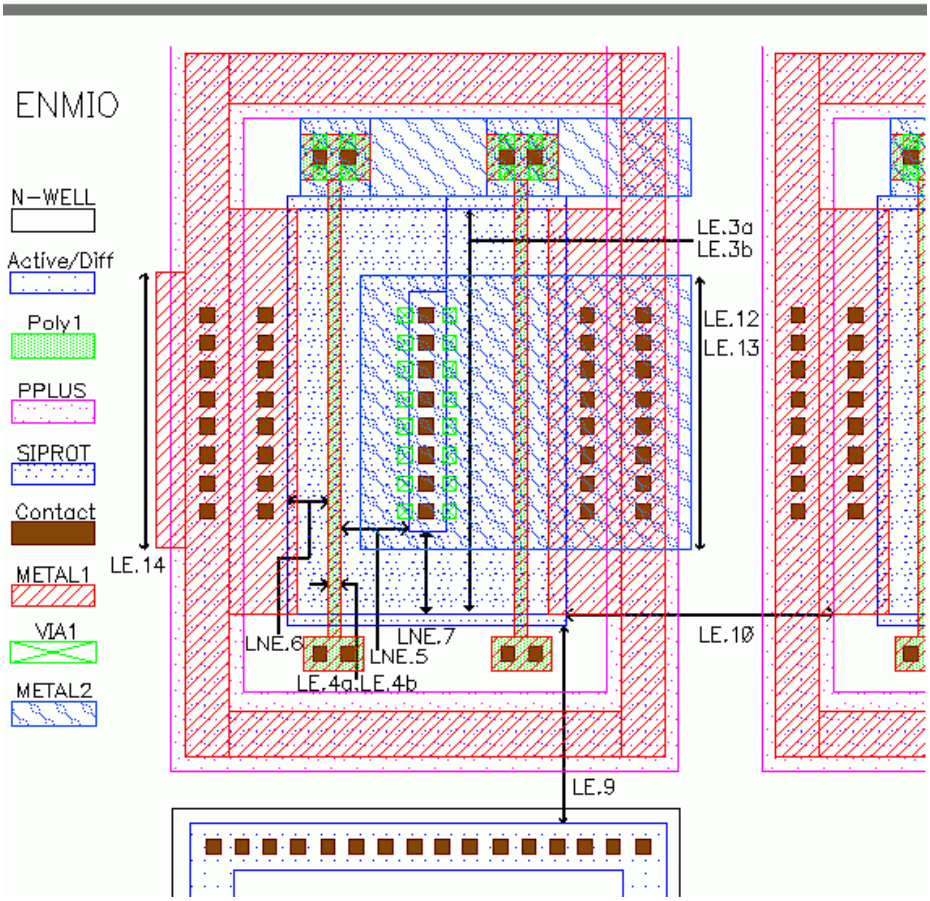
C035U_ESD (0.35 Micron) ENMIO / EPMIO / ENMIOCL Layout Rules





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Note 1: ENMIO, EPMIO and ENMIOCL are non-salicided source/drain/gate CMOS devices. The intersection of SIPROT layer with the drain ACTIVE area is different from that with source ACTIVE area. In order to properly recognize the device the DREC marking layer is placed over the device as follows: DREC is marking the ENMIO, EPMIO and ENMIOCL gate and DREC extends into the source ACTIVE with 0.1um.

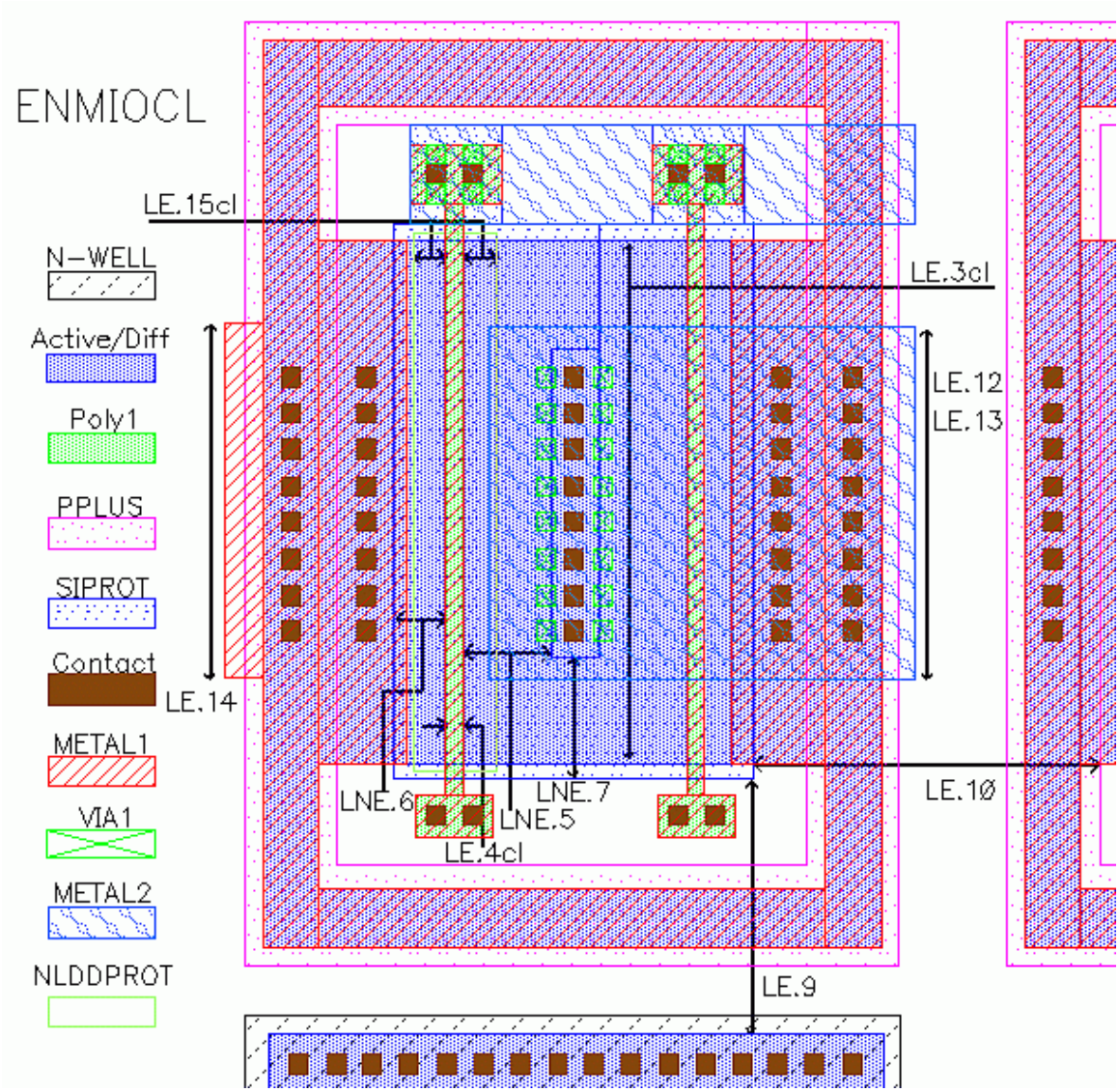
Note 2: ENMIO and EPMIO are with intended use as input/output self-protected transistors. In order to meet 4KV HBM specification, recommendation is as follows: Minimum total finger width for ENMIO = 400µm, Minimum total finger width for EPMIO = 600µm. These recommendations are implemented in parameterized cells for these devices (available in the design kit). These are also documented in the ESD guidelines for technologies in the C035U family.

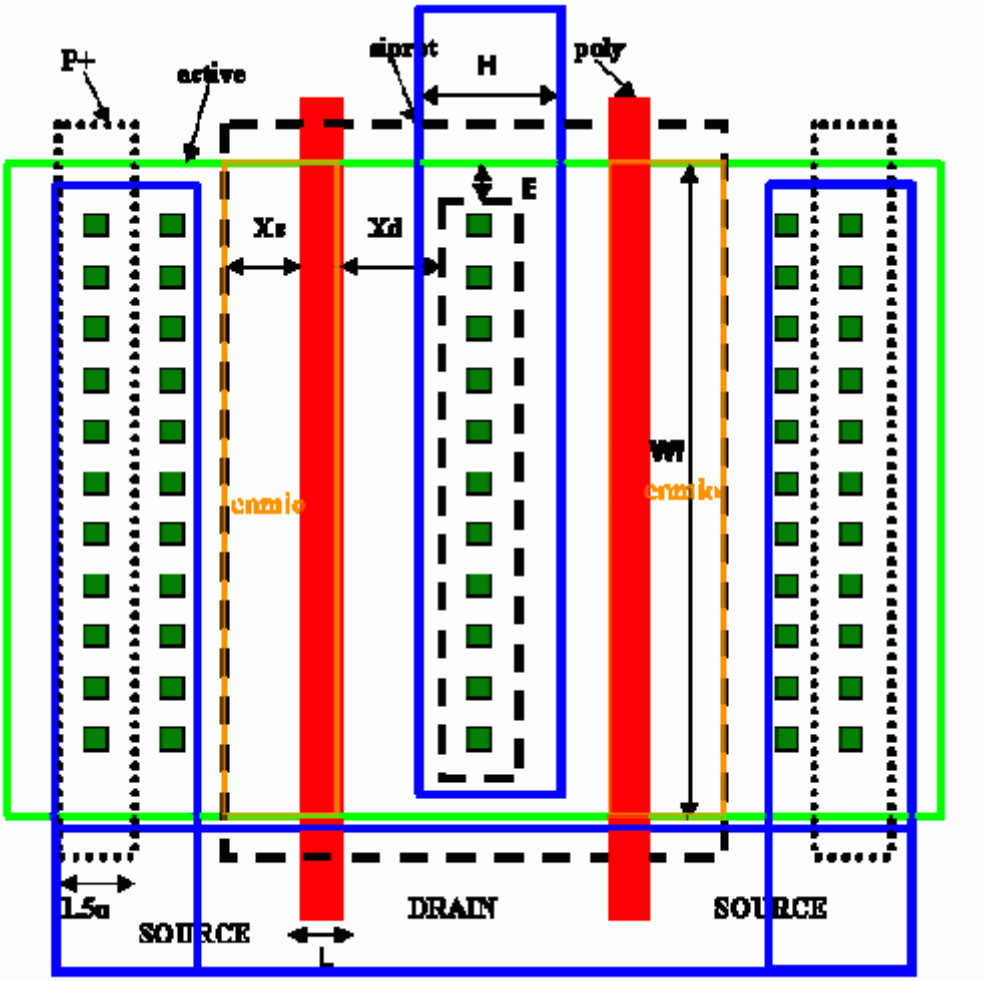
Note 3: ENMIOCL is a primitive cell of ESD protections used in IO and ESD libraries. The main difference between ENMIO and ENMIOCL is the presence of NLDDPROT layer on the ENMIOCL.

Rule Name	Rule Description	Rule	Units	Rule Type	Notes
LE.3a	Minimum Finger width for ENMIO, EPMIO and ENMIOCL	25.00	µm	*	Recommended 50 um In order to meet 4KV HBM specification, recommendation is as follows: Minimum total finger width for ENMIO = 400µm, Minimum total finger width for EPMIO = 600µm.
LE.3b	Maximum Finger width for ENMIO and EPMIO	100.00	µm	*	Recommended 50 um, applies only to ENMIO and EPMIO
LE.3cl	Maximum Finger width for ENMIOCL	80.00	µm	*	Recommended 50 um, applies only to ENMIOCL
LE.4a	Minimum Poly length of ENMIO and EPMIO	0.45	µm	*	
LE.4b	Maximum Poly length of ENMIO, EPMIO and ENMIOCL	0.50	µm	*	
LE.4cl	Minimum Poly length of ENMIOCL	0.40	µm	*	Applies only to ENMIOCL
LNE.5	Minimum SIPROT enclosure of POLYSILICON towards drain of ESD NMOS	3.00	µm	*	Applies to both ENMIO and ENMIOCL
LNE.6	Minimum SIPROT enclosure of POLYSILICON towards source of ENMIO	2.00	µm	*	Applies only to ENMIO and ENMIOCL
LNE.7	Minimum width of siprot layer on ACTIVE on edge side of ENMIO	3.50	µm	*	Applies only to ENMIO and ENMIOCL (except for P+ active of CLIOD7 inside the device)
LPE.5	Minimum SIPROT enclosure of POLYSILICON towards drain of EPMIO	2.00	µm	*	Applies only to EPMIO
LPE.6	Minimum SIPROT enclosure of POLYSILICON towards source of EPMIO	1.50	µm	*	Applies only to EPMIO
LPE.7	Minimum width of SIPROT layer on edge side of EPMIO	2.00	µm	*	Applies only to EPMIO
LE.8	Minimum Pwell bulk enclosure of P+ active	1.00	µm	*	
LE.9	Minimum distance of N-Well guard ring and nearest N+ active inside a Pwell diffusion, to kill parasitic field MOS transistors. If a P+ active tap is between them, a distance of 2 um is enough	7.00	µm	*	
LE.10	Minimum distance between N+ active areas in a Pwell implanted region, when not at the same potential, to kill parasitic field MOS. If a P+ active tap is between them, a distance of 2um is enough	7.00	µm	*	
LNE.11	Minimum enclosure of bulk contact in the abutted source active area by p+. A P+ active abutted diffusion strip should be placed between two NMOS source sites for ESD NMOS	0.10	µm	*	Applies to both ENMIO and ENMIOCL
LPE.11	Minimum spacing of bulk contacts in the abutted source active area to p+. A N+ abutted diffusion strip should be placed between two PMOS source sites	0.10	µm	*	Applies only to EPMIO
LE.12	Minimum total width of the metal 2 tracks going to a VSS or VDD bus	25.00	µm	***	The rule is a recommendation for current density and cannot be checked at this time.

LE.13	Minimum metal width on drain side of ESD MOS devices	5.00	µm	***	The rule is a recommendation for current density and cannot be checked at this time.
LE.14	Minimum metal width on source side of ESD MOS devices	3.50	µm	***	The rule is a recommendation for current density and cannot be checked at this time.
LE.15cl	Minimum enclosure of POLYSILICON by NLDDPROT of ENMIOCL	1.00	µm	*	Applies only to ENMIOCL

(Rule Type: * Required, ** Recommended, Checked, *** Suggested, NOT Checked)


ENMIOCL
LE.15cl
N-WELL
Active/Diff
Poly1
PPLUS
SIPROT
Contact
METAL1
VIA1
METAL2
NLDDPROT
LE.14
LE.3cl
LE.12
LE.13
LE.10
LE.9
LNE.6
LNE.7
LNE.5
LE.4cl



Sketch of ENMIO device with main geometry parameters

ENMIOCL (with CLIOD7 shown inside)